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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	DDR3, LPDDR2
Graphics Acceleration	Yes
Display & Interface Controllers	DCU, GPU, LCD, VideoADC, VIU
Ethernet	10/100Mbps (2)
SATA	-
USB	USB 2.0 OTG + PHY (2)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	ARM TZ, Hashing, RNG, RTC, RTIC, Secure JTAG, SNVS, TZ ASC, TZ WDOG
Package / Case	364-LFBGA
Supplier Device Package	364-MAPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/svf532r3k2cmk4

1 Ordering parts

1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web.

1. To determine the orderable part numbers for this device, go to www.freescale.com and search the required part number. The part numbering format is described in the section that follows.

2 Part identification

2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

2.2 Part Number Format

The figure below represents the format of part number of this device.

4 Handling ratings

4.1 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-2000	2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	500	V	2
I_{LAT}	Latch-up Current at ambient temperature of 85 °C	-100	100	mA	

1. Determined according to the AEC spec AEC-Q100-002 for HBM
2. Determined according to AEC spec AEC-Q100-011

4.2 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2
	Solder temperature, leaded	—	245		

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.3 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

6.2.1.5 External NPN Ballast

The internal main regulator requires an external NPN ballast transistor to be connected as shown in the following figure as well as an external capacitance to be connected to the device in order to provide a stable 1.2V digital supply to the device. The HPREG design allows for collector voltage lower than VDDREG value. See AN4807 at www.freescale.com .

NOTE

To not overload BCTRL output, collector voltage should appear no later than VDDREG / VDD33 (3.3V).

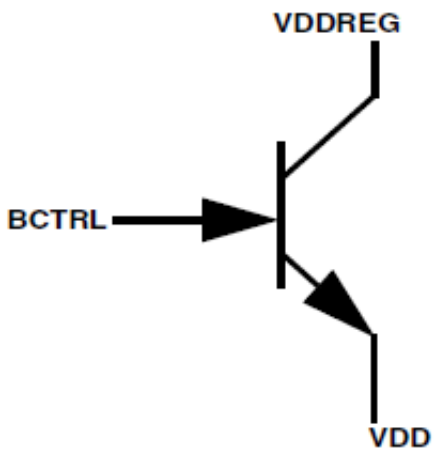

Figure 3. External NPN Ballast connections

Table 6. BCTRL OUTPUT specification

Parameter	Value	Comments
BCTRL OUTPUT specification	20mA	BCTRL driver can not drive more than 20mA current
Maximum pin voltage	VDDREG-0.5V	For Example, VDDREG =3.0V BCTRL should not exceed 2.5V.

Table 7. Assumptions For calculations

Parameter	Value
VDDREG	3.0V to 3.6V with typical value of 3.3V
Max DC Collector current	0.85A @85 °C
Emitter voltage	1.2V to 1.25V
Collector voltage	Equal to VDDREG

6.2.3.3 LDO_3P0

Table 14. LDO_3P0 parameters

Specification	Min	Typ	Max	Unit	Comments
Input OTG VBUS Supply	4.4		5.25	V	
Input HOST VBUS Supply	4.4		5.25	V	
VDD3P0_OUT	2.9	3.0	3.1	V	Regulator output at default setting
I_out	-		50	mA	500 mV drop-out voltage
Regulator output programming range	2.625		3.4	V	Programmable in 25mV steps
[P:][C:] Brownout Voltage	2.75	2.85		V	
Brownout offset step	0	-	175	mV	Programmable in 25mV steps
Minimum external decoupling capacitor	1	-	-	µF	low ESR

NOTE

These values are with Anadig_REG_3P0[ENABLE_ILIMIT]= 0 and Anadig_REG_3P0[ENABLE_LINREG]= 1. It is required to set these values before using USB.

6.2.4 Power consumption operating behaviors

Table 15. Power consumption operating behaviors

Symbol	Description	Typ.[1]	Max.[2]	Unit	Notes
I_{DD_RUN}	Run mode current — All functionalities of the chip available	400	850	mA	
I_{DD_WAIT}	Wait mode high frequency current at 3.3 V ± 10%	80	500	mA	3
I_{DD_LPRUN}	Low-power run mode current at 3.3 V ± 10%, 24MHz operation, PLL Bypass.	13	325	mA	4
I_{DD_ULPRUN}	Ultra-low-power run mode current at 3.3 V ± 10%	12	395	mA	5
I_{DD_STOP}	Stop mode current at 3.3 V ± 10%	7	300	mA	6
I_{DD_LPS3}	Low-power stop3 mode current at 3.3 V ± 10%	300	1300	uA	7
I_{DD_LPS2}	Low-power stop 2 mode current at 3.3 V ± 10%	50	875	uA	8
I_{DD_VBAT}	Battery backup mode	5	45	uA	9

1. The Typ numbers represent the average value taken from a matrix lot of parts across normal process variation at ambient temperature.

2. The Max numbers represent the single worst case value taken from a matrix lot of parts across normal process variation at maximum temperature.
3. CA5, CM4 cores halted
4. 24MHz operation, PLL Bypass
5. 32 kHz /128 kHz operation, PLL Off
6. Lowest power mode with all power retained, RAM retention and LVD protection.
7. Standby Mode. 64K RAM retention. I/O states held. ADCs/DACs optionally power-gated. RTC functional. Wakeup from interrupts. Fast IRC enabled.
8. Standby Mode 16K RAM retention. I/O states held. ADCs/DACs optionally power-gated. RTC functional. Wakeup from interrupts. Fast IRC enabled.
9. All supplies OFF, SRTC, 32kXOSC ON, tampers and monitors ON. 128k IRC optionally ON.

6.2.5 USB PHY current consumption

6.2.5.1 Power Down Mode

Everything powered down, including the VBUS valid detectors, typ condition.

Table 16. USB PHY Current Consumption in Normal Mode

	USBx_VBUS (3.0V) Avg	VDD33_LDOIN (2.5V) Avg	VDD33_LDOIN (1.1V) Avg
Current	5.1 µA	1.7 µA	<0.5 µA

NOTE

The currents on the 2.5 voltage regulator and 3.0 voltage regulator were identified to be the voltage divider circuits in the USB-specific level shifters.

6.2.6 EMC radiated emissions operating behaviors

Table 17. EMC radiated emissions operating behaviors

Symbol	Condition[1]	Clocks	Frequency band [2]	Level (Typ)[3]	Unit
V_{EME}	Device Configuration, test conditions and EM testing per standard IEC 61967-2; Supply voltages: VDD= 5.0 V VDD33 = 3.3 V VDD15 = 1.5 V VDD12 = 1.2 V Temp = 25°C	FCPU = 396 MHz FBUS = 66 MHz External Crystal = 24 MHz	150 KHz – 50 MHz	22	dBµV
			50 MHz – 150 MHz	24	
			150 MHz – 500 MHz	25	
			500–1000	20	
			IEC level[4]	K	—

1. Measurements were made per IEC 61967-2 while the device was running basic application code.
2. Measurements were performed on the BGA364 version of the device

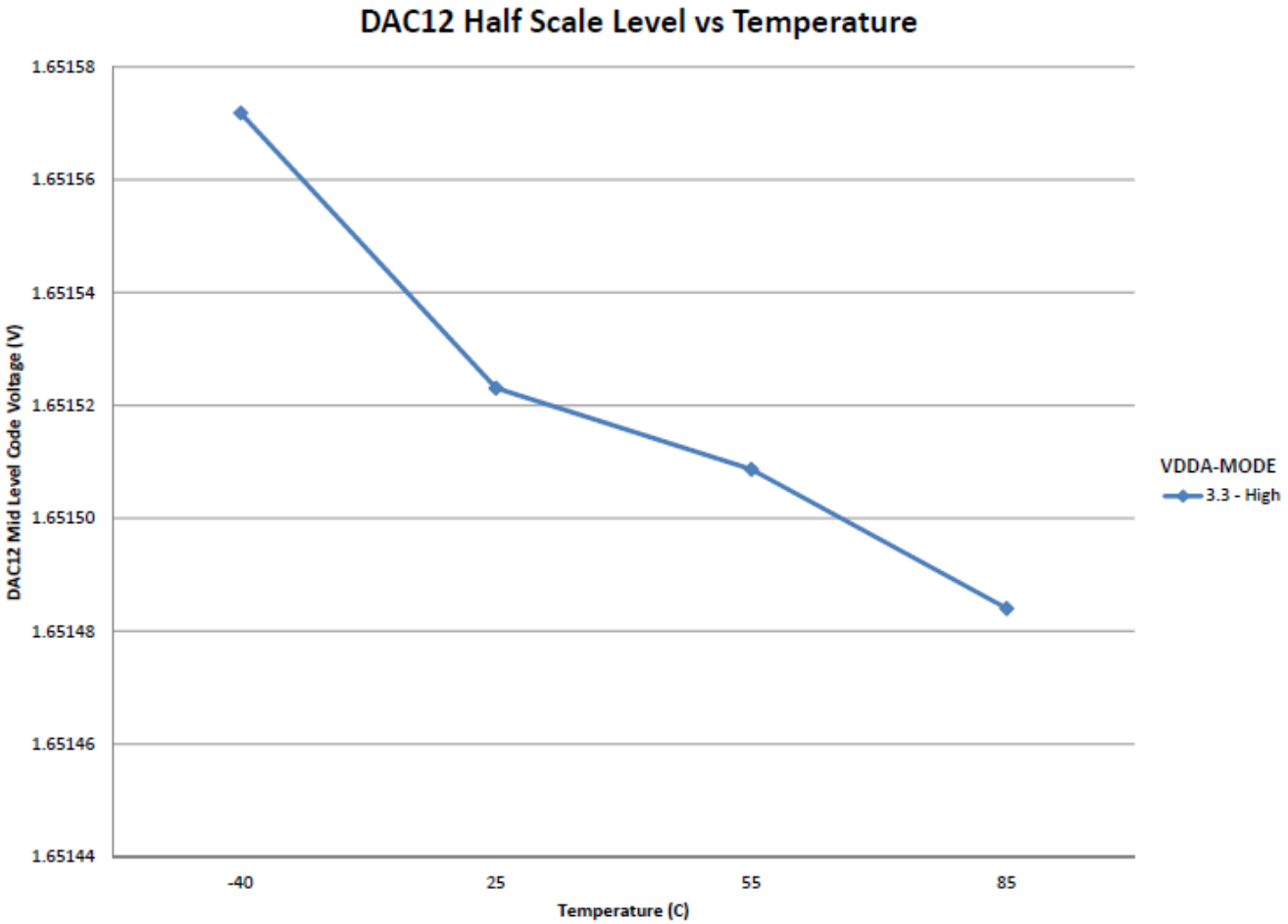

Figure 11. Offset at half scale vs. temperature

9.1.3 VideoADC Specifications

This section describes the electrical specification and characteristics of the VideoADC Analog Front End.

Table 35. VideoADC Specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
VDDA33_AFE	Supply voltage	3.0	3.3	3.6	V	—
	Supply current	—	—	41	mA	—
VDDA12_AFE	Supply voltage	1.1	1.2	1.26	V	—
	Supply current	—	—	14	mA	—
V_{in}	Input signal voltage range	0	0.5	1.4	V	—
	External AC coupling	10	47		nF	The external AC coupling capacitance cannot be too large.

Table continues on the next page...

NOTE

VideoADC 3.3V and 1.2V power supply pins should be decoupled to their respective grounds using low-ESR 100nF capacitors

NOTE

If possible, avoid using switched voltage regulators for the AFE power domains. Use linear voltage regulators instead.

NOTE

The 3.3V and 1.2V power domains should be separated from other circuitry on the board by inductors/beads to filter out high frequency noise.

9.2 Display and Video interfaces

9.2.1 DCU Switching Specifications

9.2.1.1 Interface to TFT panels (DCU0/1)

This section provides the LCD interface timing for a generic active matrix color TFT panel. In the figure below, signals are shown with positive polarity. The sequence of events for active matrix interface timing:

- PCLK latches data into the panel on its positive edge (when positive polarity is selected). In active mode, PCLK runs continuously. This signal frequency could be from 5 to 66 MHz depending on the panel type.
- HSYNC causes the panel to start a new line. It always encompasses at least one PCLK pulse.
- VSYNC causes the panel to start a new frame. It always encompasses at least one HSYNC pulse.
- DE acts like an output enable signal to the LCD panel. This output enables the data to be shifted onto the display. When disabled, the data is invalid and the trace is off.

Figure 14. TFT LCD interface timing overview[1]

1. In the figure, LD[23:0]" signal is "line data," an aggregation of the DCU's RGB signals—R[0:7], G[0:7] and B[0:7].

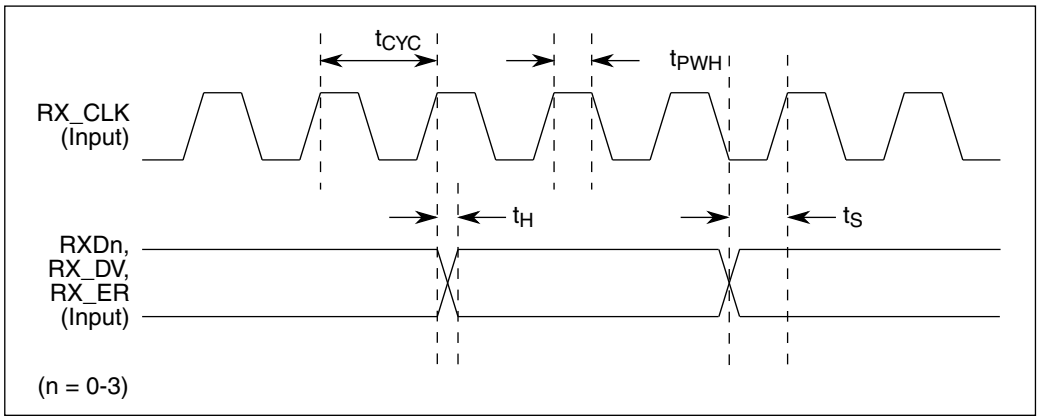

Figure 22. MII receive signal timing diagram

Table 42. Receive signal timing for MII interfaces

Characteristic		MII Mode			Unit
		Min	Typ	Max	
RX_CLK clock period (100/10 MBPS)	t_{CYC}		40/400		ns
RX_CLK duty cycle, t_{PWH}/t_{CYC}		45	50	55	%
Input setup time before RX_CLK	t_s	5			ns
Input hold time after RX_CLK	t_h	5			ns

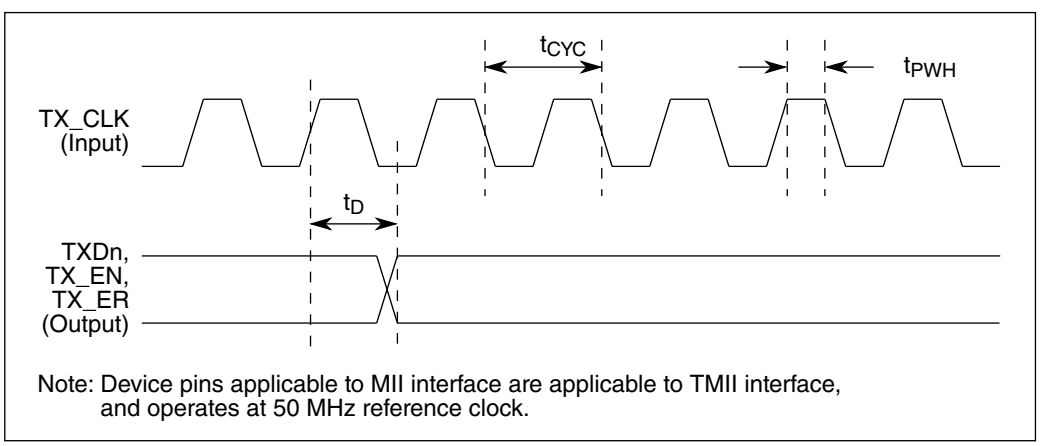

Figure 23. MII transmit signal timing diagram

Table 43. Transmit signal timing for MII interfaces

Characteristic		MII Mode			Unit
		Min	Typ	Max	
TX_CLK clock period (100/10 MBPS)	t_{CYC}		40/400		ns
TX_CLK duty cycle, t_{PWH}/t_{CYC}		45	50	55	%
Out delay from TX_CLK	t_D	2		25	ns

9.5.4 DDR controller specifications

9.5.4.1 DDR3 Timing Parameters

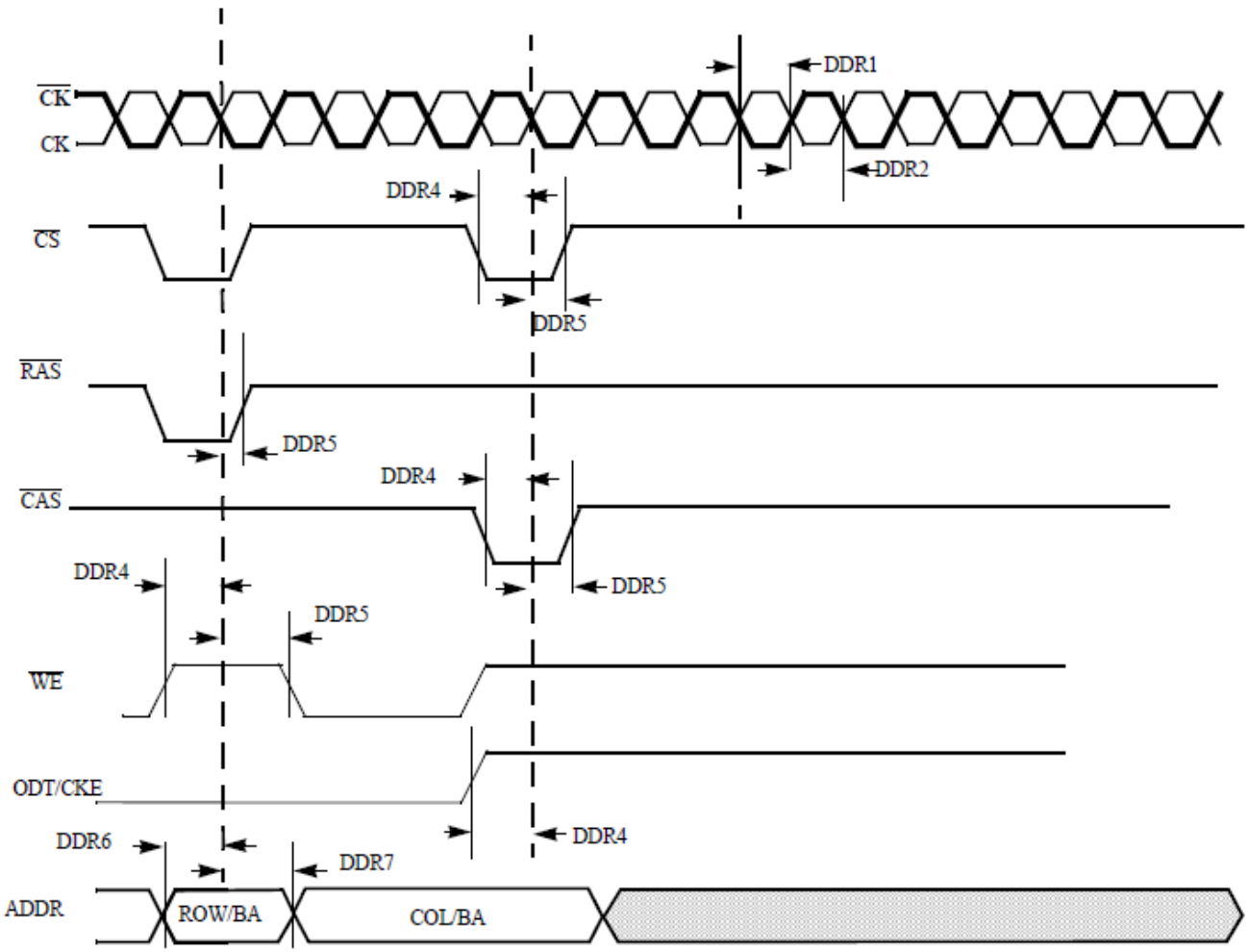

Figure 41. DDR3 Command and Address Timing Parameters

NOTE

RESET pin has a external weak pull DOWN requirement if DDR3 memory is NOT required to support content retention in the device low power modes where core voltage is off but DRAM voltage is on.

9.5.4.2 DDR3 Read Cycle

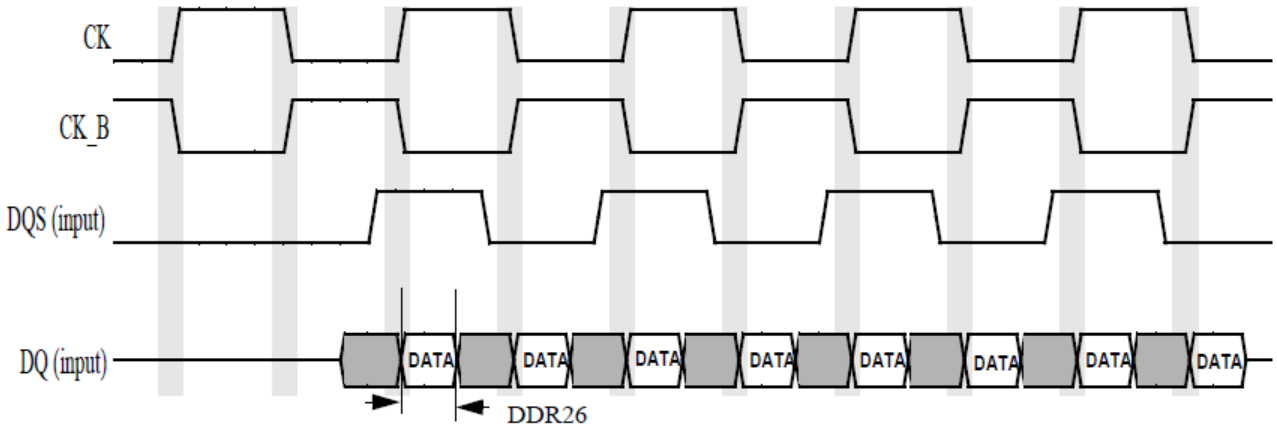

Figure 42. DDR3 Read Cycle

Table 55. DDR3 Read Cycle

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
DDR26	Minimum required DQ valid window width	-	750	-	ps

NOTE

To receive the reported setup and hold values, read calibration should be performed in order to locate the DQS in the middle of DQ window.

NOTE

All measurements are in reference to Vref level.

NOTE

Measurements were done using balanced load and 25 ohms resistor from outputs to VDD_REF

9.5.4.3 DDR3 Write cycle

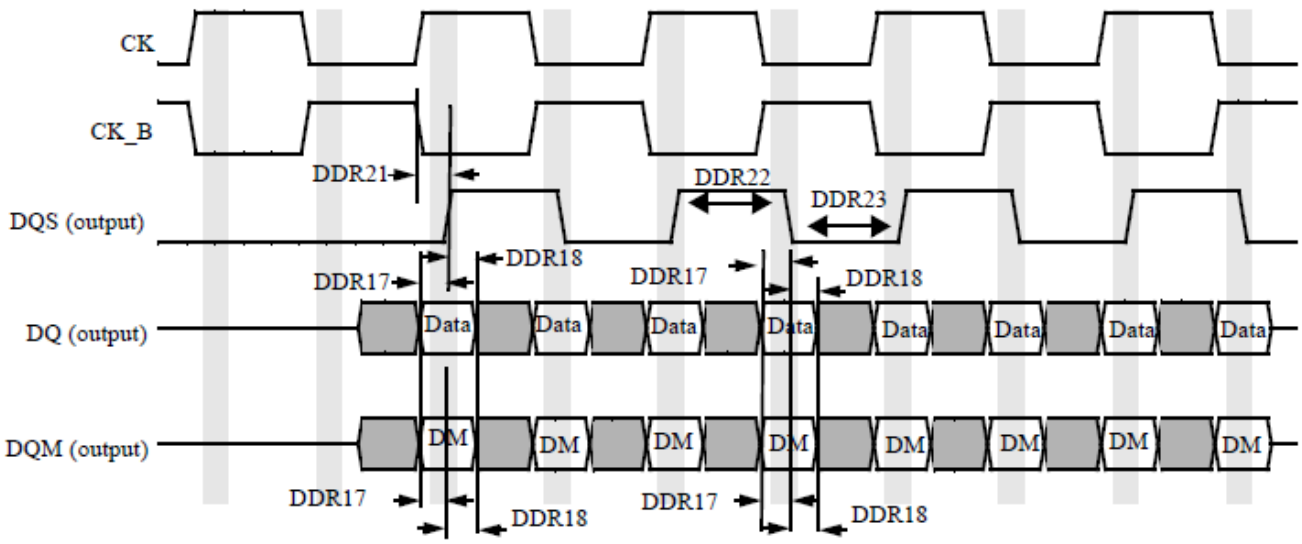

Figure 43. DDR3 Write cycle

Table 56. DDR3 Write cycle

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
DDR17	DQ and DQM setup time to DQS (differential strobe)	tDS	240	—	ps
DDR18	DQ and DQM hold time to DQS (differential strobe)	tDH	215	—	ps
DDR21	DQS latching rising transitions to associated clock edges	tDQSS	-0.25	+0.25	tCK
DDR22	DQS high level width	tDQSH	0.45	0.55	tCK
DDR22	DQS low level width	tDQSL	0.45	0.55	tCK

NOTE

To receive the reported setup and hold values, write calibration should be performed in order to locate the DQS in the middle of DQ window.

NOTE

All measurements are in reference to Vref level.

NOTE

Measurements were done using balanced load and 25 ohms resistor from outputs to VDD_REF.

NOTE

Measurements were done using balanced load and 25 ohms resistor from outputs to VDD_REF.

9.5.4.5 LPDDR2 Read Cycle

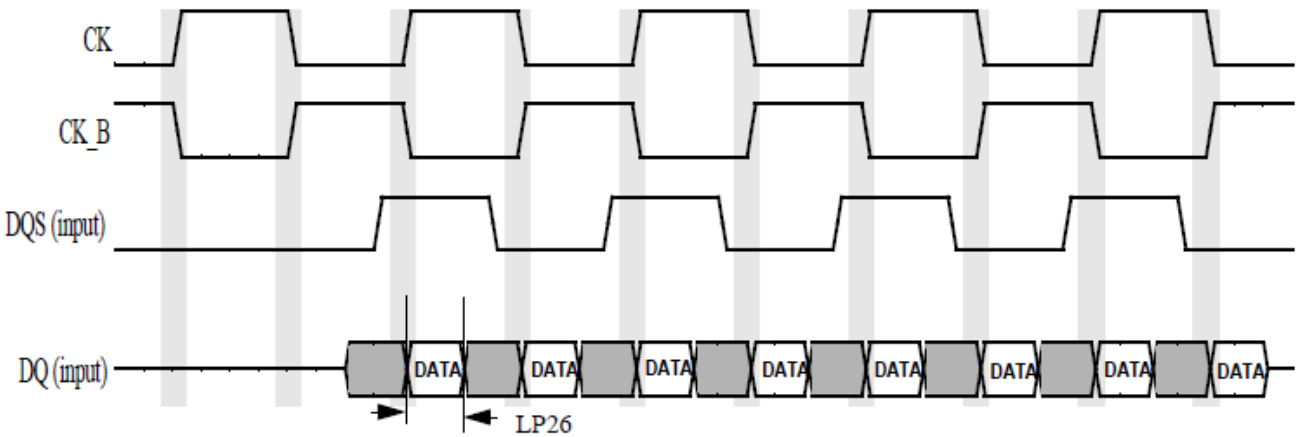

Figure 45. LPDDR2 Read cycle

Table 58. LPDDR2 Read Cycle

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
LP26	Minimum required DQ valid window width for LPDDR2	-	270	-	ps

NOTE

To receive the reported setup and hold values, read calibration should be performed in order to locate the DQS in the middle of DQ window.

NOTE

All measurements are in reference to Vref level.

NOTE

Measurements were done using balanced load and 25 ohms resistor from outputs to VDD_REF

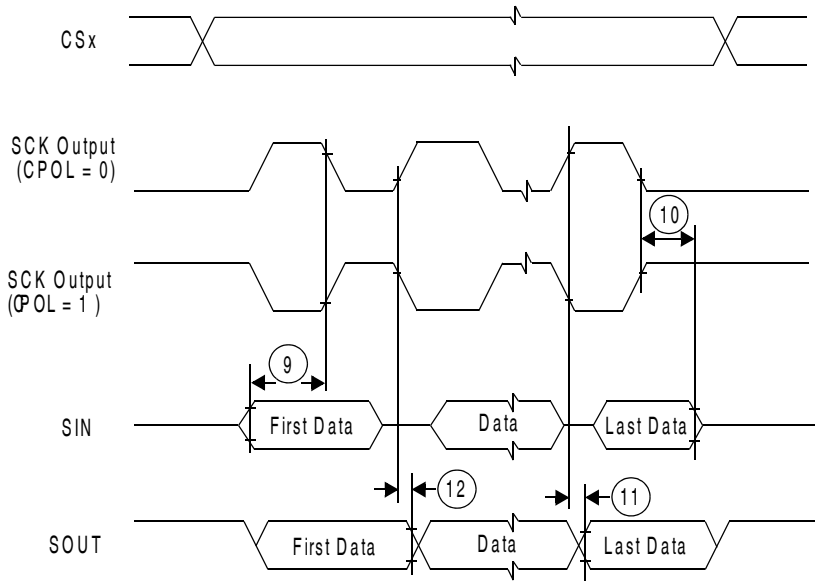

Figure 49. DSPI classic SPI timing master, CPHA=1

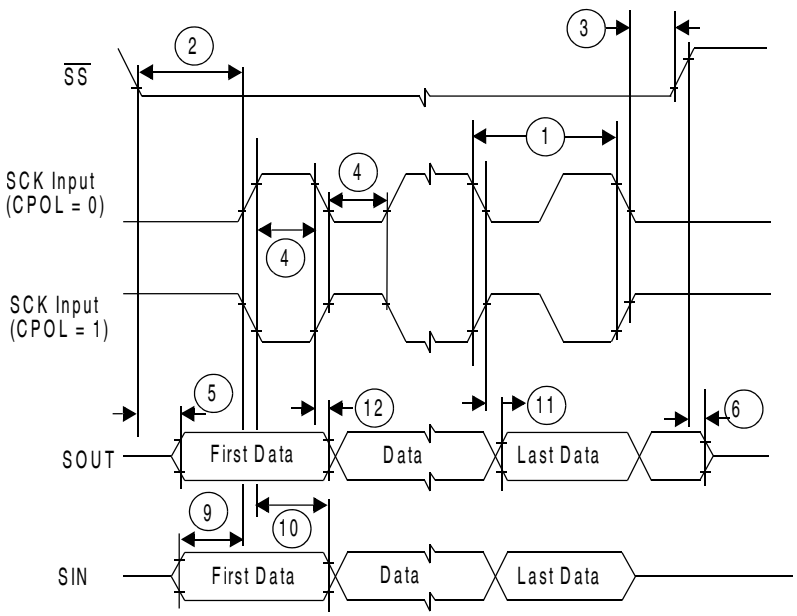

Figure 50. DSPI classic SPI timing slave, CPHA=0

Table 67. 24MHz external oscillator electrical characteristics (continued)

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
C_{IN}	Input Capacitance	EXTAL and XTAL pins	—	9	—	pF
VIH	XTAL pin input high voltage	—	0.8 x Vdd[1]	—	Vdd +0.3	V
VIL	XTAL pin input low voltage	—	Vss -0.3	—	0.2 x Vdd	V

1. V_{DD} =1.1 V ± 10%, TA = -40 to +85 °C, unless otherwise specified.

9.7.2 32 KHz Oscillator Specifications

This block implements an amplifier that when combined with a suitable quartz crystal and external load capacitors implements a low power oscillator. It also implements a power mux such that it can be powered from either a ~3 V backup battery or VDDIO such as the oscillator consumes power from VDDIO when that supply is available and transitions to the back up battery when VDDIO is lost.

In addition, if the clock monitor determines that the OSC32K is not present, then the source of the 32 K will automatically switch to the 128kHz internal RC clock divided by 4.

The OSC32k runs from vdd_rtc supply, generated inside OSC32k itself from VDDIO/ VBAT. The target battery is a ~3 V coin cell. Proper choice of coin cell type is necessary for chosen VDDIO range. Appropriate series resistor (Rs) must be used when connecting the coin cell. Rs depends on the charge current limit that depends on the chosen coin cell.

For example:

- Average Discharge Voltage is 2.5 V
- Maximum Charge Current is 0.6 mA

For a charge voltage of 3.2 V, Rs = (3.2-2.5)/0.6 m = 1.17 k

Table 68. OSC32K Main Characteristics

	Notes	Min	Typ	Max
F_{OSC}	This frequency is nominal and determined mainly by the crystal selected. 32.0 K would work as well.		32.768 KHz	
Current consumption	The 4 µA is the consumption of the oscillator alone (OSC32k). Total supply consumption will depend on what the digital portion of the RTC consumes. The ring oscillator consumes 1 µA when ring oscillator is inactive, 20 µA when the ring		4 µA	

Table continues on the next page...

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
N4	18	PTC8		PTC8	RMII0_TXEN/ MII0_TXEN		SPI1_SCK			VIU_DATA8	DCU0_B1	
T15	—	PTC9		PTC9	RMII1_MDC		ESAI_SCKT			MLBCLK		
U15	—	PTC10		PTC10	RMII1_MDIO		ESAI_FST			MLBSIGNAL		
P4	—	PTC11		PTC11	RMII1_CRS_ DV		ESAI_SDO0			MLBDATA		
P3	—	PTC12		PTC12	RMII1_RXD1		ESAI_SDO1		SAI2_TX_ BCLK			
P1	—	PTC13		PTC13	RMII1_RXD0		ESAI_SDO2/ ESAI_SDI3		SAI2_RX_ BCLK			
R1	—	PTC14		PTC14	RMII1_RXER		ESAI_SDO3/ ESAI_SDI2	SCI5_TX	SAI2_RX_ DATA	ADC0_SE6		
P2	—	PTC15		PTC15	RMII1_TXD1		ESAI_SDO5/ ESAI_SDI0	SCI5_RX	SAI2_TX_ DATA	ADC0_SE7		
R3	—	PTC16		PTC16	RMII1_TXD0		ESAI_SDO4/ ESAI_SDI1	SCI5_RTS	SAI2_RX_ SYNC	ADC1_SE6		
R4	—	PTC17		PTC17	RMII1_TXEN		ADC1_SE7	SCI5_CTS	SAI2_TX_ SYNC	USB1_SOF_ PULSE		
B10	—	DDR_A[15]			DDR_A15							
D9	—	DDR_A[14]			DDR_A14							
A10	—	DDR_A[13]			DDR_A13							
C10	—	DDR_A[12]			DDR_A12							
D10	—	DDR_A[11]			DDR_A11							
D7	—	DDR_A[10]			DDR_A10							
B9	—	DDR_A[9]			DDR_A9							
A11	—	DDR_A[8]			DDR_A8							
A7	—	DDR_A[7]			DDR_A7							
A9	—	DDR_A[6]			DDR_A6							
B6	—	DDR_A[5]			DDR_A5							
A6	—	DDR_A[4]			DDR_A4							
B7	—	DDR_A[3]			DDR_A3							
A8	—	DDR_A[2]			DDR_A2							
C11	—	DDR_A[1]			DDR_A1							
C7	—	DDR_A[0]			DDR_A0							
D8	—	DDR_BA[2]			DDR_BA2							
C9	—	DDR_BA[1]			DDR_BA1							
C8	—	DDR_BA[0]			DDR_BA0							
B4	—	DDR_CAS_b			DDR_CAS_b							
A5	—	DDR_CKE[0]			DDR_CKE0							
A2	—	DDR_CLK[0]			DDR_CLK0							
B2	—	DDR_CLK_ b[0]			DDR_CLK_ b0							

Table 78. RGPIO versus Pins (continued)

RGPIO	In GPIO module	Corresponding Pin on the chip	IOMUX register name	IOMUX register address
RGPIO[1]	PORT0[1]	PTA8	IOMUXC_PTA8	40048004
RGPIO[2]	PORT0[2]	PTA9	IOMUXC_PTA9	40048008
RGPIO[3]	PORT0[3]	PTA10	IOMUXC_PTA10	4004800C
RGPIO[4]	PORT0[4]	PTA11	IOMUXC_PTA11	40048010
RGPIO[5]	PORT0[5]	PTA12	IOMUXC_PTA12	40048014
RGPIO[6]	PORT0[6]	PTA16	IOMUXC_PTA16	40048018
RGPIO[7]	PORT0[7]	PTA17	IOMUXC_PTA17	4004801C
RGPIO[8]	PORT0[8]	PTA18	IOMUXC_PTA18	40048020
RGPIO[9]	PORT0[9]	PTA19	IOMUXC_PTA19	40048024
RGPIO[10]	PORT0[10]	PTA20	IOMUXC_PTA20	40048028
RGPIO[11]	PORT0[11]	PTA21	IOMUXC_PTA21	4004802C
RGPIO[12]	PORT0[12]	PTA22	IOMUXC_PTA22	40048030
RGPIO[13]	PORT0[13]	PTA23	IOMUXC_PTA23	40048034
RGPIO[14]	PORT0[14]	PTA24	IOMUXC_PTA24	40048038
RGPIO[15]	PORT0[15]	PTA25	IOMUXC_PTA25	4004803C
RGPIO[16]	PORT0[16]	PTA26	IOMUXC_PTA26	40048040
RGPIO[17]	PORT0[17]	PTA27	IOMUXC_PTA27	40048044
RGPIO[18]	PORT0[18]	PTA28	IOMUXC_PTA28	40048048
RGPIO[19]	PORT0[19]	PTA29	IOMUXC_PTA29	4004804C
RGPIO[20]	PORT0[20]	PTA30	IOMUXC_PTA30	40048050
RGPIO[21]	PORT0[21]	PTA31	IOMUXC_PTA31	40048054
RGPIO[22]	PORT0[22]	PTB0	IOMUXC_PTB0	40048058
RGPIO[23]	PORT0[23]	PTB1	IOMUXC_PTB1	4004805C
RGPIO[24]	PORT0[24]	PTB2	IOMUXC_PTB2	40048060
RGPIO[25]	PORT0[25]	PTB3	IOMUXC_PTB3	40048064
RGPIO[26]	PORT0[26]	PTB4	IOMUXC_PTB4	40048068
RGPIO[27]	PORT0[27]	PTB5	IOMUXC_PTB5	4004806C
RGPIO[28]	PORT0[28]	PTB6	IOMUXC_PTB6	40048070
RGPIO[29]	PORT0[29]	PTB7	IOMUXC_PTB7	40048074
RGPIO[30]	PORT0[30]	PTB8	IOMUXC_PTB8	40048078
RGPIO[31]	PORT0[31]	PTB9	IOMUXC_PTB9	4004807C
RGPIO[32]	PORT1[0]	PTB10	IOMUXC_PTB10	40048080
RGPIO[33]	PORT1[1]	PTB11	IOMUXC_PTB11	40048084
RGPIO[34]	PORT1[2]	PTB12	IOMUXC_PTB12	40048088
RGPIO[35]	PORT1[3]	PTB13	IOMUXC_PTB13	4004808C
RGPIO[36]	PORT1[4]	PTB14	IOMUXC_PTB14	40048090
RGPIO[37]	PORT1[5]	PTB15	IOMUXC_PTB15	40048094
RGPIO[38]	PORT1[6]	PTB16	IOMUXC_PTB16	40048098
RGPIO[39]	PORT1[7]	PTB17	IOMUXC_PTB17	4004809C

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Table 81. Functional Assignment Pins (continued)

Signal Name	364 MAP BGA	176 LQFP (R-series ONLY)	Power Group	Pad Type	Default Mode (Reset)	Default Function	Input/ Output	Value
DDR_CLK_b[0]	B2	—	SDRAMC_VDD2P5	DDR	—	DDR_CLK_b[0]	—	—
DDR_CS_b[0]	C5	—	SDRAMC_VDD2P5	DDR	—	DDR_CS_b[0]	—	—
DDR_D[0]	F4	—	SDRAMC_VDD2P5	DDR	—	DDR_D[0]	—	—
DDR_D[1]	H3	—	SDRAMC_VDD2P5	DDR	—	DDR_D[1]	—	—
DDR_D[2]	D4	—	SDRAMC_VDD2P5	DDR	—	DDR_D[2]	—	—
DDR_D[3]	G4	—	SDRAMC_VDD2P5	DDR	—	DDR_D[3]	—	—
DDR_D[4]	F3	—	SDRAMC_VDD2P5	DDR	—	DDR_D[4]	—	—
DDR_D[5]	J3	—	SDRAMC_VDD2P5	DDR	—	DDR_D[5]	—	—
DDR_D[6]	C3	—	SDRAMC_VDD2P5	DDR	—	DDR_D[6]	—	—
DDR_D[7]	G3	—	SDRAMC_VDD2P5	DDR	—	DDR_D[7]	—	—
DDR_D[8]	J1	—	SDRAMC_VDD2P5	DDR	—	DDR_D[8]	—	—
DDR_D[9]	D1	—	SDRAMC_VDD2P5	DDR	—	DDR_D[9]	—	—
DDR_D[10]	H1	—	SDRAMC_VDD2P5	DDR	—	DDR_D[10]	—	—
DDR_D[11]	E2	—	SDRAMC_VDD2P5	DDR	—	DDR_D[11]	—	—
DDR_D[12]	G1	—	SDRAMC_VDD2P5	DDR	—	DDR_D[12]	—	—
DDR_D[13]	C1	—	SDRAMC_VDD2P5	DDR	—	DDR_D[13]	—	—
DDR_D[14]	H2	—	SDRAMC_VDD2P5	DDR	—	DDR_D[14]	—	—
DDR_D[15]	D2	—	SDRAMC_VDD2P5	DDR	—	DDR_D[15]	—	—
DDR_DQM[0]	J4	—	SDRAMC_VDD2P5	DDR	—	DDR_DQM[0]	—	—
DDR_DQM[1]	G2	—	SDRAMC_VDD2P5	DDR	—	DDR_DQM[1]	—	—
DDR_DQS[0]	D3	—	SDRAMC_VDD2P5	DDR	—	DDR_DQS[0]	—	—

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15 Revision History

The following table provides a revision history for this document.

Table 82. Revision History

Rev. No.	Date	Substantial Changes
Rev1	12/2011	Initial release
Rev2	02/2012	Updated feature list Updated VREG electrical specifications Updated LDO_1P1, LDO2P5 tables Updated DDR IO parameters Added DDR memory controller parameters Updated Power sequencing table Added Power supply diagram Updated Recommended operating conditions Replaced DryIce Tamper Electrical Specifications with Voltage and temperature monitor electrical specifications Updated VideoADC electricals. Updated VideoADC supply scheme diagram. Added VideoADC supply_decoupling diagram Added QuadSPI DDR mode electrical specifications Updated Fast internal RC oscillator table Updated Slow internal RC oscillator table Updated Pinouts section
Rev3	04/2012	Updated device name throughout the document Minor editorial updates in the feature list Updated VREG electrical specifications Updated LDO electrical specifications Updated Power consumption operating behaviors table Added USB PHY Current Consumption table Updated GPIO parameters Updated DDR parameters

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Table 82. Revision History (continued)

Rev. No.	Date	Substantial Changes
		• Removed Temperature Voltage Monitor section to security RM • Updated VideoADC Specifications table
Rev 5	April 2013	Updated pin muxing table with the following changes: • Added MII0 including M AC0.TXDATA[2], MAC0.TXDATA[3], MAC0.RXDATA[2], MAC0.RXDATA[3] , MAC0.TXERR, MAC0.TXCLK, MAC0.RXCLK, MAC0.COL, MAC0.CRS • Following signals muxed on same RMII0 Pins : MII0_MDC, MII0_MDC, MII0_RXD[1], MII0_RXD[0], MII0_RXER, MII0_TXD[1], MII0_TXD[0], MII0_TXEN • Replaced FB_ALE with FB_MUXED_ALE, FB_CS4_b with FB_MUXED_TSIZ0, FB_TSIZ1 with FB_MUXED_TSIZ1, FB_TBST_b with FB_MUXED_TBST_b, FB_BE0_b with FB_MUXED_BE0_b • Removed RCON18,19,20 • Replaced ESAI_SDO2 with ESAI_SDO2/ESAI_SDI3 Replaced ESAI_SDO3 with ESAI_SDO3/ ESAI_SDI2 Replaced ESAI_SDI0 with ESAI_SDO5/ESAI_SDI0 Replaced ESAI_SDI1 with ESAU_SDO4/ESAI_SDI1 • CKO1 additionally muxed at PAD40
Rev 5	May 2013	In the Features, minor editorial updates Added Part Number Format figure Updated the Fields table as per the device part numbers Added Part Numbers table Added External NPN Ballast section In the LVD Dig Electrical Specs, minimum value of Upper Voltage Threshold and Lower Voltage threshold In the FlexBus timing specifications table, clarified the Frequency of operation In the Power consumption, filled TBDs. Updated footnotes

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Table 82. Revision History (continued)

Rev. No.	Date	Substantial Changes
		• In the USB PHY Current Consumption table, removed the Normal Mode • In the Power Sequence table, revised the Power UP/ Down Order column for USB0_VBUs and USB1_VBUS • In the Recommended operating conditions table, revised the min value of VBAT. Revised the min value of VREFH_ADC Revised the min and max values of SDRAMC_VDD1P5 • In the Recommended Connections for Unused Analog Interfaces section, added the notes. Revised the Recommendation if Unused column • In the 12-bit ADC operating conditions, revised Conditions for Ground voltage. Revised min Ref High Voltage • In the 12-bit DAC operating requirements, revised the min and max value of VREFH_ADC • In the SDHC switching specifications, revised the max value of SD6 • In the 24MHz external oscillator electrical characteristics table, revised the min value of VIH and max value of VIL
Rev 7	November 2014	• Updated list of security features on page 1. • In "Part number format" figure, updated explanation for '1'. • In "Fields" table, updated definition of 'R'. • In "Part Numbers" table, added parts SVF331R3K1CKU2, SVF531R3K1CMK4, and SVF532R2K1CMK4. • In "External NPN ballast" section, updated recommendations for transistor selection. • In "DDR parameters" section, updated table footnotes regarding typical condition. • In "Power sequencing" table, added comment regarding SDRAMC_VDD1P5: "In case the Ballast transistor's collector is connected to the 1.5 V DRAM supply (instead of the 3.3 V