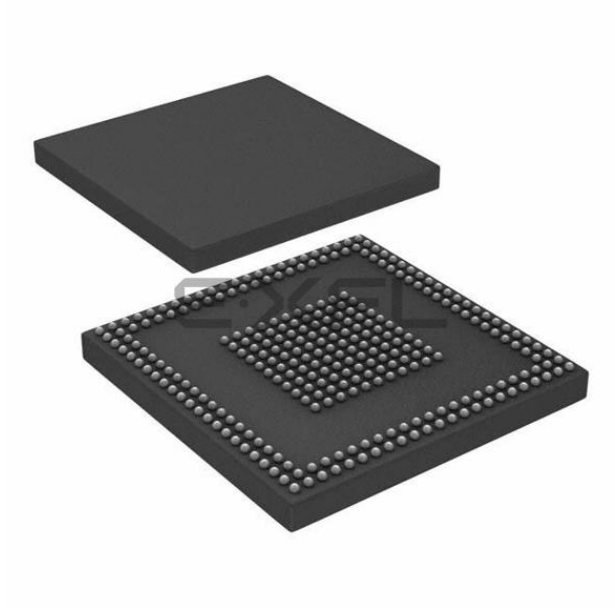

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	DMA, I²C, PPI, SPI, SPORT, UART
Clock Rate	533MHz
Non-Volatile Memory	ROM (32kB)
On-Chip RAM	132kB
Voltage - I/O	1.8V, 2.5V, 3.3V
Voltage - Core	1.10V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	289-LFBGA, CSPBGA
Supplier Device Package	289-CSPBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf523kbcz-5c2

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REVISION HISTORY

3/10—Rev. 0 to Rev. A

Revised the following figures.
Recommended Application Circuit Using SPI Control 13
Recommended Application Circuit Using TWI Control .. 14

Added Sampling Rate = 48 kHz to all figures in
Converter Filter Response 30

Revised Ordering Guide 36

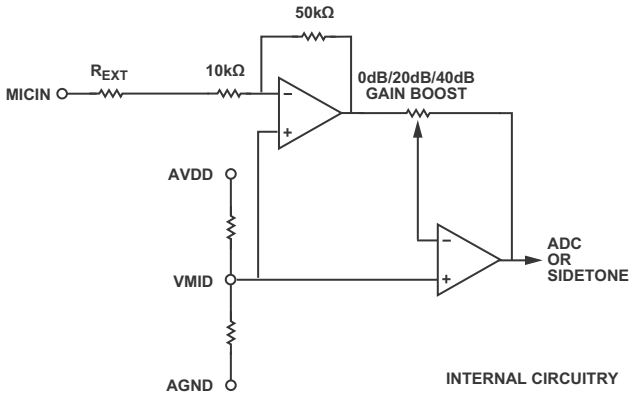

Figure 3. Microphone Input to ADC

The first gain stage is composed of a low noise operational amplifier set to an inverting configuration with integrated 50 kΩ feedback and 10 kΩ input resistors. The default microphone input signal gain is 14 dB. An external resistor (R_{EXT}) can be connected in series with the MICIN pin to reduce the first-stage gain of the microphone input signal to as low as 0 dB by using the following equation:

Microphone Input Gain = 50 kΩ/(10 kΩ + R_{EXT})

The second-stage gain of the microphone signal path is derived from the internal microphone boost circuitry. The available settings are 0 dB, 20 dB, and 40 dB and are controlled by the MICBOOST (Register R4, Bit D0) and MICBOOST2 (Register R4, Bit D8) bits. To achieve 20 dB of secondary gain boost, the programmer can select either MICBOOST or MICBOOST2. To achieve 40 dB of secondary microphone signal gain, the programmer must select both MICBOOST and MICBOOST2.

The MUTEMIC bit (Register R4, Bit D1) mutes the microphone input signal to the ADC.

When using either the line or microphone inputs, the maximum full-scale input to the ADC is 1.0 V rms when AVDD = 3.3 V. Do not apply an input voltage larger than full-scale to avoid overloading the ADC, which causes distortion of sound and deterioration of audio quality. For best sound quality in both microphone and line inputs, gain should be carefully configured so that the ADC receives a signal equal to its full-scale. This maximizes the signal-to-noise ratio for best total audio quality.

Bypass and Sidetone Paths to Output

The line and microphone inputs can be routed and mixed directly to the output terminals by programming the SIDETONE (Register R4, Bit D5) and BYPASS (Register R4, Bit D3) registers. In both modes, the analog input signal is routed directly to the output terminals and is not digitally converted. The bypass signal at the output mixer is the same level as the output of the PGA associated with each line input.

The sidetone signal at the output mixer can be attenuated from –6 dB to –15 dB in steps of –3 dB by configuring the SIDEATT (Register R4, Bit D6 and Bit D7) control register bits. The selected level of attenuation occurs after the initial microphone signal amplification from the microphone first and second stage gains.

Line and Headphone Outputs

The DAC outputs, the microphone (the sidetone path), and the line inputs (the bypass path) are summed at an output mixer (see Figure 4). This output signal is then applied to both the stereo line outputs and stereo headphone outputs.

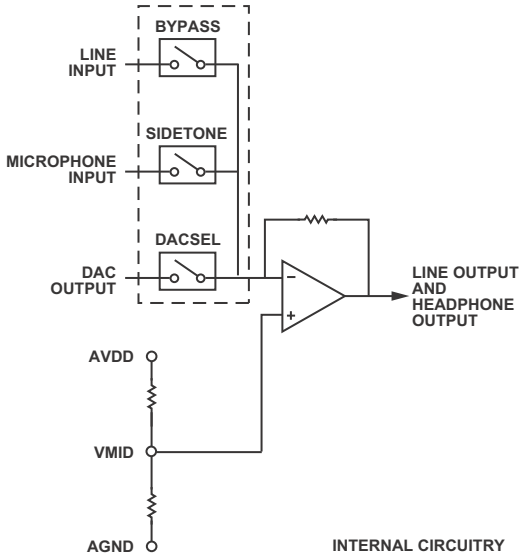

Figure 4. Output Signal Chain

The codec has a set of efficient headphone amplifier outputs, LHPOUT and RHPOUT, that are able to drive 16 Ω or 32 Ω headphones (shown in Figure 5).

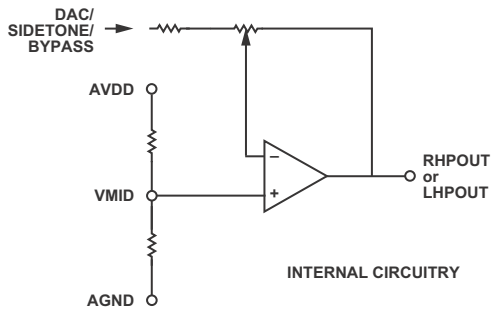

Figure 5. Headphone Output

Like the line inputs, the LHPOUT and RHPOUT volumes, by default, are independently adjusted by setting the LHPVOL (Register R2, Bit D0 to Bit D6) and RHPVOL (Register R3, Bit D0 to Bit D6) bits of the headphone output control registers. The headphone outputs can be muted by writing codes less than 0110000 to the LHPVOL and RHPVOL bits.

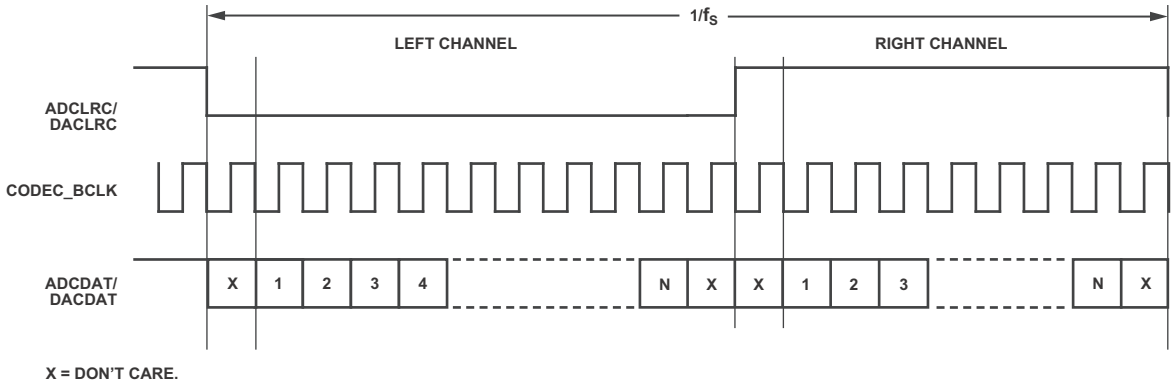

Figure 8. I²S Audio Input Mode

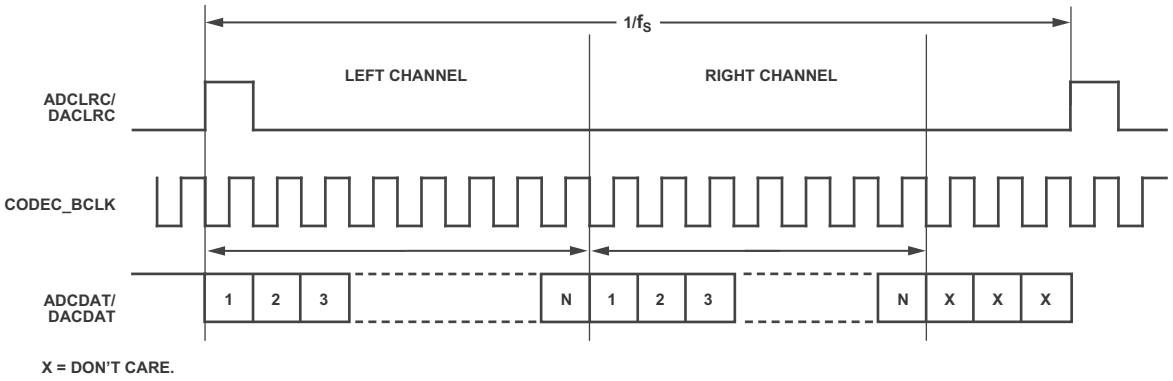

Figure 9. Frame Sync/PCM Mode Audio Input (Submode 1) [Bit LRP = 0]

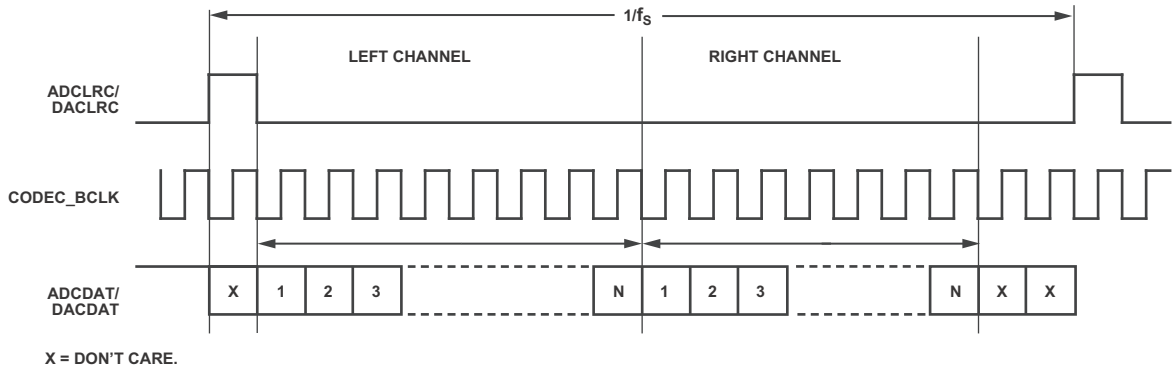

Figure 10. Frame Sync/PCM Mode Audio Input (Submode 2) [Bit LRP = 1]

Normal Mode

In normal mode, the codec supports digital audio sampling rates from 8 kHz to 96 kHz. Normal mode supports 256 × f_S and 384 × f_S based clocks. To select the desired sampling rate, the programmer must set the appropriate sampling rate register in the SR control bits (Register R8, Bit D2 to Bit D5) and match this selection to the core clock frequency that is pulsed on the CODEC_MCLK pin. See Table 1 for sampling rates in normal mode.

Table 1. Sampling Rate Lookup Table, Normal Mode (USB Disabled)

CODEC_MCLK (CLKDIV2 = 0)	CODEC_MCLK (CLKDIV2 = 1)	ADC Sampling Rate (ADCLRC)	DAC Sampling Rate (DACLRC)	USB	SR [3:0]	BOSR	CODEC_BCLK (MS = 1)[1]
12.288 MHz	24.576 MHz	8 kHz (CODEC_MCLK/1536)	8 kHz (CODEC_MCLK/1536)	0	0011	0	CODEC_MCLK/4
		8 kHz (CODEC_MCLK/1536)	48 kHz (CODEC_MCLK/256)	0	0010	0	CODEC_MCLK/4
		12 kHz (CODEC_MCLK/1024)	12 kHz (CODEC_MCLK/1024)	0	0100	0	CODEC_MCLK/4
		16 kHz (CODEC_MCLK/768)	16 kHz (CODEC_MCLK/768)	0	0101	0	CODEC_MCLK/4
		24 kHz (CODEC_MCLK/512)	24 kHz (CODEC_MCLK/512)	0	1110	0	CODEC_MCLK/4
		32 kHz (CODEC_MCLK/384)	32 kHz (CODEC_MCLK/384)	0	0110	0	CODEC_MCLK/4
		48 kHz (CODEC_MCLK/256)	8 kHz (CODEC_MCLK/1536)	0	0001	0	CODEC_MCLK/4
		48 kHz (CODEC_MCLK/256)	48 kHz (CODEC_MCLK/256)	0	0000	0	CODEC_MCLK/4
		96 kHz (CODEC_MCLK/128)	96 kHz (CODEC_MCLK/128)	0	0111	0	CODEC_MCLK/2
11.2896 MHz	22.5792 MHz	8.0182 kHz (CODEC_MCLK/1408)	8.0182 kHz (CODEC_MCLK/1408)	0	1011	0	CODEC_MCLK/4
		8.0182 kHz (CODEC_MCLK/1408)	44.1 kHz (CODEC_MCLK/256)	0	1010	0	CODEC_MCLK/4
		11.025 kHz (CODEC_MCLK/1024)	11.025 kHz (CODEC_MCLK/1024)	0	1100	0	CODEC_MCLK/4
		22.05 kHz (CODEC_MCLK/512)	22.05 kHz (CODEC_MCLK/512)	0	1101	0	CODEC_MCLK/4
		44.1 kHz (CODEC_MCLK/256)	8.0182 kHz (CODEC_MCLK/1408)	0	1001	0	CODEC_MCLK/4
		44.1 kHz (CODEC_MCLK/256)	44.1 kHz (CODEC_MCLK/256)	0	1000	0	CODEC_MCLK/4
		88.2 kHz (CODEC_MCLK/128)	88.2 kHz (CODEC_MCLK/128)	0	1111	0	CODEC_MCLK/2
18.432 MHz	36.864 MHz	8 kHz (CODEC_MCLK/2304)	8 kHz (CODEC_MCLK/2304)	0	0011	1	CODEC_MCLK/6
		8 kHz (CODEC_MCLK/2304)	48 kHz (CODEC_MCLK/384)	0	0010	1	CODEC_MCLK/6
		12 kHz (CODEC_MCLK/1536)	12 kHz (CODEC_MCLK/1536)	0	0100	1	CODEC_MCLK/6
		16 kHz (CODEC_MCLK/1152)	16 kHz (CODEC_MCLK/1152)	0	0101	1	CODEC_MCLK/6
		24 kHz (CODEC_MCLK/768)	24 kHz (CODEC_MCLK/768)	0	1110	1	CODEC_MCLK/6
		32 kHz (CODEC_MCLK/576)	32 kHz (CODEC_MCLK/576)	0	0110	1	CODEC_MCLK/6
		48 kHz (CODEC_MCLK/384)	48 kHz (CODEC_MCLK/384)	0	0000	1	CODEC_MCLK/6
		48 kHz (CODEC_MCLK/384)	8 kHz (CODEC_MCLK/2304)	0	0001	1	CODEC_MCLK/6
		96 kHz (CODEC_MCLK/192)	96 kHz (CODEC_MCLK/192)	0	0111	1	CODEC_MCLK/3
16.9344 MHz	33.8688 MHz	8.0182 kHz (CODEC_MCLK/2112)	8.0182 kHz (CODEC_MCLK/2112)	0	1011	1	CODEC_MCLK/6
		8.0182 kHz (CODEC_MCLK/2112)	44.1 kHz (CODEC_MCLK/384)	0	1010	1	CODEC_MCLK/6
		11.025 kHz (CODEC_MCLK/1536)	11.025 kHz (CODEC_MCLK/1536)	0	1100	1	CODEC_MCLK/6
		22.05 kHz (CODEC_MCLK/768)	22.05 kHz (CODEC_MCLK/768)	0	1101	1	CODEC_MCLK/6
		44.1 kHz (CODEC_MCLK/384)	8.0182 kHz (CODEC_MCLK/2112)	0	1001	1	CODEC_MCLK/6
		44.1 kHz (CODEC_MCLK/384)	44.1 kHz (CODEC_MCLK/384)	0	1000	1	CODEC_MCLK/6
		88.2 kHz (CODEC_MCLK/192)	88.2 kHz (CODEC_MCLK/192)	0	1111	1	CODEC_MCLK/3

[1] CODEC_BCLK frequency is for master mode and slave right-justified mode only.

Figure 14 on Page 13 and Figure 15 on Page 14 describe alternative external connections for SPI or TWI control of the ADSP-BF52xC codec. The figures are the same except for the shaded area in each.

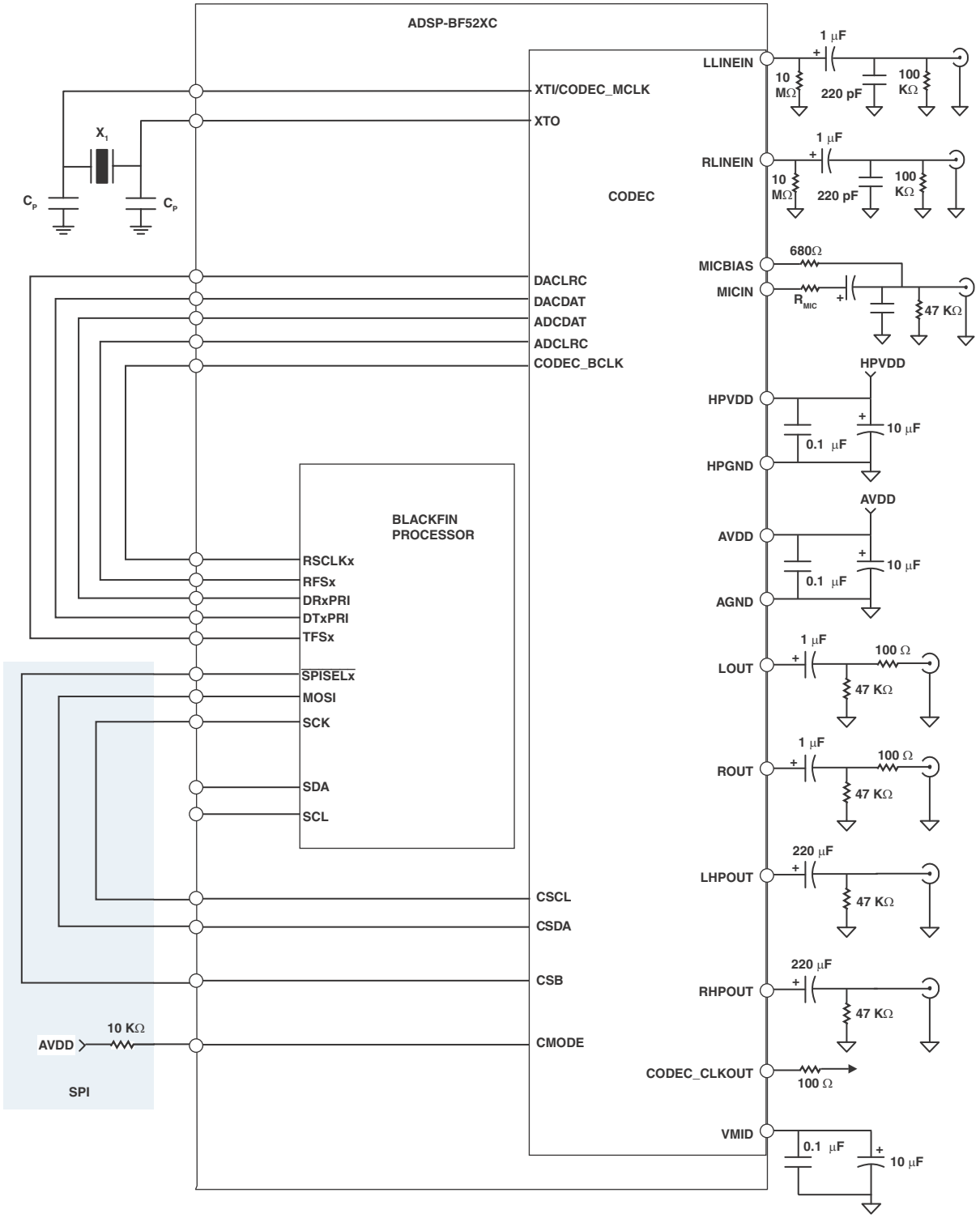

Figure 14. Recommended Application Circuit Using SPI Control

REGISTER DETAILS

Register	Address	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 0 Left-Channel ADC Input Volume on Page 16	0x00	LRINBOTH	LINMUTE	0	LINVOL					
		Default = 010010111								
Register 1 Right-Channel ADC Input Volume on Page 17	0x01	RLINBOTH	RINMUTE	0	RINVOL					
		Default = 010010111								
Register 2 Left-Channel DAC Volume on Page 17	0x02	LRHPBOTH	LZCEN	LHPVOL						
		Default = 001111001								
Register 3 Right-Channel DAC Volume on Page 18	0x03	RLHPBOTH	RZCEN	RHPVOL						
		Default = 001111001								
Register 4 Analog Audio Path on Page 18	0x04	MICBOOST2	SIDEATT[1:0]		SIDETONE	DACSEL	BYPASS	INSEL	MUTEMIC	MICBOOST
		Default = 000001010								
Register 5 Digital Audio Path on Page 19	0x05	0	0	0	0	HPOR	DACMU	DEEMPH[1:0]		ADC HPD
		Default = 000001000								
Register 6 Power Management on Page 19	0x06	0	POWEROFF	CLKOUTPD	OSCPD	OUTPD	DACPD	ADCPD	MICPD	LINEINPD
		Default = 010011111								
Register 7 Digital Audio I/F on Page 20	0x07	0	BCLKINV	MS	LRSWAP	LRP	WL[1:0]		FORMAT[1:0]	
		Default = 000001010								
Register 8 Sampling Rate on Page 20	0x08	0	CLKODIV2	CLKDIV2	SR[3:0]				BOSR	USB
		Default = 000000000								
Register 9 Active on Page 20	0x09	0	0	0	0	0	0	0	0	ACTIVE
		Default = 000000000								
Register 10 Software Reset on Page 20	0x0F	RESET								
		Default = 000000000								

Figure 16. Register Mapping

Table 5. Register 1 Right-Channel ADC Input Volume

Bit Name	Bits	Description	Settings
RLINBOTH	B8	Right-to-left line input ADC data load control	0 = disable simultaneous loading of right-channel ADC data to left-channel register (default)
			1 = enable simultaneous loading of right-channel ADC data to left-channel register
RINMUTE	B7	Right-channel input mute	0 = disable mute
			1 = enable mute on data path to ADC (default)
RINVOL	B[5:0]	Right-channel PGA volume control	00 0000 = –34.5 dB
			… 1.5 dB step up
			01 0111 = 0 dB (default)
			… 1.5 dB step up
			01 1111 = 12 dB
			10 0000 = 13.5 dB
			10 0001 = 15 dB
			10 0010 = 16.5 dB
			10 0011 = 18 dB
			10 0100 = 19.5 dB
			10 0101 = 21 dB
			10 0110 = 22.5 dB
			10 0111 = 24 dB
			10 1000 = 25.5 dB
			10 1001 = 27 dB
			10 1010 = 28.5 dB
			10 1011 = 30 dB
			10 1100 = 31.5 dB
			10 1101 = 33 dB
			11 1111 to 10 1101 = 33 dB

Table 6. Register 2 Left-Channel DAC Volume

Bit Name	Bits	Description	Settings
LRHPBOTH	B8	Left-to-right headphone volume load control	0 = disable simultaneous loading of left-channel headphone volume data to right-channel register (default)
			1 = enable simultaneous loading of left-channel headphone volume data to right-channel register
LZCEN	B7	Left-channel zero cross detect enable	0 = disable (default) 1 = enable
LHPVOL	B[6:0]	Left-channel headphone volume control	000 0000 to 010 1111 = mute
			011 0000 = –73 dB
			…
			111 1001 = 0 dB (default)
			… 1 dB steps up to
			111 1111 = +6 dB

Table 7. Register 3 Right-Channel DAC Volume

Bit Name	Bits	Description	Settings
RLHPBOTH	B8	Right-to-left headphone volume load control	0 = disable simultaneous loading of right-channel headphone volume data to left-channel register (default) 1 = enable simultaneous loading of right-channel headphone volume data to left-channel register
RZCEN	B7	Right-channel zero cross detect enable	0 = disable (default) 1 = enable
RHPVOL [6:0]	B[6:0]	Right-channel headphone volume control	000 0000 to 010 1111 = mute 011 0000 = –73 dB … 111 1001 = 0 dB (default) … 1 dB steps up to 111 1111 = +6 dB

Table 8. Register 4 Analog Audio Path

Bit Name	Bits	Description	Settings
MICBOOST2	B8	Additional microphone amplifier gain booster control	0 = 0 dB (default) 1 = 20 dB
SIDEATT[1:0]	B[7:6]	Microphone sidetone gain control	00 = –6 dB (default) 01 = –9 dB 10 = –12 dB 11 = –15 dB
SIDETONE	B5	Sidetone enable. Allow attenuated microphone signal to be mixed at device output terminal	0 = sidetone disable (default) 1 = sidetone enable
DACSEL	B4	DAC select—allow DAC output to be mixed at device output terminal	0 = do not select DAC (default) 1 = select DAC
BYPASS	B3	Bypass select—allow line input signal to be mixed at device output terminal	0 = bypass disable 1 = bypass enable (default)
INSEL	B2	Line input or microphone input select to ADC	0 = line input select to ADC (default) 1 = microphone input select to ADC
MUTEMIC	B1	Microphone mute control to ADC	0 = mute on data path to ADC disable 1 = mute on data path to ADC enable (default)
MICBOOST	B0	Primary microphone amplifier gain booster control	0 = 0 dB (default) 1 = 20 dB

Table 9. Register 5 Digital Audio Path

Bit Name	Bits	Description	Settings
HPOR	B4	Store dc offset when high-pass filter is disabled	0 = clear offset (default)
			1 = store offset
DACMU	B3	DAC digital mute	0 = no mute (signal active)
			1 = mute (default)
DEEMPH[1:0]	B[2:1]	De-emphasis control	00 = no de-emphasis (default)
			01 = 32 kHz sampling rate
			10 = 44.1 kHz sampling rate
			11 = 48 kHz sampling rate
ADCHPD	B0	ADC high-pass filter control	0 = ADC high-pass filter enable (default)
			1 = ADC high-pass filter disable

Table 10. Register 6 Power Management

Bit Name	Bits	Description	Settings
POWEROFF	B7	Whole chip power-down control	0 = power-up
			1 = power-down (default)
CLKOUTPD	B6	Clock output power-down control	0 = power-up (default)
			1 = power-down
OSCPD	B5	Crystal power-down control	0 = power-up (default)
			1 = power-down
OUTPD	B4	Output power-down control	0 = power-up
			1 = power-down (default)
DACPD	B3	DAC power-down control	0 = power-up
			1 = power-down (default)
ADCPD	B2	ADC power-down control	0 = power-up
			1 = power-down (default)
MICPD	B1	Microphone input power-down control	0 = power-up
			1 = power-down (default)
LINEINPD	B0	Line input power-down control	0 = power-up
			1 = power-down (default)

Table 11. Register 7 Digital Audio I/F

Bit Name	Bits	Description	Settings
BCLKINV	B7	CODEC_BCLK inversion control	0 = CODEC_BCLK not inverted (default)
			1 = CODEC_BCLK inverted
MS	B6	Master mode enable	0 = enable slave mode (default)
			1 = enable master mode
LRSWAP	B5	Swap DAC data control	0 = output left- and right-channel data as normal (default)
			1 = swap left- and right-channel DAC data in audio interface
LRP	B4	Polarity control for clocks in right-justified, left-justified, and I^2S modes	0 = normal DACLRC and ADCLRC (default), or processor Submode 1
			1 = invert DACLRC and ADCLRC polarity, or processor Submode 2
WL [1:0]	B[3:2]	Data-word length control	00 = 16 bits
			01 = 20 bits
			10 = 24 bits (default)
			11 = 32 bits
FORMAT [1:0]	B[1:0]	Digital audio input format control	00 = right justified
			01 = left justified
			10 = I^2S mode (default)
			11 = processor mode

Table 12. Register 8 Sampling Rate

Bit Name	Bits	Description	Settings
CLKODIV2	B7	CODEC_CLKOUT divider select	0 = CODEC_CLKOUT is codec clock (default)
			1 = CODEC_CLKOUT is codec clock divided by 2
CLKDIV2	B6	Codec clock divide select	0 = codec clock is CODEC_MCLK (default)
			1= codec clock is CODEC_MCLK divided by 2
SR [3:0]	B[5:2]	Clock setting condition	See Table 1 on Page 9 and Table 2 on Page 10
BOSR	B1	Base oversampling rate	USB mode:
			0 = support for 250 × f_S based clock (default)
			1 = support for 272 × f_S based clock
			Normal mode:
			0 = support for 256 × f_S based clock (default)
			1 = support for 384 × f_S based clock
USB	B0	USB mode select	0 = normal mode enable (default)
			1 = USB mode enable

Table 13. Register 9 Active

Bit Name	Bit	Description	Settings
ACTIVE	B0	Digital core activation control	0 = disable digital core (default)
			1 = activate digital core

Table 14. Register 10 Software Reset

Bit Name	Bit	Description	Settings
RESET [8:0]	B[8:0]	Write all 0s to this register to set all registers to their default settings. Other data written to this register has no effect.	0 = reset (default)

POWER CONSUMPTION

These current consumption values are for the codec alone. Please refer to the published ADSP-BF52x processor data sheet for the additional current consumption of the Blackfin processor.

Table 16. Power Consumption

Mode	POWEROFF	CLKOUTPD	OSCPD	OUTPD	DACPD	ADCPD	MICPD	LINEINPD	(1.8V) AVDD	(1.8V) HPVDD	(1.8V) V_{DDEXT}[1]	(3.3V) AVDD	(3.3V) HPVDD	(3.3V) V_{DDEXT}[1]	Unit
Record and Playback	0	0	0	0	0	0	0	0	7.4	1.5	6.3	14.8	2.0	12.0	mA
Playback Only															
Oscillator Enabled	0	0	0	0	0	1	1	1	3.1	1.30	3.0	4.7	2.0	6.1	mA
External Clock	0	1	1	0	0	1	1	1	2.9	1.2	3.0	4.7	2.0	6.1	mA
Record Only															
Line Oscillator	0	0	0	1	1	0	1	0	2.4	N/A	3.7	4.3	N/A	7.4	mA
Line Clock	0	0	1	1	1	0	1	0	2.5	N/A	3.8	4.3	N/A	7.4	mA
Microphone 1	0	0	0	1	1	0	0	1	3.6	N/A	1.9	9.4	N/A	3.6	mA
Microphone 2	0	0	1	1	1	0	0	1	3.6	N/A	1.8	9.4	N/A	3.6	mA
Sidetone (Microphone-to-Headphone Output)															
Internally Generated Clock	0	0	0	0	1	1	0	1	2.3	1.0	2.0	7.9	2.0	4.0	mA
External Clock	0	0	1	0	1	1	0	1	2.3	1.0	2.0	7.9	2.0	4.0	mA
Analog Bypass (Line Input or Line Output)															
Internally Generated Line	0	0	0	0	1	1	1	0	0.9	1.0	2.0	1.8	2.0	4.0	mA
External Line	0	0	1	0	1	1	1	0	0.9	1.0	2.0	1.8	2.0	4.0	mA
Power-Down															
Clock Stopped	1	1	1	1	1	1	1	1	3.1	6.3	3.8	9.4	6.3	12.3	µA

[1] V_{DDEXT} here refers to the total of the codec's DCVDD and DBVDD signals and does not include VDDExt supplies in the Blackfin device.

TIMING SPECIFICATIONS

TWI Timing

Table 17. TWI Timing

Parameter		Test Conditions[1]	Min	Max	Unit
t_{SCS}	Start condition setup time		600		ns
t_{SCH}	Start condition hold time		600		ns
t_{PH}	CSCL pulse width high		600		ns
t_{PL}	CSCL pulse width low		1.3		µs
f_{SCL}	CSCL frequency		0	526	kHz
t_{DS}	Data setup time		100		ns
t_{DH}	Data hold time			900	ns
t_{RT}	CSDA and CSCL rise time			300	ns
t_{FT}	CSDA and CSCL fall time			300	ns
t_{HCS}	Stop condition setup time		600		ns

[1] AVDD, HPVDD, V_{DDEXT} = 3.3 V, AGND = 0 V, T_A = +25°C, Slave Mode, f_S = 48 kHz, XTI/CODEC_MCLK = 256 × f_S unless otherwise stated.

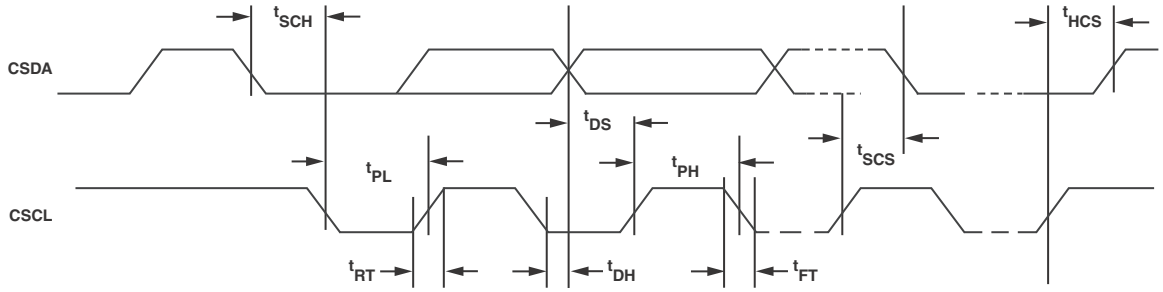

Figure 18. TWI Timing

SPI Timing

Table 18. SPI Timing

Parameter		Test Conditions[1]	Min	Max	Unit
t_{DSU}	CSDA to CSCL setup time		20		ns
t_{DHO}	CSCL to CSDA hold time		20		ns
t_{SCH}	CSCL pulse width high		20		ns
t_{SCL}	CSCL pulse width low		20		ns
t_{SCS}	CSCL rising edge to CSB rising edge		60		ns
t_{CSS}	CSB rising to CSCL rising		20		ns
t_{CSH}	CSB pulse width high		20		ns
t_{CSL}	CSB pulse width low		20		ns
t_{PS}	Pulse width of spikes to be suppressed		0	5	ns

[1] AVDD, HPVDD, V_{DDEXT} = 3.3 V, AGND = 0 V, T_A = +25°C, Slave Mode, f_S = 48 kHz, XTI/CODEC_MCLK = 256 × f_S unless otherwise stated.

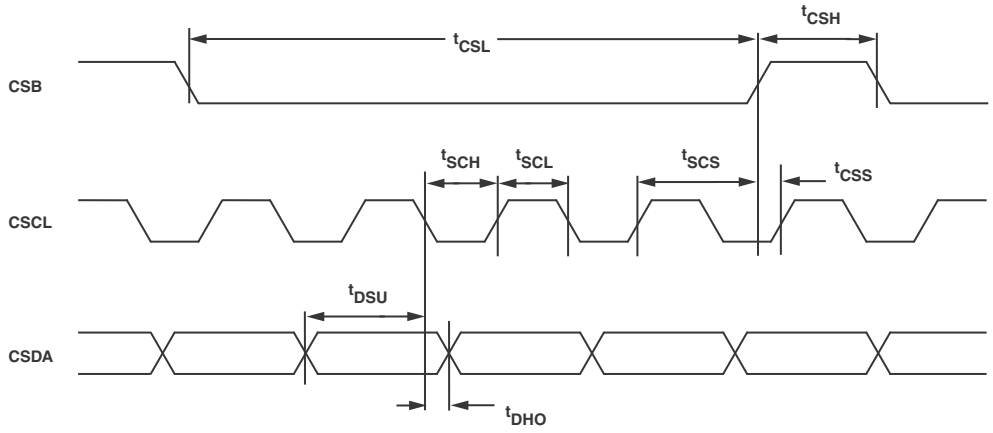

Figure 19. SPI Timing

Digital Audio Interface Slave Mode Timing

Table 19. Digital Audio Interface Slave Mode Timing

Parameter		Test Conditions[1]	Min	Max	Unit
t_{DS}	DACDAT setup time from CODEC_BCLK rising edge		10		ns
t_{DH}	DACDAT hold time from CODEC_BCLK rising edge		10		ns
t_{LRSU}	ADCLRC/DACLRC setup time to CODEC_BCLK rising edge		10		ns
t_{LRH}	ADCLRC/DACLRC hold time to CODEC_BCLK rising edge		10		ns
t_{DD}	ADCDAT propagation delay from CODEC_BCLK falling edge (external load of 70 pF)			30	ns
t_{BCH}	CODEC_BCLK pulse width high		25		ns
t_{BCL}	CODEC_BCLK pulse width low		25		ns
t_{BCY}	CODEC_BCLK cycle time		50		ns

[1] AVDD, HPVDD, V_{DDEXT} = 3.3 V, AGND = 0 V, T_A = +25°C, Slave Mode, f_S = 48 kHz, XTI/CODEC_MCLK = 256 × f_S unless otherwise stated.

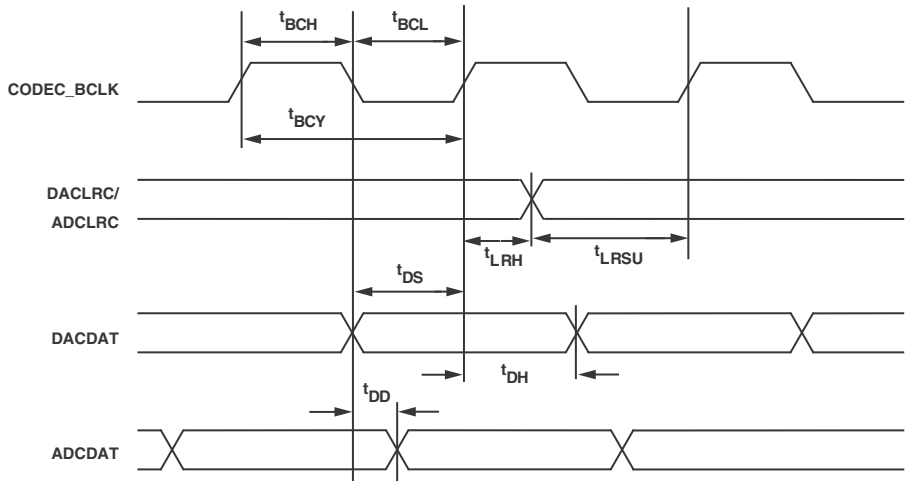

Figure 20. Digital Audio Interface Slave Mode Timing

Digital Audio Interface Master Mode Timing

Table 20. Digital Audio Interface Master Mode Timing

Parameter		Test Conditions[1]	Min	Max	Unit
t_{DST}	DACDAT setup time to CODEC_BCLK rising edge		30		ns
t_{DHT}	DACDAT hold time to CODEC_BCLK rising edge		10		ns
t_{DL}	ADCLRC/DACLRC propagation delay from CODEC_BCLK falling edge			10	ns
t_{DDA}	ADCDAT propagation delay from CODEC_BCLK falling edge			10	ns
t_{BCLKR}	CODEC_BCLK rising time (10 pF load)		10		ns
t_{BCLKF}	CODEC_BCLK falling time (10 pF load)		10		ns
t_{BCLKDS}	CODEC_BCLK duty cycle (normal and USB mode)		45:55	55:45	

[1] AVDD, HPVDD, V_{DDEXT} = 3.3 V, AGND = 0 V, T_A = +25°C, Slave Mode, f_S = 48 kHz, XTI/CODEC_MCLK = 256 × f_S unless otherwise stated.

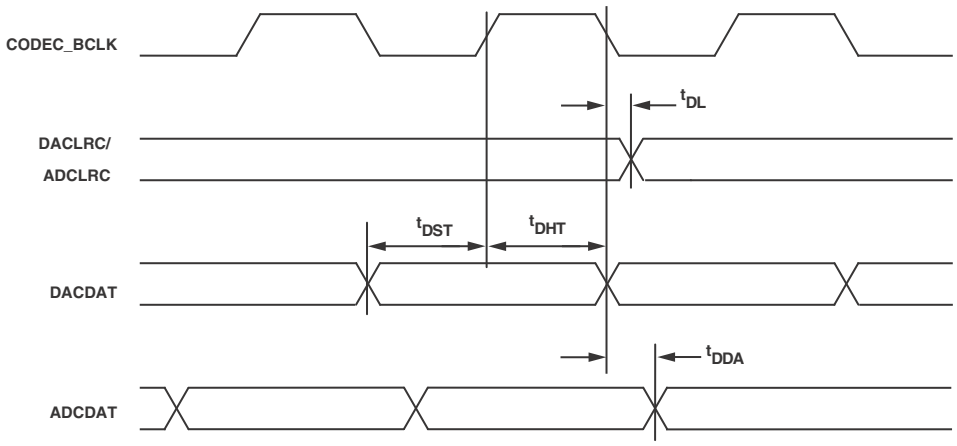

Figure 21. Digital Audio Interface Master Mode Timing

System Clock Timing

Table 21. System Clock Timing

Parameter		Test Conditions[1]	Min	Max	Unit
t_{XTIY}	XTI/CODEC_MCLK system clock cycle time		72		ns
t_{MCLKDS}	XTI/CODEC_MCLK duty cycle		40:60	60:40	
t_{XTIH}	XTI/CODEC_MCLK system clock pulse width high		32		ns
t_{XTIL}	XTI/CODEC_MCLK system clock pulse width low		32		ns
t_{COP}	CODEC_CLKOUT propagation delay from XTI/CODEC_MCLK falling edge		20		ns
$t_{COPDIV2}$	CLKODIV2 propagation delay from XTI/CODEC_MCLK falling edge		20		ns

[1] AVDD, HPVDD, V_{DDEXT} = 3.3 V, AGND = 0 V, T_A = +25°C, Slave Mode, f_S = 48 kHz, XTI/CODEC_MCLK = 256 × f_S unless otherwise stated.

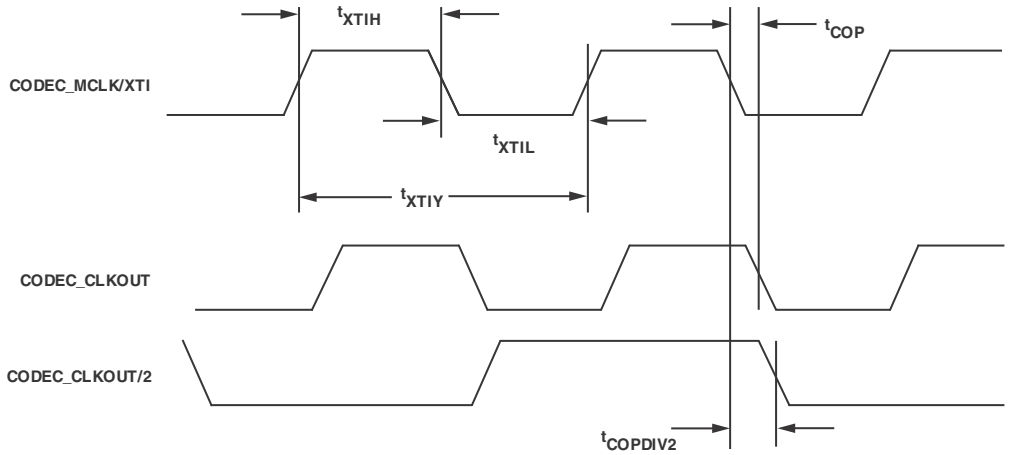

Figure 22. System (CODEC_MCLK) Clock Timing

Digital Filter Characteristics

Table 22. Digital Filter Characteristics

Parameter	Conditions	Min	Typical	Max	Unit
ADC FILTER					
Pass Band	±0.04 dB	0		$0.445 \times f_S$	Hz
	–6 dB		$0.5 \times f_S$		Hz
Pass Band Ripple				±0.04	dB
Stop Band		$0.555 \times f_S$			Hz
Stop Band Attenuation	$f > 0.567 \times f_S$	–61			dB
High-Pass Filter Corner Frequency	–3 dB		3.7		Hz
	–0.5 dB		10.4		Hz
	–0.1 dB		21.6		Hz
DAC FILTER					
Pass Band	±0.04 dB	0		$0.445 \times f_S$	Hz
	–6 dB		$0.5 \times f_S$		Hz
Pass Band Ripple				±0.04	dB
Stop Band		$0.555 \times f_S$			Hz
Stop Band Attenuation	$f > 0.565 \times f_S$	–61			dB
Codec Clock Tolerance					
Frequency Range		8.0		13.8	MHz
Jitter Tolerance			50		pS

CONVERTER FILTER RESPONSE

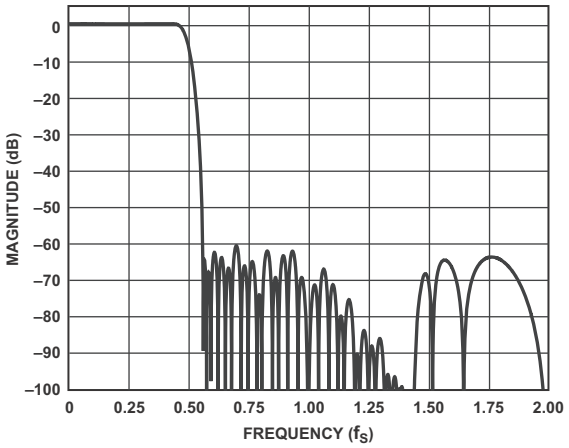

Figure 23. ADC Digital Filter Frequency Response, Sampling Rate = 48 kHz

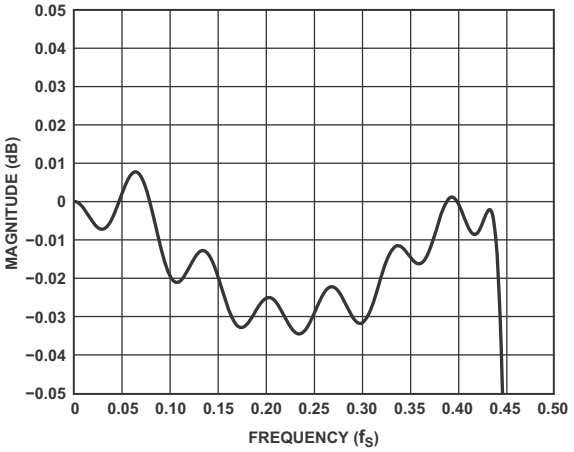

Figure 24. ADC Digital Filter Ripple, Sampling Rate = 48 kHz

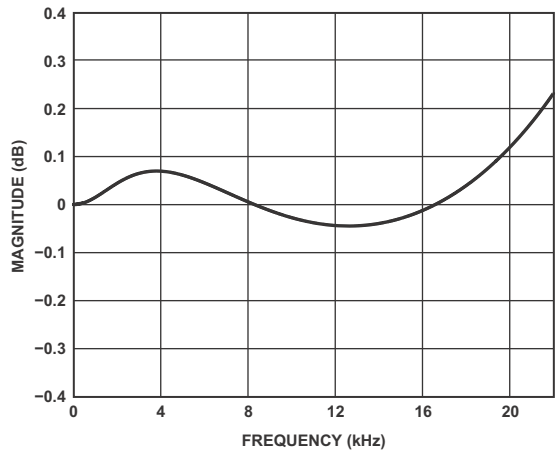

Figure 31. De-Emphasis Error, Sampling Rate = 44.1 kHz

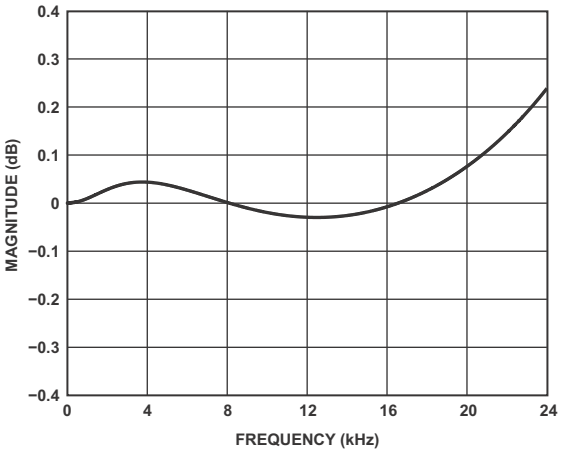

Figure 32. De-Emphasis Error, Sampling Rate = 48 kHz

289-BALL CSP_BGA BALL ASSIGNMENT

Signals added or changed to the ADSP-BF52xC processor for the embedded codec are shown in Table 23 and Table 24. Please refer to the published ADSP-BF52x processor data sheet for descriptions of additional signals for the processor.

Table 23. 289-Ball CSP_BGA Ball Assignment (Alphabetically)

Signal	Ball No.	Signal	Ball No.
ADCDAT	A16	HPGND	G17
ADCLRC	A15	HPVDD	G16[1]
AGND	H22	LHPOUT	B20
AVDD	J22[1]	LLINEIN	E23
CMODE	E22	LOUT	F22
CODEC_BCLK	A19	MICBIAS	H23
CODEC_CLKOUT	D22	MICIN	J23
CSB	D23	RHPOUT	B21
CSCL	B23	RLINEIN	F23
CSDA	C23	ROUT	G22
CVDD	H17[1]	VMID	G23
DACDAT	A18	XTI/CODEC_MCLK	A22
DACLRC	A17	XTO	A21

[1] For ADSP-BF52x processor (without internal codec) compatibility, connect this ball to V_{DDEXT}.

Table 24. 289-Ball CSP_BGA Ball Assignment (Numerically)

Ball No.	Signal	Ball No.	Signal
A15	ADCLRC	E22	CMODE
A16	ADCDAT	E23	LLINEIN
A17	DACLRC	F22	LOUT
A18	DACDAT	F23	RLINEIN
A19	CODEC_BCLK	G16[1]	HPVDD
A21	XTO	G17	HPGND
A22	XTI/CODEC_MCLK	G22	ROUT
B20	LHPOUT	G23	VMID
B21	RHPOUT	H17[1]	CVDD
B23	CSCL	H22	AGND
C23	CSDA	H23	MICBIAS
D22	CODEC_CLKOUT	J22[1]	AVDD
D23	CSB	J23	MICIN

[1] For ADSP-BF52x processor (without internal codec) compatibility, connect this ball to V_{DDEXT}.

OUTLINE DIMENSIONS

Dimensions in Figure 35, 289-Ball CSP_BGA (BC-289-2) are shown in millimeters.

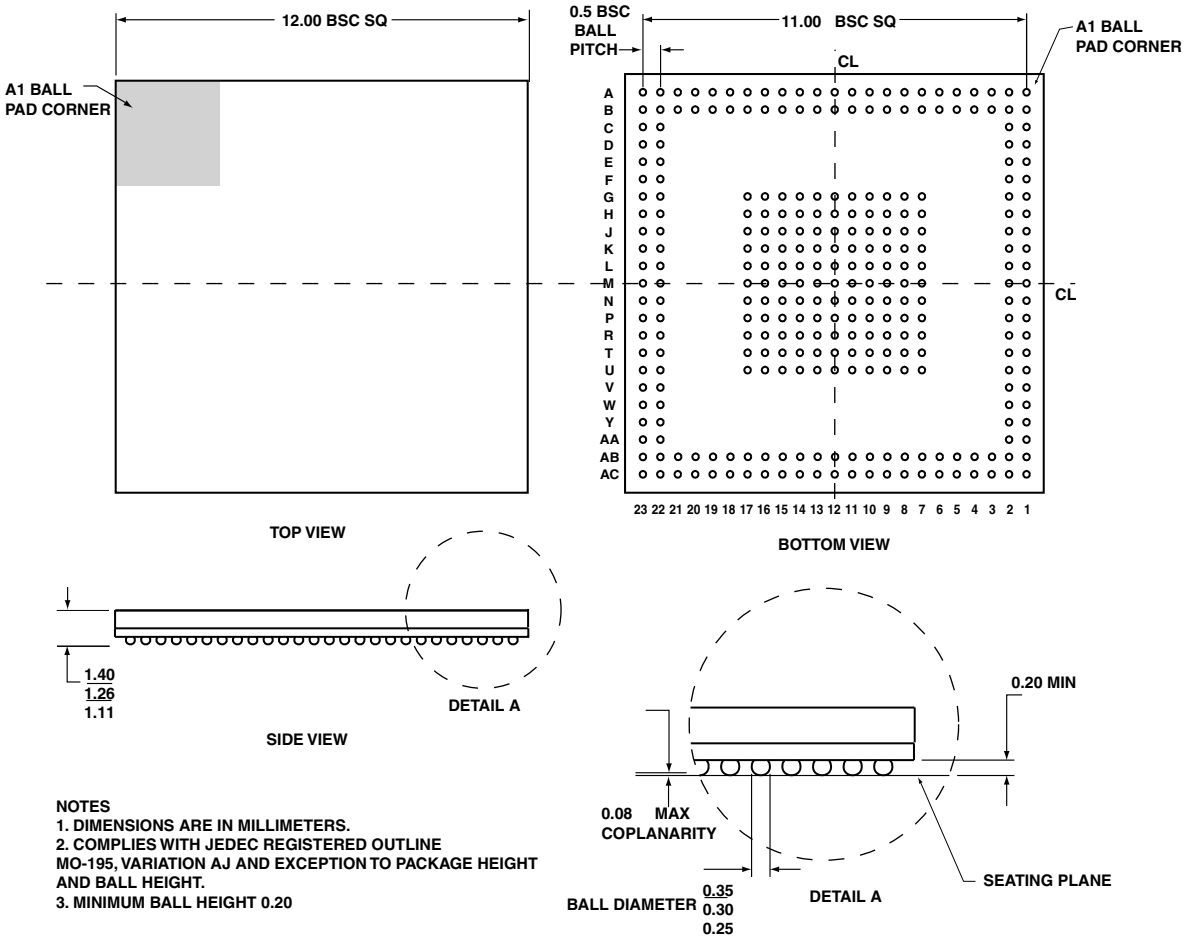

Figure 35. 289-Ball CSP_BGA (BC-289-2)

ORDERING GUIDE

Model[1]	Temperature Range[2]	Instruction Rate (Max)	Package Description	Package Option
ADSP-BF522KBCZ-3C2	0°C to +70°C	300 MHz	289-Ball Chip Scale Package Ball Grid Array (CSP_BGA)	BC-289-2
ADSP-BF522KBCZ-4C2	0°C to +70°C	400 MHz	289-Ball Chip Scale Package Ball Grid Array (CSP_BGA)	BC-289-2
ADSP-BF523KBCZ-5C2	0°C to +70°C	533 MHz	289-Ball Chip Scale Package Ball Grid Array (CSP_BGA)	BC-289-2
ADSP-BF523KBCZ-6C2	0°C to +70°C	600 MHz	289-Ball Chip Scale Package Ball Grid Array (CSP_BGA)	BC-289-2
ADSP-BF524KBCZ-3C2	0°C to +70°C	300 MHz	289-Ball Chip Scale Package Ball Grid Array (CSP_BGA)	BC-289-2
ADSP-BF524KBCZ-4C2	0°C to +70°C	400 MHz	289-Ball Chip Scale Package Ball Grid Array (CSP_BGA)	BC-289-2
ADSP-BF525KBCZ-5C2	0°C to +70°C	533 MHz	289-Ball Chip Scale Package Ball Grid Array (CSP_BGA)	BC-289-2
ADSP-BF525KBCZ-6C2	0°C to +70°C	600 MHz	289-Ball Chip Scale Package Ball Grid Array (CSP_BGA)	BC-289-2
ADSP-BF526KBCZ-3C2	0°C to +70°C	300 MHz	289-Ball Chip Scale Package Ball Grid Array (CSP_BGA)	BC-289-2
ADSP-BF526KBCZ-4C2	0°C to +70°C	400 MHz	289-Ball Chip Scale Package Ball Grid Array (CSP_BGA)	BC-289-2
ADSP-BF527KBCZ-5C2	0°C to +70°C	533 MHz	289-Ball Chip Scale Package Ball Grid Array (CSP_BGA)	BC-289-2
ADSP-BF527KBCZ-6C2	0°C to +70°C	600 MHz	289-Ball Chip Scale Package Ball Grid Array (CSP_BGA)	BC-289-2

[1] Z = RoHS Compliant Part.

[2] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 21 for junction temperature (T_J) specification which is the only temperature specification.

D06876-0-3/10(A)