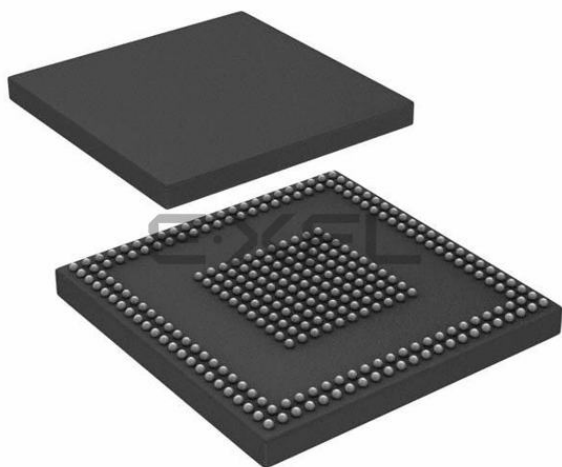




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Understanding [Embedded - DSP \(Digital Signal Processors\)](#)

[Embedded - DSP \(Digital Signal Processors\)](#) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of [Embedded - DSP \(Digital Signal Processors\)](#)

Details

Product Status	Obsolete
Type	Fixed Point
Interface	DMA, I ² C, PPI, SPI, SPORT, UART
Clock Rate	600MHz
Non-Volatile Memory	ROM (32kB)
On-Chip RAM	132kB
Voltage - I/O	1.8V, 2.5V, 3.3V
Voltage - Core	1.10V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	289-LFBGA, CSPBGA
Supplier Device Package	289-CSPBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf523kbcz-6c2

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REVISION HISTORY

3/10—Rev. 0 to Rev. A

Revised the following figures.

Recommended Application Circuit Using SPI Control 13

Recommended Application Circuit Using TWI Control .. 14

Added Sampling Rate = 48 kHz to all figures in

Converter Filter Response 30

Revised Ordering Guide 36

GENERAL DESCRIPTION

This document describes the differences between the ADSP-BF52xC and the ADSP-BF52x standard Blackfin® product. Please refer to the published ADSP-BF52x data sheet for general description and specifications. This document only describes the differences from that data sheet.

The ADSP-BF52xC processors add a low power, high quality stereo audio codec for portable digital audio applications with one set of stereo programmable gain amplifier (PGA) line inputs and one monaural microphone input. It features two 24-bit analog-to-digital converter (ADC) channels and two 24-bit digital-to-analog (DAC) converter channels.

The codec can operate as a master or a slave. It supports various master clock frequencies, including 12 MHz or 24 MHz for USB devices; standard $256 \times f_s$ or $384 \times f_s$ based rates, such as 12.288 MHz and 24.576 MHz; and many common audio sampling rates, such as 96 kHz, 88.2 kHz, 48 kHz, 44.1 kHz, 32 kHz, 24 kHz, 22.05 kHz, 16 kHz, 12 kHz, 11.025 kHz, and 8 kHz.

The codec can operate at power supplies as low as 1.8 V for the analog circuitry and as low as 1.8 V for the digital circuitry. The maximum voltage supply is 3.6 V for all supplies.

The codec software-programmable stereo output options provide the programmer with many application possibilities because the device can be used as a headphone driver or as a speaker driver. Its volume control functions provide a large range of gain control of the audio signal.

CODEC DESCRIPTION

The ADSP-BF52xC codec contains a central clock source, called the codec master clock (CODEC_MCLK) that produces a reference clock for all internal audio data processing and synchronization. When using an external clock source to drive the CODEC_MCLK pin, care should be taken to select a clock source with less than 50 ps of jitter. Without careful generation of the CODEC_MCLK signal, the digital audio quality will suffer.

To enable the codec to generate the central reference clock in a system, connect a crystal oscillator between the XT1/ CODEC_MCLK input pin and the XTO output pin.

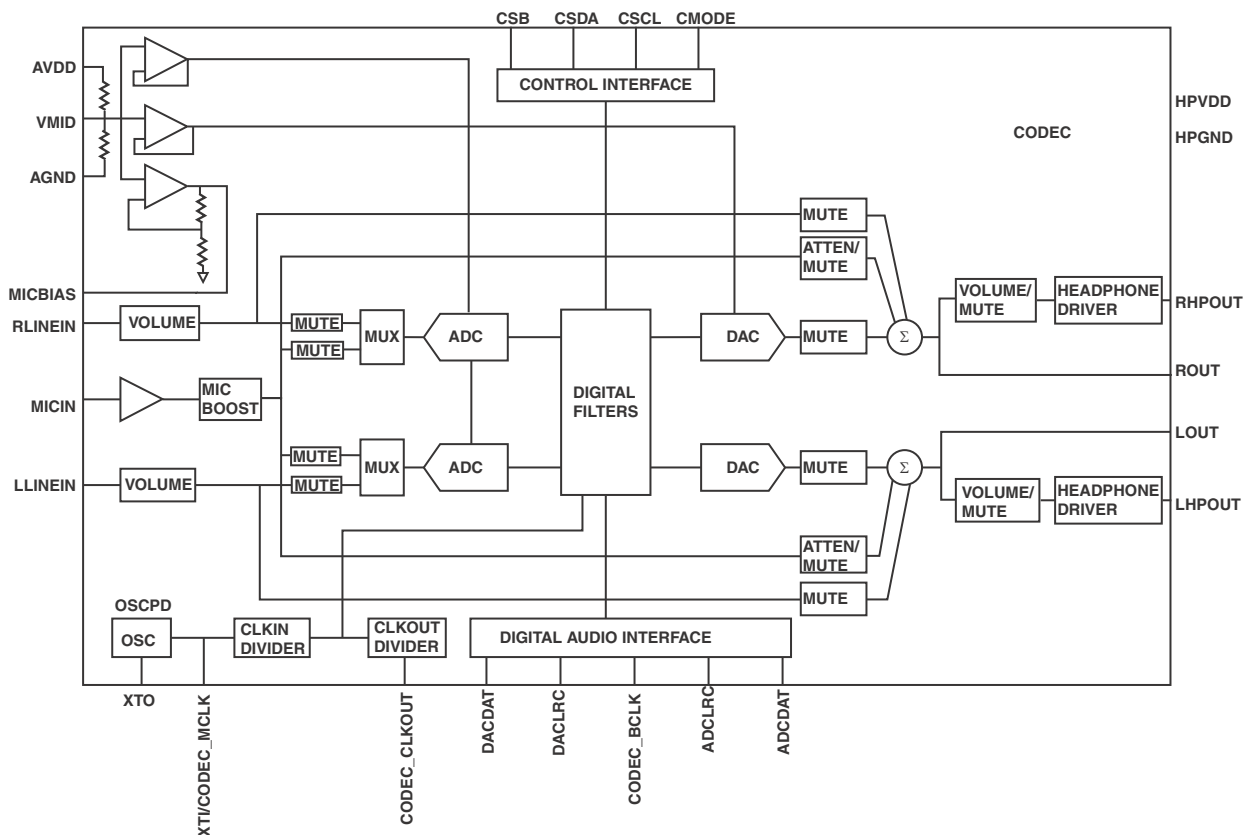


Figure 1. Codec Block Diagram

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To allow an external device to generate the central reference clock, apply the external clock signal directly through the XTI/ CODEC_MCLK input pin. In this configuration, the oscillator circuit of the codec can be powered down by using the OSCPD bit (Register R6, Bit D5) to reduce power consumption.

To accommodate applications with very high frequency master clocks, the internal core reference clock of the codec can be set to either CODEC_MCLK or CODEC_MCLK divided by 2. This is enabled by adjusting the setting of the CLKDIV2 bit (Register R8, Bit D6). The CODEC_CLKOUT pin can also drive external clock sources with either the codec clock signal or codec clock divided by 2 by enabling the CLKODIV2 bit (Register R8, Bit D7).

ADC AND DAC

The codec contains a pair of oversampling Σ - Δ ADCs. The maximum ADC full-scale input level is $1.0 V_{rms}$ when $AVDD = 3.3 V$. If the input signal to the ADC exceeds this level, data overloading occurs and causes audible distortion.

The ADC can accept analog audio input from either the stereo line inputs or the monaural microphone input. Note that the ADC can only accept input from a single source, so the programmer must choose either the line inputs or the microphone input using the INSEL bit (Register R4, Bit D2). The digital data from the ADC output, once converted, is processed using the ADC filters.

Complementary to the Σ - Δ ADC channels, the codec contains a pair of oversampling DACs that convert the digital audio data from the internal DAC filters into an analog audio signal. The DAC output can also be muted by setting the DACMU bit (Register R5, Bit D3) in the control register.

ADC HIGH-PASS AND DAC DE-EMPHASIS FILTERS

The ADC and DAC employ separate digital filters that perform 24-bit signal processing. The digital filters are used for both record and playback modes and are optimized for each individual sampling rate used.

For recording mode operations, the unprocessed data from the ADC enters the ADC filters and is converted to the appropriate sampling frequency, then is output to the digital audio interface.

For playback mode operations, the DAC filters convert the digital audio interface data to oversampled data using a sampling rate selected by the programmer. The oversampled data is processed by the DAC and sent to the analog output mixer by enabling the DACSEL (Register R4, Bit D4).

Programmers have the option of setting up the device so that any dc offset in the input source signal is automatically detected and removed. To accomplish this, enable the digital high-pass filter (see Table 22 on Page 30 for characteristics) contained in the ADC digital filters by using the ADCHPD bit (Register R5, Bit D0).

In addition, programmers can implement digital de-emphasis by using the DEEMPH bits (Register R5, Bit D1 and Bit D2).

ANALOG AUDIO INTERFACES

The codec includes stereo single-ended line inputs and a monaural microphone input to the on-board ADC. Either the line inputs or the microphone input, but not both simultaneously, can be connected to the ADC by setting the INSEL bit (Register R4, Bit D2).

The codec also includes line and headphone outputs from the on-board DAC. The line or microphone inputs can be routed and mixed directly to the output terminals.

Stereo Line and Monaural Microphone Inputs

The single-ended stereo line inputs (RLINEIN and LLINEIN) are internally biased to VMID by way of a voltage divider between AVDD and AGND (see Figure 2). The line input signal can be connected to the internal ADC and, if desired, routed directly to the outputs via the bypass path by using the BYPASS bit (Register R4, Bit D3).

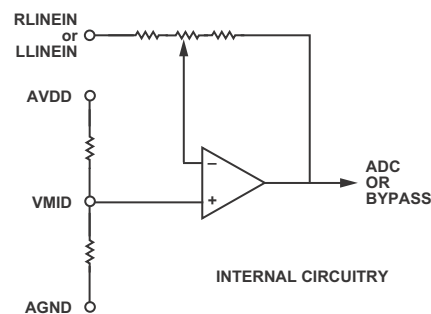


Figure 2. Line Input to ADC

The line input volume can be adjusted from -34.5 dB to $+33 \text{ dB}$ in steps of $+1.5 \text{ dB}$ by setting the LINVOL (Register R0, Bit D0 to Bit D5) and RINVOL (Register R1, Bit D0 to Bit D5) bits. By default the volume is independently adjustable for both right and left line inputs. However, if the LRINBOTH or RLINBOTH bit is programmed, both LINVOL and RINVOL are loaded with the same value. The programmer can also set the LINMUTE (Register R0, Bit D7) and RINMUTE (Register R1, Bit D7) bits to mute the line input signal to the ADC.

The high impedance, low capacitance monaural microphone input pin (MICIN, shown in Figure 3) has two gain stages and a microphone bias level (MICBIAS) that is internally biased to the VMID voltage level by way of a voltage divider between AVDD and AGND. The microphone input signal can be connected to the internal ADC and, if desired, routed directly to the outputs via the sidetone path by using the SIDETONE bit (Register R4, Bit D5).

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The programmer can simultaneously load the volume control of both channels by writing to the LRHPBOTH (Register R2, Bit D8) and RLHPBOTH (Register R3, Bit D8) bits of the left- or right-channel DAC volume registers.

The maximum output level of the headphone outputs is 1.0 V rms when AVDD and HPVDD = 3.3 V. To suppress audible pops and clicks, the headphone and line outputs are held at the VMID dc voltage level when the device is set to standby mode or when the headphone outputs are muted.

The stereo line outputs of the codec, the LOUT and ROUT pins, can drive a load impedance of 10 k Ω and 50 pF. The line output signal levels are not adjustable at the output mixer, which has a fixed gain of 0 dB. The maximum output level of the line outputs is 1.0 V rms when AVDD = 3.3 V.

DIGITAL AUDIO INTERFACE

The digital audio input can support the following digital audio communication protocols: right-justified mode, left-justified mode, I²S mode, and frame sync mode. See [Figure 6 on Page 6](#) through [Figure 10 on Page 7](#).

The mode selection is performed by writing to the FORMAT bits of the digital audio interface register (Register R7, Bit D1 and Bit D0). All modes are MSB first and operate with data of 16 to 32 bits.

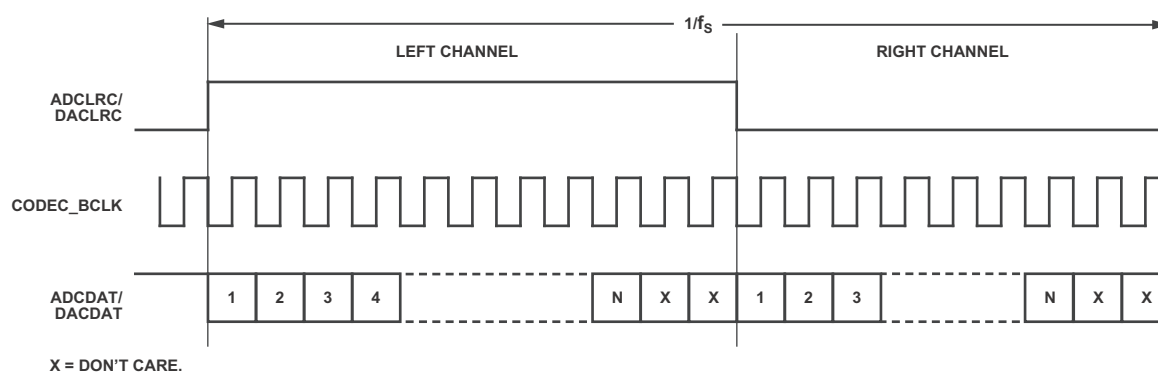


Figure 6. Left-Justified Audio Input Mode

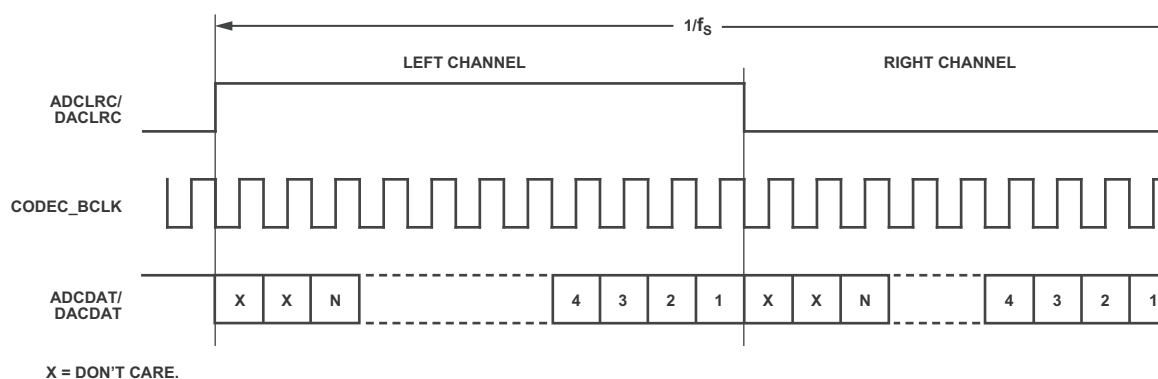


Figure 7. Right-Justified Audio Input Mode

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Normal Mode

In normal mode, the codec supports digital audio sampling rates from 8 kHz to 96 kHz. Normal mode supports $256 \times f_s$ and $384 \times f_s$ based clocks. To select the desired sampling rate, the programmer must set the appropriate sampling rate register in

the SR control bits (Register R8, Bit D2 to Bit D5) and match this selection to the core clock frequency that is pulsed on the CODEC_MCLK pin. See [Table 1](#) for sampling rates in normal mode.

Table 1. Sampling Rate Lookup Table, Normal Mode (USB Disabled)

CODEC_MCLK (CLKDIV2 = 0)	CODEC_MCLK (CLKDIV2 = 1)	ADC Sampling Rate (ADCLRC)	DAC Sampling Rate (DACLRC)	USB	SR [3:0]	BOSR	CODEC_BCLK (MS = 1) ¹
12.288 MHz	24.576 MHz	8 kHz (CODEC_MCLK/1536)	8 kHz (CODEC_MCLK/1536)	0	0011	0	CODEC_MCLK/4
		8 kHz (CODEC_MCLK/1536)	48 kHz (CODEC_MCLK/256)	0	0010	0	CODEC_MCLK/4
		12 kHz (CODEC_MCLK/1024)	12 kHz (CODEC_MCLK/1024)	0	0100	0	CODEC_MCLK/4
		16 kHz (CODEC_MCLK/768)	16 kHz (CODEC_MCLK/768)	0	0101	0	CODEC_MCLK/4
		24 kHz (CODEC_MCLK/512)	24 kHz (CODEC_MCLK/512)	0	1110	0	CODEC_MCLK/4
		32 kHz (CODEC_MCLK/384)	32 kHz (CODEC_MCLK/384)	0	0110	0	CODEC_MCLK/4
		48 kHz (CODEC_MCLK/256)	8 kHz (CODEC_MCLK/1536)	0	0001	0	CODEC_MCLK/4
		48 kHz (CODEC_MCLK/256)	48 kHz (CODEC_MCLK/256)	0	0000	0	CODEC_MCLK/4
		96 kHz (CODEC_MCLK/128)	96 kHz (CODEC_MCLK/128)	0	0111	0	CODEC_MCLK/2
11.2896 MHz	22.5792 MHz	8.0182 kHz (CODEC_MCLK/1408)	8.0182 kHz (CODEC_MCLK/1408)	0	1011	0	CODEC_MCLK/4
		8.0182 kHz (CODEC_MCLK/1408)	44.1 kHz (CODEC_MCLK/256)	0	1010	0	CODEC_MCLK/4
		11.025 kHz (CODEC_MCLK/1024)	11.025 kHz (CODEC_MCLK/1024)	0	1100	0	CODEC_MCLK/4
		22.05 kHz (CODEC_MCLK/512)	22.05 kHz (CODEC_MCLK/512)	0	1101	0	CODEC_MCLK/4
		44.1 kHz (CODEC_MCLK/256)	8.0182 kHz (CODEC_MCLK/1408)	0	1001	0	CODEC_MCLK/4
		44.1 kHz (CODEC_MCLK/256)	44.1 kHz (CODEC_MCLK/256)	0	1000	0	CODEC_MCLK/4
18.432 MHz	36.864 MHz	88.2 kHz (CODEC_MCLK/128)	88.2 kHz (CODEC_MCLK/128)	0	1111	0	CODEC_MCLK/2
		8 kHz (CODEC_MCLK/2304)	8 kHz (CODEC_MCLK/2304)	0	0011	1	CODEC_MCLK/6
		8 kHz (CODEC_MCLK/2304)	48 kHz (CODEC_MCLK/384)	0	0010	1	CODEC_MCLK/6
		12 kHz (CODEC_MCLK/1536)	12 kHz (CODEC_MCLK/1536)	0	0100	1	CODEC_MCLK/6
		16 kHz (CODEC_MCLK/1152)	16 kHz (CODEC_MCLK/1152)	0	0101	1	CODEC_MCLK/6
		24 kHz (CODEC_MCLK/768)	24 kHz (CODEC_MCLK/768)	0	1110	1	CODEC_MCLK/6
		32 kHz (CODEC_MCLK/576)	32 kHz (CODEC_MCLK/576)	0	0110	1	CODEC_MCLK/6
		48 kHz (CODEC_MCLK/384)	48 kHz (CODEC_MCLK/384)	0	0000	1	CODEC_MCLK/6
		48 kHz (CODEC_MCLK/384)	8 kHz (CODEC_MCLK/2304)	0	0001	1	CODEC_MCLK/6
16.9344 MHz	33.8688 MHz	96 kHz (CODEC_MCLK/192)	96 kHz (CODEC_MCLK/192)	0	0111	1	CODEC_MCLK/3
		8.0182 kHz (CODEC_MCLK/2112)	8.0182 kHz (CODEC_MCLK/2112)	0	1011	1	CODEC_MCLK/6
		8.0182 kHz (CODEC_MCLK/2112)	44.1 kHz (CODEC_MCLK/384)	0	1010	1	CODEC_MCLK/6
		11.025 kHz (CODEC_MCLK/1536)	11.025 kHz (CODEC_MCLK/1536)	0	1100	1	CODEC_MCLK/6
		22.05 kHz (CODEC_MCLK/768)	22.05 kHz (CODEC_MCLK/768)	0	1101	1	CODEC_MCLK/6
		44.1 kHz (CODEC_MCLK/384)	8.0182 kHz (CODEC_MCLK/2112)	0	1001	1	CODEC_MCLK/6
		44.1 kHz (CODEC_MCLK/384)	44.1 kHz (CODEC_MCLK/384)	0	1000	1	CODEC_MCLK/6
		88.2 kHz (CODEC_MCLK/192)	88.2 kHz (CODEC_MCLK/192)	0	1111	1	CODEC_MCLK/3

¹ CODEC_BCLK frequency is for master mode and slave right-justified mode only.

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USB Mode

In USB mode, the codec supports digital audio sampling rates from 8 kHz to 96 kHz. USB mode is enabled on the codec to support the common universal serial bus (USB) clock rate of

12 MHz, or to support 24 MHz if the CLKDIV2 control register bit is activated. The programmer must set the appropriate sampling rate in the SR control bits (Register R8, Bit D2 to Bit D5). See [Table 2](#) for sampling rates in USB mode.

Table 2. Sampling Rate Lookup Table, USB Mode (USB Enabled)

CODEC_MCLK (CLKDIV2 = 0)	CODEC_MCLK (CLKDIV2 = 1)	ADC Sampling Rate (ADCLRC)	DAC Sampling Rate (DACLRC)	USB	SR [3:0]	BOSR	CODEC_BCLK (MS = 1) ¹
12.000 MHz	24.000 MHz	8 kHz (CODEC_MCLK/1500)	8 kHz (CODEC_MCLK/1500)	1	0011	0	CODEC_MCLK
		8 kHz (CODEC_MCLK/1500)	48 kHz (CODEC_MCLK/250)	1	0010	0	CODEC_MCLK
		8.0214 kHz (CODEC_MCLK/1496)	8.0214 kHz (CODEC_MCLK/1496)	1	1011	1	CODEC_MCLK
		8.0214 kHz (CODEC_MCLK/1496)	44.118 kHz (CODEC_MCLK/272)	1	1010	1	CODEC_MCLK
		11.0259 kHz (CODEC_MCLK/1088)	11.0259 kHz (CODEC_MCLK/1088)	1	1100	1	CODEC_MCLK
		12 kHz (CODEC_MCLK/1000)	12 kHz (CODEC_MCLK/1000)	1	1000	0	CODEC_MCLK
		16 kHz (CODEC_MCLK/750)	16 kHz (CODEC_MCLK/750)	1	1010	0	CODEC_MCLK
		22.0588 kHz (CODEC_MCLK/544)	22.0588 kHz (CODEC_MCLK/544)	1	1101	1	CODEC_MCLK
		24 kHz (CODEC_MCLK/500)	24 kHz (CODEC_MCLK/500)	1	1110	0	CODEC_MCLK
		32 kHz (CODEC_MCLK/375)	32 kHz (CODEC_MCLK/375)	1	0110	0	CODEC_MCLK
		44.118 kHz (CODEC_MCLK/272)	8.0214 kHz (CODEC_MCLK/1496)	1	1001	1	CODEC_MCLK
		44.118 kHz (CODEC_MCLK/272)	44.118 kHz (CODEC_MCLK/272)	1	1000	1	CODEC_MCLK
		48 kHz (CODEC_MCLK/250)	8 kHz (CODEC_MCLK/1500)	1	0001	0	CODEC_MCLK
		48 kHz (CODEC_MCLK/250)	48 kHz (CODEC_MCLK/250)	1	0000	0	CODEC_MCLK
		88.235 kHz (CODEC_MCLK/136)	88.235 kHz (CODEC_MCLK/136)	1	1111	1	CODEC_MCLK
		96 kHz (CODEC_MCLK/125)	96 kHz (CODEC_MCLK/125)	1	0111	0	CODEC_MCLK

¹ CODEC_BCLK frequency is for master mode and slave right-justified mode only.

SOFTWARE CONTROL INTERFACE

The software control interface provides access to the programmer-selectable control registers and can operate with a 2-wire (TWI) or 3-wire (SPI) interface, depending on the setting of the CMODE pin. If the CMODE pin is set to 0, the 2-wire interface is selected; if 1, the 3-wire interface is selected.

Within each control register is a control data-word consisting of 16 bits, MSB first. Bit B15 to Bit B9 are the register map address, and Bit B8 to Bit B0 are register data for the associated register map.

When 2-wire (TWI) mode is selected, CSDA generates the serial control data-word; CSCL clocks the serial data; and CSB determines the TWI device address. If the CSB pin is set to 0, the address selected is 0011010; if 1, the address is 0011011.

When 3-wire (SPI) mode is selected, CSDA generates the control data-word, CSCL clocks the control data-word into the codec, and CSB latches in the control data-word.

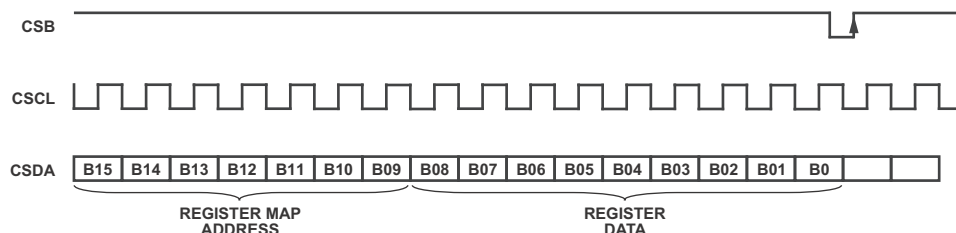


Figure 11. Codec SPI Serial Interface

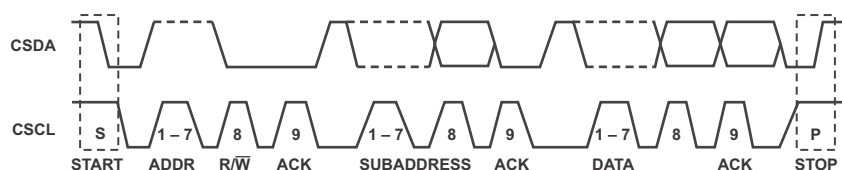


Figure 12. Codec TWI Serial Interface

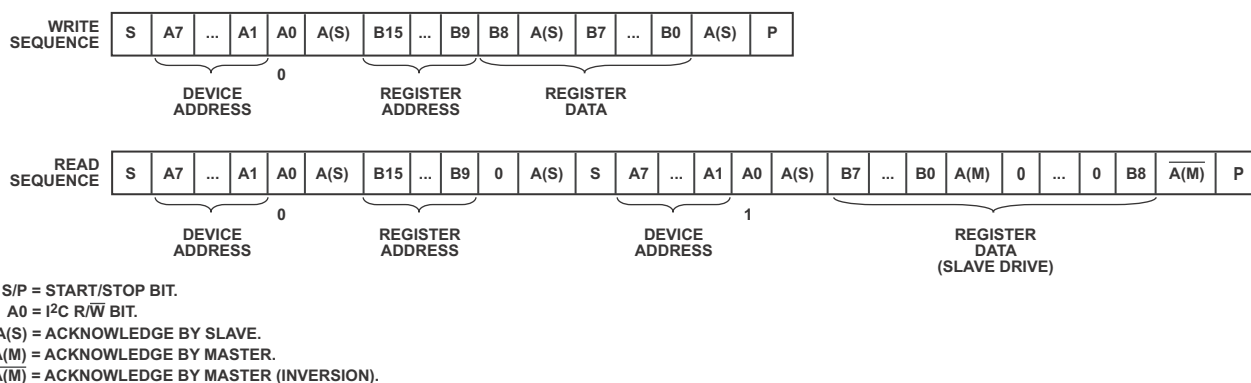


Figure 13. Codec TWI Write and Read Sequences

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Figure 14 on Page 13 and Figure 15 on Page 14 describe alternative external connections for SPI or TWI control of the ADSP-BF52xC codec. The figures are the same except for the shaded area in each.

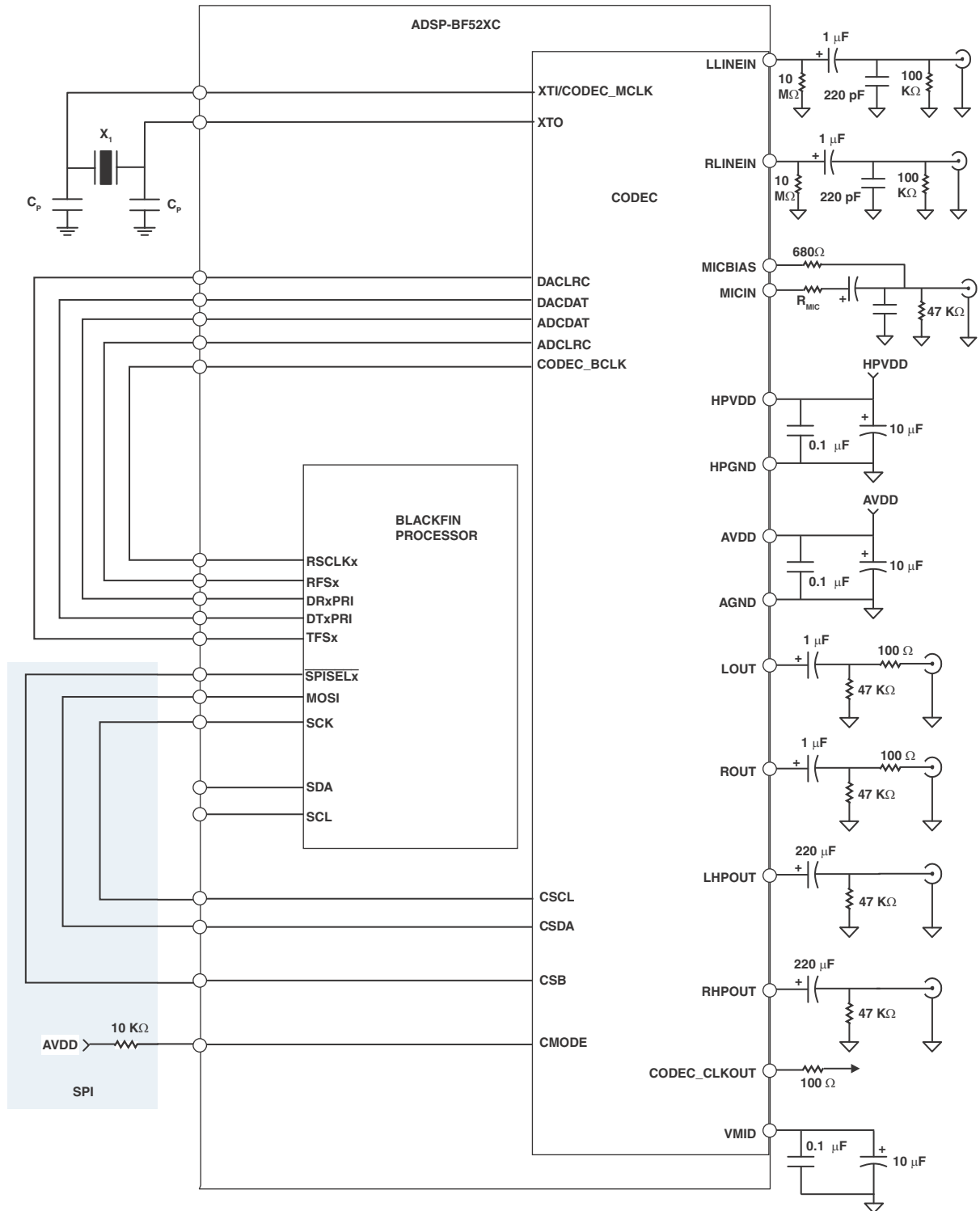


Figure 14. Recommended Application Circuit Using SPI Control

REGISTER DETAILS

Register	Address	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 0 Left-Channel ADC Input Volume on Page 16	0x00	LRINBOTH	LINMUTE	0	LINVOL					
		Default = 010010111								
Register 1 Right-Channel ADC Input Volume on Page 17	0x01	RLINBOTH	RINMUTE	0	RINVOL					
		Default = 010010111								
Register 2 Left-Channel DAC Volume on Page 17	0x02	LRHPBOTH	LZCEN	LHPVOL						
		Default = 001111001								
Register 3 Right-Channel DAC Volume on Page 18	0x03	RLHPBOTH	RZCEN	RHPVOL						
		Default = 001111001								
Register 4 Analog Audio Path on Page 18	0x04	MICBOOST2	SIDEATT[1:0]		SIDETONE	DACSEL	BYPASS	INSEL	MUTEMIC	MICBOOST
		Default = 000001010								
Register 5 Digital Audio Path on Page 19	0x05	0	0	0	0	HPOR	DACMU	DEEMPH[1:0]		ADC HPD
		Default = 000001000								
Register 6 Power Management on Page 19	0x06	0	POWEROFF	CLKOUTPD	OSCPD	OUTPD	DACPD	ADCPD	MICPD	LINEINPD
		Default = 010011111								
Register 7 Digital Audio I/F on Page 20	0x07	0	BCLKINV	MS	LRSWAP	LRP	WL[1:0]		FORMAT[1:0]	
		Default = 000001010								
Register 8 Sampling Rate on Page 20	0x08	0	CLKODIV2	CLKDIV2	SR[3:0]				BOSR	USB
		Default = 000000000								
Register 9 Active on Page 20	0x09	0	0	0	0	0	0	0	0	ACTIVE
		Default = 000000000								
Register 10 Software Reset on Page 20	0x0F	RESET								
		Default = 000000000								

Figure 16. Register Mapping

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BIT DESCRIPTIONS

Table 4 through Table 14 on Page 20 describe each bit in the control registers.

Table 4. Register 0 Left-Channel ADC Input Volume

Bit Name	Bits	Description	Settings
LRINBOTH	B8	Left-to-right line input ADC data load control	0 = disable simultaneous loading of left-channel ADC data to right-channel register (default) 1 = enable simultaneous loading of left-channel ADC data to right-channel register
LINMUTE	B7	Left-channel input mute	0 = disable mute 1 = enable mute on data path to ADC (default)
LINVOL	B[5:0]	Left-channel PGA volume control	00 0000 = -34.5 dB ... 1.5 dB step up 01 0111 = 0 dB (default) ... 1.5 dB step up 01 1111 = 12 dB 10 0000 = 13.5 dB 10 0001 = 15 dB 10 0010 = 16.5 dB 10 0011 = 18 dB 10 0100 = 19.5 dB 10 0101 = 21 dB 10 0110 = 22.5 dB 10 0111 = 24 dB 10 1000 = 25.5 dB 10 1001 = 27 dB 10 1010 = 28.5 dB 10 1011 = 30 dB 10 1100 = 31.5 dB 10 1101 = 33 dB 11 1111 to 10 1101 = 33 dB

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Table 7. Register 3 Right-Channel DAC Volume

Bit Name	Bits	Description	Settings
RLHPBOTH	B8	Right-to-left headphone volume load control	0 = disable simultaneous loading of right-channel headphone volume data to left-channel register (default) 1 = enable simultaneous loading of right-channel headphone volume data to left-channel register
RZCEN	B7	Right-channel zero cross detect enable	0 = disable (default) 1 = enable
RHPVOL [6:0]	B[6:0]	Right-channel headphone volume control	000 0000 to 010 1111 = mute 011 0000 = -73 dB ... 111 1001 = 0 dB (default) ... 1 dB steps up to 111 1111 = +6 dB

Table 8. Register 4 Analog Audio Path

Bit Name	Bits	Description	Settings
MICBOOST2	B8	Additional microphone amplifier gain booster control	0 = 0 dB (default) 1 = 20 dB
SIDEATT[1:0]	B[7:6]	Microphone sidetone gain control	00 = -6 dB (default) 01 = -9 dB 10 = -12 dB 11 = -15 dB
SIDETONE	B5	Sidetone enable. Allow attenuated microphone signal to be mixed at device output terminal	0 = sidetone disable (default) 1 = sidetone enable
DACSEL	B4	DAC select—allow DAC output to be mixed at device output terminal	0 = do not select DAC (default) 1 = select DAC
BYPASS	B3	Bypass select—allow line input signal to be mixed at device output terminal	0 = bypass disable 1 = bypass enable (default)
INSEL	B2	Line input or microphone input select to ADC	0 = line input select to ADC (default) 1 = microphone input select to ADC
MUTEMIC	B1	Microphone mute control to ADC	0 = mute on data path to ADC disable 1 = mute on data path to ADC enable (default)
MICBOOST	B0	Primary microphone amplifier gain booster control	0 = 0 dB (default) 1 = 20 dB

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Table 9. Register 5 Digital Audio Path

Bit Name	Bits	Description	Settings
HPOR	B4	Store dc offset when high-pass filter is disabled	0 = clear offset (default) 1 = store offset
DACMU	B3	DAC digital mute	0 = no mute (signal active) 1 = mute (default)
DEEMPH[1:0]	B[2:1]	De-emphasis control	00 = no de-emphasis (default) 01 = 32 kHz sampling rate 10 = 44.1 kHz sampling rate 11 = 48 kHz sampling rate
ADCHPD	B0	ADC high-pass filter control	0 = ADC high-pass filter enable (default) 1 = ADC high-pass filter disable

Table 10. Register 6 Power Management

Bit Name	Bits	Description	Settings
POWEROFF	B7	Whole chip power-down control	0 = power-up 1 = power-down (default)
CLKOUTPD	B6	Clock output power-down control	0 = power-up (default) 1 = power-down
OSCPD	B5	Crystal power-down control	0 = power-up (default) 1 = power-down
OUTPD	B4	Output power-down control	0 = power-up 1 = power-down (default)
DACPD	B3	DAC power-down control	0 = power-up 1 = power-down (default)
ADCPD	B2	ADC power-down control	0 = power-up 1 = power-down (default)
MICPD	B1	Microphone input power-down control	0 = power-up 1 = power-down (default)
LINEINPD	B0	Line input power-down control	0 = power-up 1 = power-down (default)

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SPECIFICATIONS

$T_{\text{Ambient}} = 25^{\circ}\text{C}$, $\text{AVDD} = \text{VDDEXT} = 3.3 \text{ V}$, $\text{HPVDD} = 3.3 \text{ V}$,
1 kHz signal, $f_s = 48 \text{ kHz}$, PGA gain = 0 dB, 24-bit audio data,
unless otherwise noted.

OPERATING CONDITIONS

See operating conditions in the published ADSP-BF52xC
data sheet.

Parameter	Conditions	Min	Typical	Max	Unit
AVDD ¹		1.8	3.3	3.6	V
HPVDD		1.8	3.3	3.6	V

¹ Note that AVDD must equal HPVDD.

CODEC ELECTRICAL CHARACTERISTICS

Parameter	Conditions	Min	Typical	Max	Unit
<i>Line Input</i>					
Input Signal Level (0 dB)			AVDD/3.3		V(rms)
Input Impedance	PGA gain = 0 dB		200		k Ω
	PGA gain = +33 dB		10		k Ω
	PGA gain = -34.5 dB		480		k Ω
Input Capacitance			10		pF
Signal-to-Noise Ratio (A-Weighted)	PGA gain = 0 dB, AVDD = 3.3 V	82	87		dB
	PGA gain = 0 dB, AVDD = 1.8 V		84		dB
Total Harmonic Distortion (THD)	-1 dBFS input, AVDD = 3.3 V	-80	-84		dB
	-1 dBFS input, AVDD = 1.8 V		-71	-60	dB
Channel Separation ¹			80		dB
Programmable Gain		-34.5	0	+33.5	dB
Gain Step			1.5		dB
Mute Attenuation			-80		dB
<i>Microphone Input</i>					
Input Signal Level			1		V(rms)
Signal-to-Noise Ratio (A-Weighted)	Microphone gain = 0 dB ($R_{\text{SOURCE}} = 40 \text{ k}\Omega$)		85		dB
Total Harmonic Distortion	-1 dBFS input, 0 dB gain, AVDD = 3.3 V		-75		dB
	-1 dBFS input, 0 dB gain, AVDD = 1.8 V		-65		dB
Power Supply Rejection Ratio			50		dB
Mute Attenuation			80		dB
Input Resistance			10		k Ω
Input Capacitance			10		pF
<i>Microphone Bias</i>					
Bias Voltage			$0.75 \times \text{AVDD}$		V
Bias Current Source				3	mA
Noise in the Signal Bandwidth	20 Hz to 20 kHz		40		nV/ $\sqrt{\text{Hz}}$

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Parameter	Conditions	Min	Typical	Max	Unit
<i>Line Output</i>					
DAC	–1 dBFS input DAC + line output				
Full-Scale Output			AVDD/3.3		V(rms)
Signal-to-Noise Ratio (A-Weighted)	AVDD = 3.3 V	90	95		dB
	AVDD = 1.8 V	85	88		dB
THD + N	AVDD = 3.3 V		–80	–70	dB
	AVDD = 1.8 V		–80	–70	dB
Power Supply Rejection Ratio			50		dB
Channel Separation			80		dB
<i>Headphone Output</i>					
Full-Scale Output Voltage			AVDD/3.3		V(rms)
Maximum Output Power	$R_L = 32 \Omega$		30		mW
	$R_L = 16 \Omega$		60		mW
Signal-to-Noise Ratio (A-Weighted)	AVDD = 3.3 V	90	94		dB
	AVDD = 1.8 V	80	85		dB
THD + N	HPOUT = 10 mW		–65		dB
	HPOUT = 20 mW		–60		dB
Power Supply Rejection Ratio			50		dB
Mute Attenuation			80		dB
<i>Line Input To Line Output</i>					
Full-Scale Output Voltage			AVDD/3.3		V(rms)
Signal-to-Noise Ratio (A-Weighted)	AVDD = 3.3 V		92		dB
	AVDD = 1.8 V		86		dB
Total Harmonic Distortion	AVDD = 3.3 V		–80		dB
	AVDD = 1.8 V		–80		dB
Power Supply Rejection			50		dB
<i>Microphone Input To Headphone Output</i>					
Full-Scale Output Voltage			AVDD/3.3		V(rms)
Signal-to-Noise Ratio (A-Weighted)	AVDD = 3.3 V		94		dB
	AVDD = 1.8 V		88		dB
Power Supply Rejection Ratio			50		dB
Programmable Attenuation		6		15	dB
Gain Step			3		dB
Mute Attenuation			80		dB

¹ Guaranteed but not tested.

ABSOLUTE MAXIMUM RATINGS

See absolute maximum ratings in the published ADSP-BF52x processor data sheet.

ESD SENSITIVITY



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PACKAGE INFORMATION

The information presented in [Figure 17](#) and [Table 15](#) provides details about the package branding for the ADSP-BF52xC processor. For a complete listing of product availability, see [Ordering Guide on Page 36](#).



Figure 17. Product Information on Package

Table 15. Package Brand Information

Brand Key	Field Description
t	Temperature Range
pp	Package Type
Z	Lead Free Option
ccc	See Ordering Guide
vvvvvv.x	Assembly Lot Code
n.n	Silicon Revision
yyww	Date Code

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SPI Timing

Table 18. SPI Timing

Parameter	Test Conditions ¹	Min	Max	Unit
t_{DSU}	CSDA to CSCL setup time	20		ns
t_{DHO}	CSCL to CSDA hold time	20		ns
t_{SCH}	CSCL pulse width high	20		ns
t_{SCL}	CSCL pulse width low	20		ns
t_{SCS}	CSCL rising edge to CSB rising edge	60		ns
t_{CSS}	CSB rising to CSCL rising	20		ns
t_{CSH}	CSB pulse width high	20		ns
t_{CSL}	CSB pulse width low	20		ns
t_{PS}	Pulse width of spikes to be suppressed	0	5	ns

¹ AVDD, HPVDD, $V_{DDEXT} = 3.3$ V, AGND = 0 V, $T_A = +25^\circ\text{C}$, Slave Mode, $f_s = 48$ kHz, XTI/CODEC_MCLK = $256 \times f_s$ unless otherwise stated.

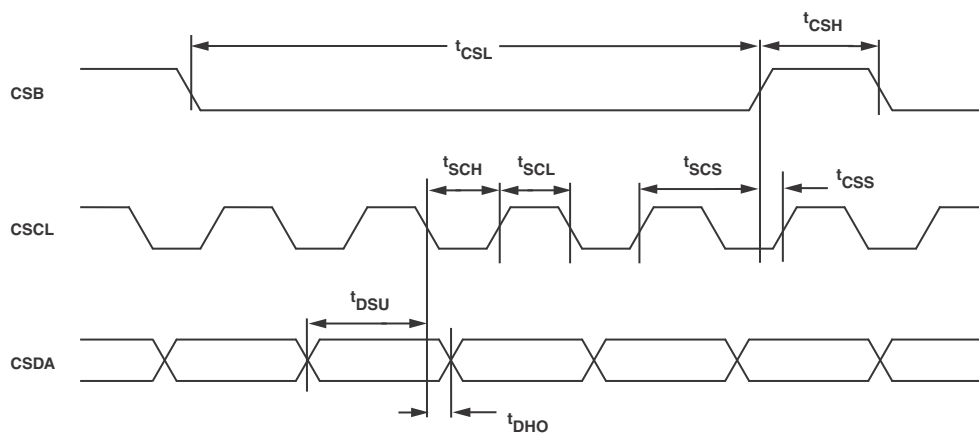


Figure 19. SPI Timing

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Digital Audio Interface Slave Mode Timing

Table 19. Digital Audio Interface Slave Mode Timing

Parameter	Test Conditions ¹	Min	Max	Unit
t_{DS}	DACDAT setup time from CODEC_BCLK rising edge	10		ns
t_{DH}	DACDAT hold time from CODEC_BCLK rising edge	10		ns
t_{LRSU}	ADCLRC/DACLRC setup time to CODEC_BCLK rising edge	10		ns
t_{LRH}	ADCLRC/DACLRC hold time to CODEC_BCLK rising edge	10		ns
t_{DD}	ADCDAT propagation delay from CODEC_BCLK falling edge (external load of 70 pF)		30	ns
t_{BCH}	CODEC_BCLK pulse width high	25		ns
t_{BCL}	CODEC_BCLK pulse width low	25		ns
t_{BCY}	CODEC_BCLK cycle time	50		ns

¹ AVDD, HPVDD, $V_{DDEXT} = 3.3$ V, AGND = 0 V, $T_A = +25^\circ\text{C}$, Slave Mode, $f_s = 48$ kHz, XTI/CODEC_MCLK = $256 \times f_s$ unless otherwise stated.

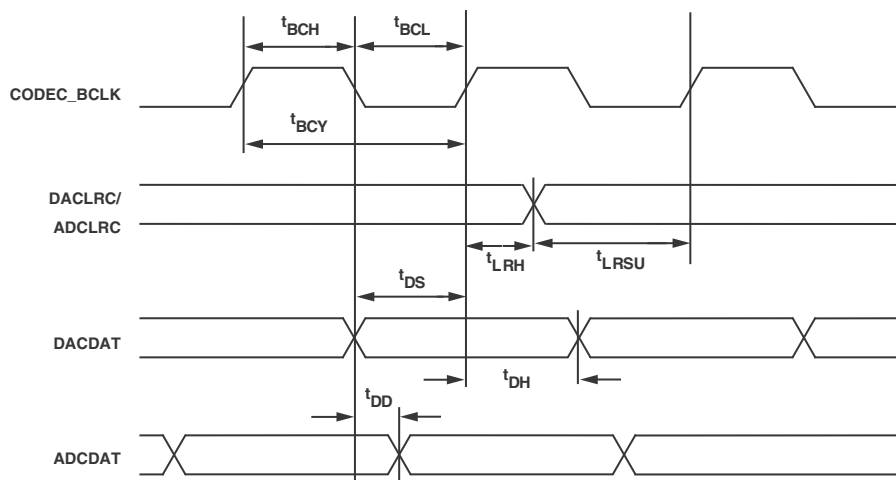


Figure 20. Digital Audio Interface Slave Mode Timing

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Digital Filter Characteristics

Table 22. Digital Filter Characteristics

Parameter	Conditions	Min	Typical	Max	Unit
ADC FILTER					
Pass Band	± 0.04 dB	0		$0.445 \times f_s$	Hz
	-6 dB		$0.5 \times f_s$		Hz
Pass Band Ripple				± 0.04	dB
Stop Band		$0.555 \times f_s$			Hz
Stop Band Attenuation	$f > 0.567 \times f_s$	-61			dB
High-Pass Filter Corner Frequency	-3 dB		3.7		Hz
	-0.5 dB		10.4		Hz
	-0.1 dB		21.6		Hz
DAC FILTER					
Pass Band	± 0.04 dB	0		$0.445 \times f_s$	Hz
	-6 dB		$0.5 \times f_s$		Hz
Pass Band Ripple				± 0.04	dB
Stop Band		$0.555 \times f_s$			Hz
Stop Band Attenuation	$f > 0.565 \times f_s$	-61			dB
Codec Clock Tolerance					
Frequency Range		8.0		13.8	MHz
Jitter Tolerance			50		pS

CONVERTER FILTER RESPONSE

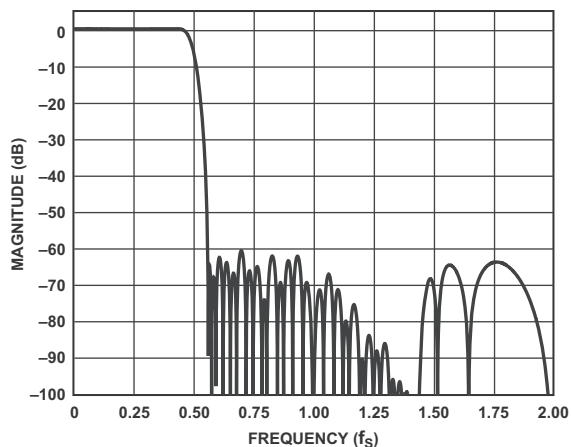


Figure 23. ADC Digital Filter Frequency Response, Sampling Rate = 48 kHz

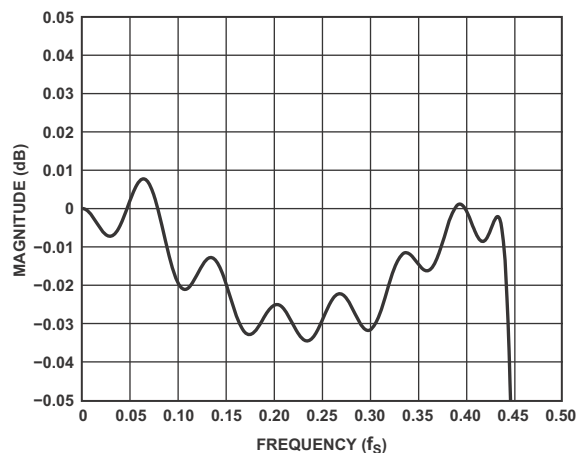


Figure 24. ADC Digital Filter Ripple, Sampling Rate = 48 kHz

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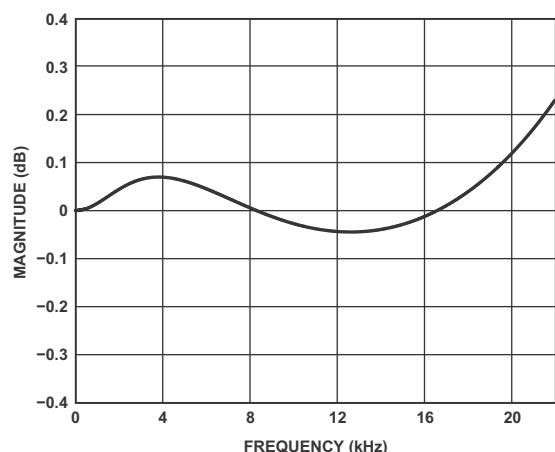


Figure 31. De-Emphasis Error, Sampling Rate = 44.1 kHz

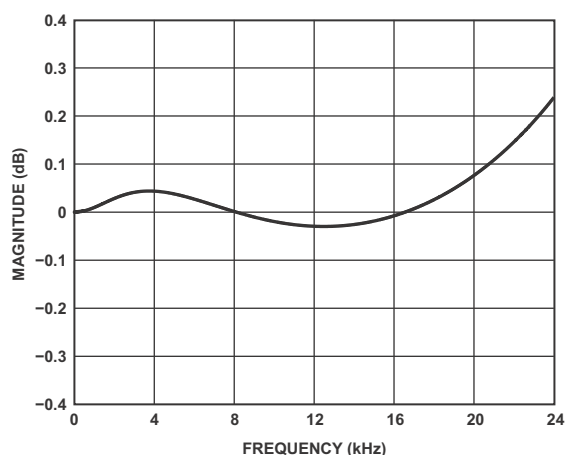


Figure 32. De-Emphasis Error, Sampling Rate = 48 kHz

289-BALL CSP_BGA BALL ASSIGNMENT

Signals added or changed to the ADSP-BF52xC processor for the embedded codec are shown in Table 23 and Table 24. Please refer to the published ADSP-BF52x processor data sheet for descriptions of additional signals for the processor.

Table 23. 289-Ball CSP_BGA Ball Assignment (Alphabetically)

Signal	Ball No.	Signal	Ball No.
ADCDAT	A16	HPGND	G17
ADCLRC	A15	HPVDD	G16 ¹
AGND	H22	LHPOUT	B20
AVDD	J22 ¹	LLINEIN	E23
CMODE	E22	LOUT	F22
CODEC_BCLK	A19	MICBIAS	H23
CODEC_CLKOUT	D22	MICIN	J23
CSB	D23	RHPOUT	B21
CSCL	B23	RLINEIN	F23
CSDA	C23	ROUT	G22
CVDD	H17 ¹	VMID	G23
DACDAT	A18	XTI/CODEC_MCLK	A22
DACLRC	A17	XTO	A21

¹ For ADSP-BF52x processor (without internal codec) compatibility, connect this ball to V_{DDEXT}.

Table 24. 289-Ball CSP_BGA Ball Assignment (Numerically)

Ball No.	Signal	Ball No.	Signal
A15	ADCLRC	E22	CMODE
A16	ADCDAT	E23	LLINEIN
A17	DACLRC	F22	LOUT
A18	DACDAT	F23	RLINEIN
A19	CODEC_BCLK	G16 ¹	HPVDD
A21	XTO	G17	HPGND
A22	XTI/CODEC_MCLK	G22	ROUT
B20	LHPOUT	G23	VMID
B21	RHPOUT	H17 ¹	CVDD
B23	CSCL	H22	AGND
C23	CSDA	H23	MICBIAS
D22	CODEC_CLKOUT	J22 ¹	AVDD
D23	CSB	J23	MICIN

¹ For ADSP-BF52x processor (without internal codec) compatibility, connect this ball to V_{DDEXT}.

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Figure 34 shows the bottom view of the ADSP-BF52xC processor ball configuration.

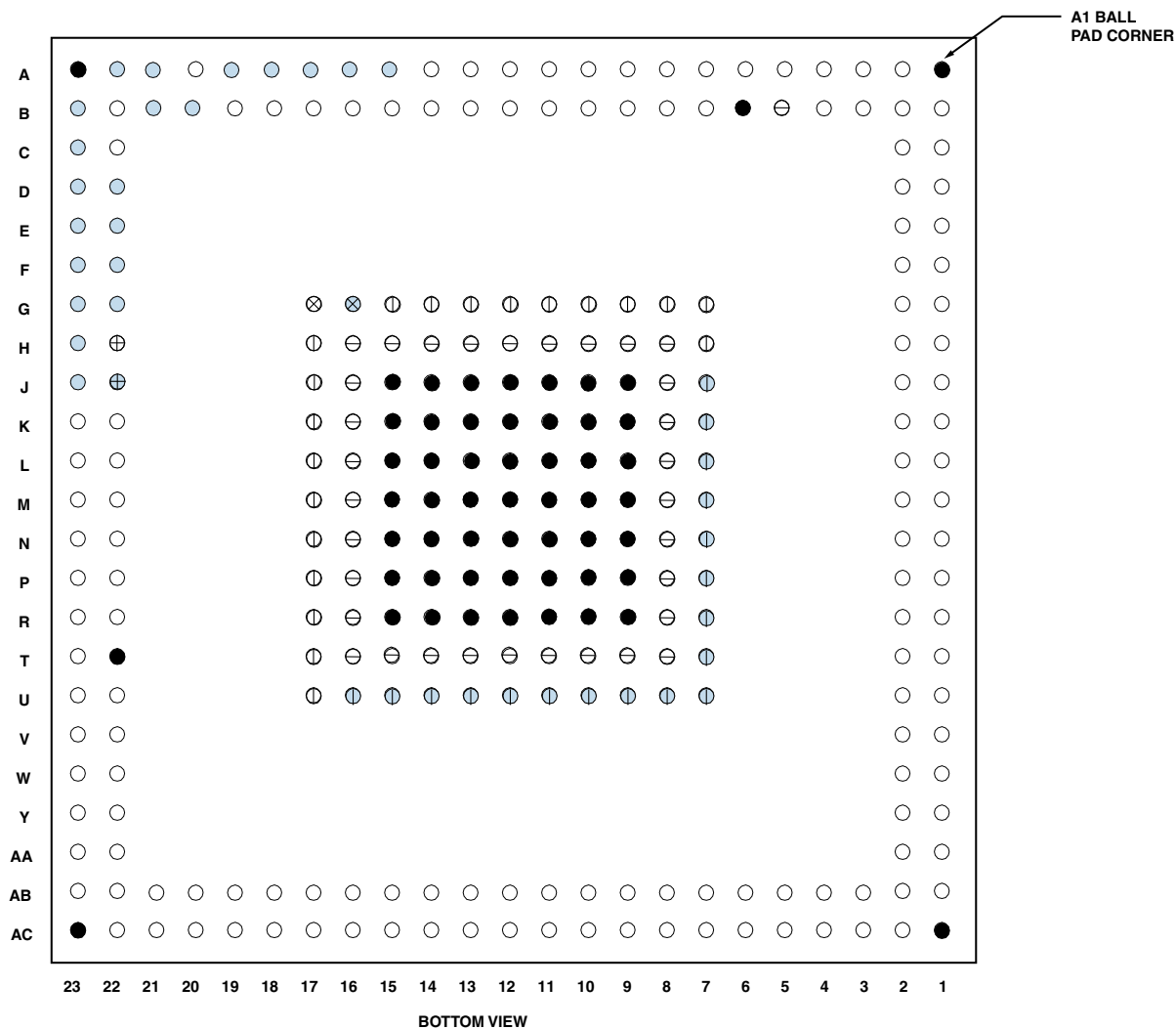


Figure 34. ADSP-BF52xC Processor Ball Configuration (Bottom View)