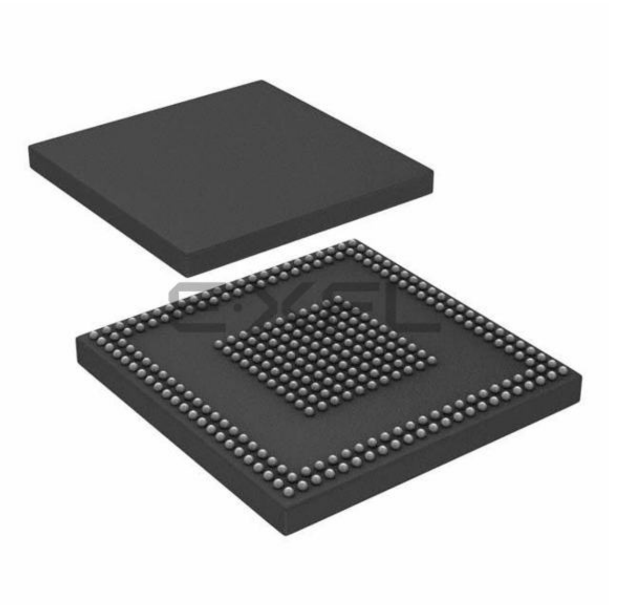

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	DMA, I²C, PPI, SPI, SPORT, UART, USB
Clock Rate	400MHz
Non-Volatile Memory	ROM (32kB)
On-Chip RAM	132kB
Voltage - I/O	1.8V, 2.5V, 3.3V
Voltage - Core	1.30V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	289-LFBGA, CSPBGA
Supplier Device Package	289-CSPBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf524kbcz-4c2

To allow an external device to generate the central reference clock, apply the external clock signal directly through the XTI/CODEC_MCLK input pin. In this configuration, the oscillator circuit of the codec can be powered down by using the OSCPD bit (Register R6, Bit D5) to reduce power consumption.

To accommodate applications with very high frequency master clocks, the internal core reference clock of the codec can be set to either CODEC_MCLK or CODEC_MCLK divided by 2. This is enabled by adjusting the setting of the CLKDIV2 bit (Register R8, Bit D6). The CODEC_CLKOUT pin can also drive external clock sources with either the codec clock signal or codec clock divided by 2 by enabling the CLKODIV2 bit (Register R8, Bit D7).

ADC AND DAC

The codec contains a pair of oversampling Σ-Δ ADCs. The maximum ADC full-scale input level is 1.0 V_{rms} when AVDD = 3.3 V. If the input signal to the ADC exceeds this level, data overloading occurs and causes audible distortion.

The ADC can accept analog audio input from either the stereo line inputs or the monaural microphone input. Note that the ADC can only accept input from a single source, so the programmer must choose either the line inputs or the microphone input using the INSEL bit (Register R4, Bit D2). The digital data from the ADC output, once converted, is processed using the ADC filters.

Complementary to the Σ-Δ ADC channels, the codec contains a pair of oversampling DACs that convert the digital audio data from the internal DAC filters into an analog audio signal. The DAC output can also be muted by setting the DACMU bit (Register R5, Bit D3) in the control register.

ADC HIGH-PASS AND DAC DE-EMPHASIS FILTERS

The ADC and DAC employ separate digital filters that perform 24-bit signal processing. The digital filters are used for both record and playback modes and are optimized for each individual sampling rate used.

For recording mode operations, the unprocessed data from the ADC enters the ADC filters and is converted to the appropriate sampling frequency, then is output to the digital audio interface.

For playback mode operations, the DAC filters convert the digital audio interface data to oversampled data using a sampling rate selected by the programmer. The oversampled data is processed by the DAC and sent to the analog output mixer by enabling the DACSEL (Register R4, Bit D4).

Programmers have the option of setting up the device so that any dc offset in the input source signal is automatically detected and removed. To accomplish this, enable the digital high-pass filter (see Table 22 on Page 30 for characteristics) contained in the ADC digital filters by using the ADCHPD bit (Register R5, Bit D0).

In addition, programmers can implement digital de-emphasis by using the DEEMPH bits (Register R5, Bit D1 and Bit D2).

ANALOG AUDIO INTERFACES

The codec includes stereo single-ended line inputs and a monaural microphone input to the on-board ADC. Either the line inputs or the microphone input, but not both simultaneously, can be connected to the ADC by setting the INSEL bit (Register R4, Bit D2).

The codec also includes line and headphone outputs from the on-board DAC. The line or microphone inputs can be routed and mixed directly to the output terminals.

Stereo Line and Monaural Microphone Inputs

The single-ended stereo line inputs (RLINEIN and LLINEIN) are internally biased to VMID by way of a voltage divider between AVDD and AGND (see Figure 2). The line input signal can be connected to the internal ADC and, if desired, routed directly to the outputs via the bypass path by using the BYPASS bit (Register R4, Bit D3).

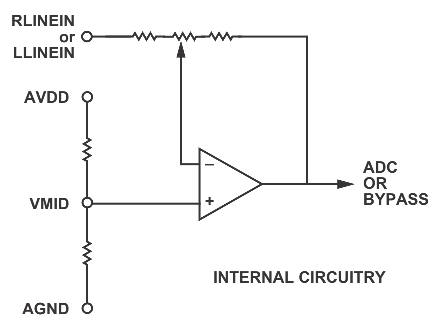

Figure 2. Line Input to ADC

The line input volume can be adjusted from –34.5 dB to +33 dB in steps of +1.5 dB by setting the LINVOL (Register R0, Bit D0 to Bit D5) and RINVOL (Register R1, Bit D0 to Bit D5) bits. By default the volume is independently adjustable for both right and left line inputs. However, if the LRINBOTH or RLINBOTH bit is programmed, both LINVOL and RINVOL are loaded with the same value. The programmer can also set the LINMUTE (Register R0, Bit D7) and RINMUTE (Register R1, Bit D7) bits to mute the line input signal to the ADC.

The high impedance, low capacitance monaural microphone input pin (MICIN, shown in Figure 3) has two gain stages and a microphone bias level (MICBIAS) that is internally biased to the VMID voltage level by way of a voltage divider between AVDD and AGND. The microphone input signal can be connected to the internal ADC and, if desired, routed directly to the outputs via the sidetone path by using the SIDETONE bit (Register R4, Bit D5).

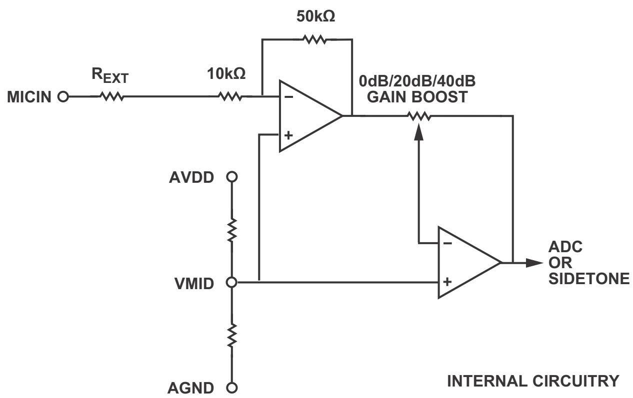

Figure 3. Microphone Input to ADC

The first gain stage is composed of a low noise operational amplifier set to an inverting configuration with integrated 50 kΩ feedback and 10 kΩ input resistors. The default microphone input signal gain is 14 dB. An external resistor (R_{EXT}) can be connected in series with the MICIN pin to reduce the first-stage gain of the microphone input signal to as low as 0 dB by using the following equation:

Microphone Input Gain = 50 kΩ/(10 kΩ + R_{EXT})

The second-stage gain of the microphone signal path is derived from the internal microphone boost circuitry. The available settings are 0 dB, 20 dB, and 40 dB and are controlled by the MICBOOST (Register R4, Bit D0) and MICBOOST2 (Register R4, Bit D8) bits. To achieve 20 dB of secondary gain boost, the programmer can select either MICBOOST or MICBOOST2. To achieve 40 dB of secondary microphone signal gain, the programmer must select both MICBOOST and MICBOOST2.

The MUTEMIC bit (Register R4, Bit D1) mutes the microphone input signal to the ADC.

When using either the line or microphone inputs, the maximum full-scale input to the ADC is 1.0 V rms when AVDD = 3.3 V. Do not apply an input voltage larger than full-scale to avoid overloading the ADC, which causes distortion of sound and deterioration of audio quality. For best sound quality in both microphone and line inputs, gain should be carefully configured so that the ADC receives a signal equal to its full-scale. This maximizes the signal-to-noise ratio for best total audio quality.

Bypass and Sidetone Paths to Output

The line and microphone inputs can be routed and mixed directly to the output terminals by programming the SIDETONE (Register R4, Bit D5) and BYPASS (Register R4, Bit D3) registers. In both modes, the analog input signal is routed directly to the output terminals and is not digitally converted. The bypass signal at the output mixer is the same level as the output of the PGA associated with each line input.

The sidetone signal at the output mixer can be attenuated from −6 dB to −15 dB in steps of −3 dB by configuring the SIDEATT (Register R4, Bit D6 and Bit D7) control register bits. The selected level of attenuation occurs after the initial microphone signal amplification from the microphone first and second stage gains.

Line and Headphone Outputs

The DAC outputs, the microphone (the sidetone path), and the line inputs (the bypass path) are summed at an output mixer (see Figure 4). This output signal is then applied to both the stereo line outputs and stereo headphone outputs.

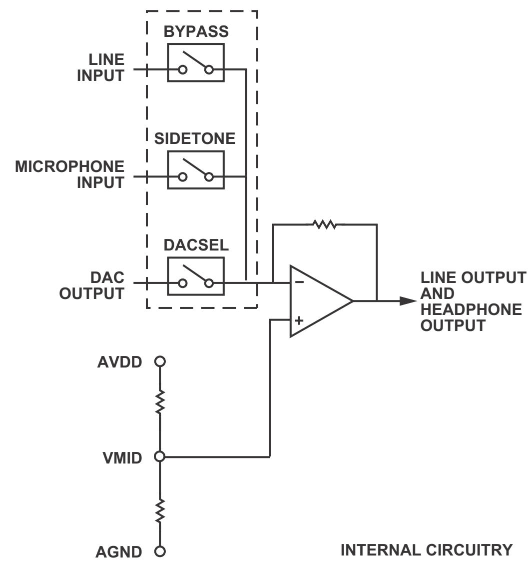

Figure 4. Output Signal Chain

The codec has a set of efficient headphone amplifier outputs, LHPOUT and RHPOUT, that are able to drive 16 Ω or 32 Ω headphones (shown in Figure 5).

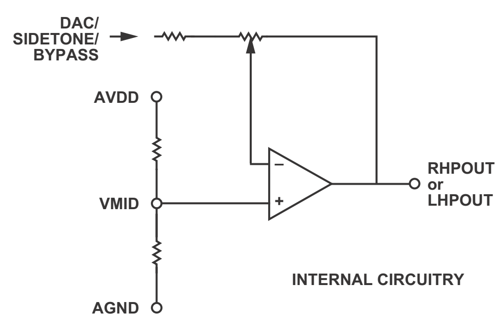

Figure 5. Headphone Output

Like the line inputs, the LHPOUT and RHPOUT volumes, by default, are independently adjusted by setting the LHPVOL (Register R2, Bit D0 to Bit D6) and RHPVOL (Register R3, Bit D0 to Bit D6) bits of the headphone output control registers. The headphone outputs can be muted by writing codes less than 0110000 to the LHPVOL and RHPVOL bits.

The programmer can simultaneously load the volume control of both channels by writing to the LRHPBOTH (Register R2, Bit D8) and RLHPBOTH (Register R3, Bit D8) bits of the left- or right-channel DAC volume registers.

The maximum output level of the headphone outputs is 1.0 V rms when AVDD and HPVDD = 3.3 V. To suppress audible pops and clicks, the headphone and line outputs are held at the VMID dc voltage level when the device is set to standby mode or when the headphone outputs are muted.

The stereo line outputs of the codec, the LOUT and ROUT pins, can drive a load impedance of 10 kΩ and 50 pF. The line output signal levels are not adjustable at the output mixer, which has a fixed gain of 0 dB. The maximum output level of the line outputs is 1.0 V rms when AVDD = 3.3 V.

DIGITAL AUDIO INTERFACE

The digital audio input can support the following digital audio communication protocols: right-justified mode, left-justified mode, I^2S mode, and frame sync mode. See Figure 6 on Page 6 through Figure 10 on Page 7.

The mode selection is performed by writing to the FORMAT bits of the digital audio interface register (Register R7, Bit D1 and Bit D0). All modes are MSB first and operate with data of 16 to 32 bits.

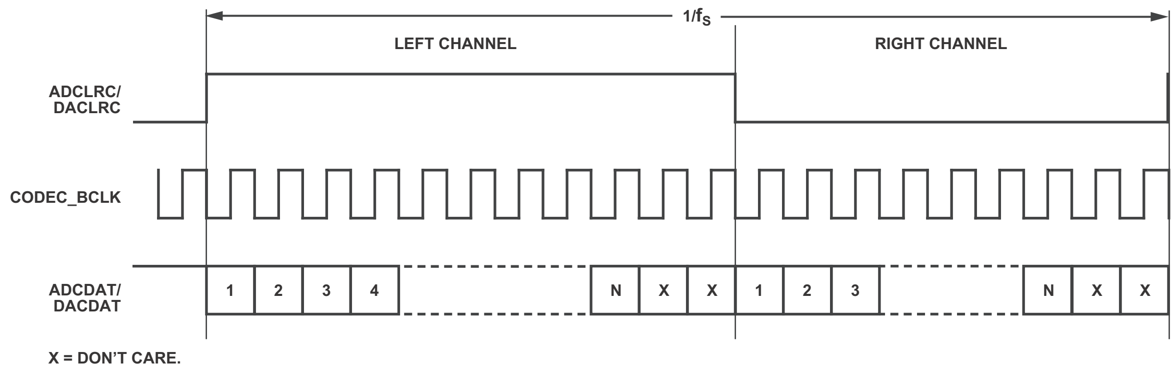

Figure 6. Left-Justified Audio Input Mode

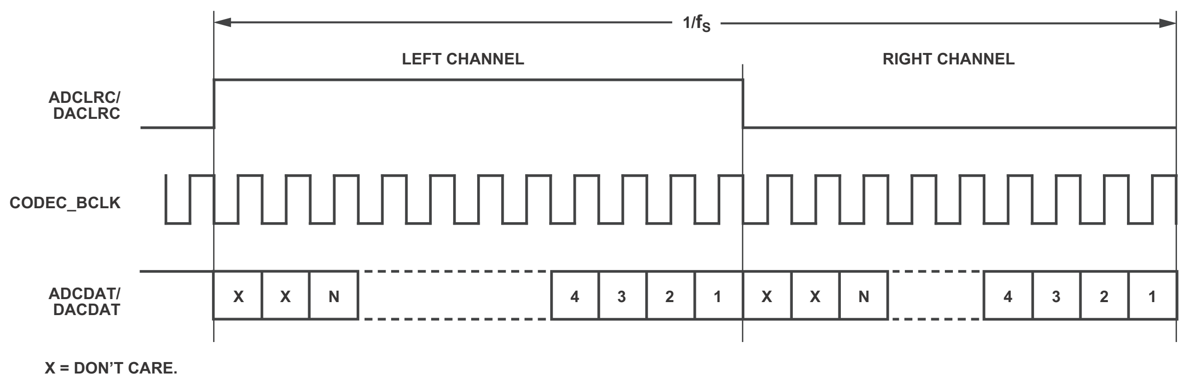

Figure 7. Right-Justified Audio Input Mode

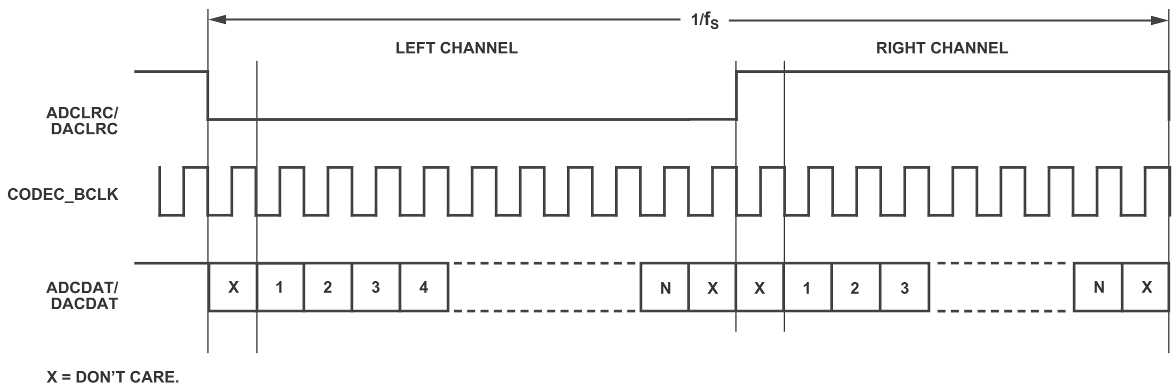

Figure 8. I^2S Audio Input Mode

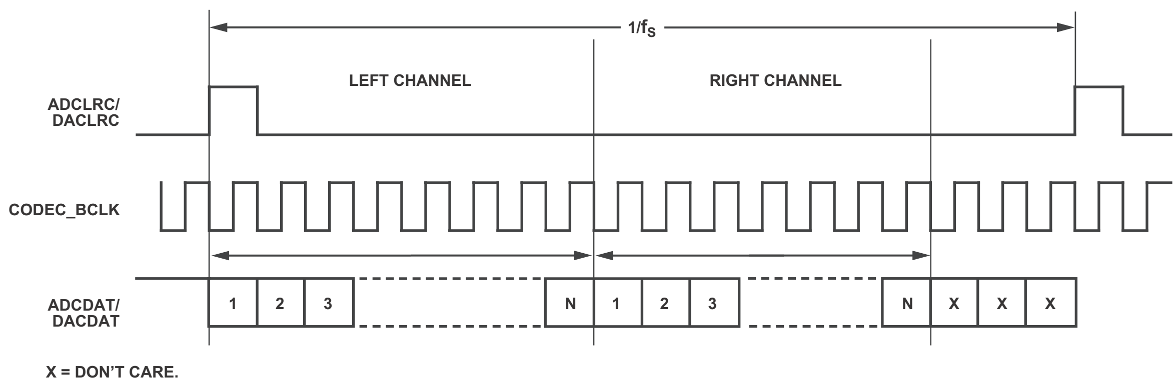

Figure 9. Frame Sync/PCM Mode Audio Input (Submode 1) [Bit LRP = 0]

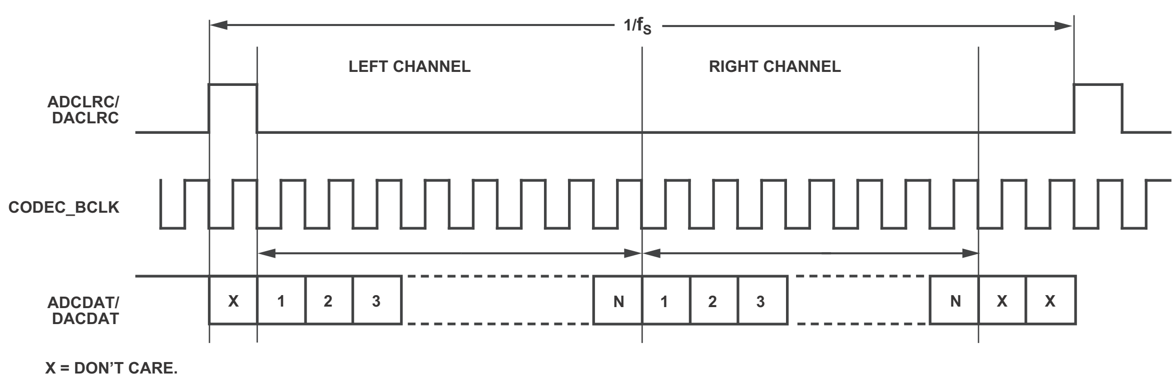

Figure 10. Frame Sync/PCM Mode Audio Input (Submode 2) [Bit LRP = 1]

Normal Mode

In normal mode, the codec supports digital audio sampling rates from 8 kHz to 96 kHz. Normal mode supports 256 × f_S and 384 × f_S based clocks. To select the desired sampling rate, the programmer must set the appropriate sampling rate register in the SR control bits (Register R8, Bit D2 to Bit D5) and match this selection to the core clock frequency that is pulsed on the CODEC_MCLK pin. See Table 1 for sampling rates in normal mode.

Table 1. Sampling Rate Lookup Table, Normal Mode (USB Disabled)

CODEC_MCLK (CLKDIV2 = 0)	CODEC_MCLK (CLKDIV2 = 1)	ADC Sampling Rate (ADCLRC)	DAC Sampling Rate (DACLRC)	USB	SR [3:0]	BOSR	CODEC_BCLK (MS = 1)[1]
12.288 MHz	24.576 MHz	8 kHz (CODEC_MCLK/1536)	8 kHz (CODEC_MCLK/1536)	0	0011	0	CODEC_MCLK/4
		8 kHz (CODEC_MCLK/1536)	48 kHz (CODEC_MCLK/256)	0	0010	0	CODEC_MCLK/4
		12 kHz (CODEC_MCLK/1024)	12 kHz (CODEC_MCLK/1024)	0	0100	0	CODEC_MCLK/4
		16 kHz (CODEC_MCLK/768)	16 kHz (CODEC_MCLK/768)	0	0101	0	CODEC_MCLK/4
		24 kHz (CODEC_MCLK/512)	24 kHz (CODEC_MCLK/512)	0	1110	0	CODEC_MCLK/4
		32 kHz (CODEC_MCLK/384)	32 kHz (CODEC_MCLK/384)	0	0110	0	CODEC_MCLK/4
		48 kHz (CODEC_MCLK/256)	8 kHz (CODEC_MCLK/1536)	0	0001	0	CODEC_MCLK/4
		48 kHz (CODEC_MCLK/256)	48 kHz (CODEC_MCLK/256)	0	0000	0	CODEC_MCLK/4
		96 kHz (CODEC_MCLK/128)	96 kHz (CODEC_MCLK/128)	0	0111	0	CODEC_MCLK/2
11.2896 MHz	22.5792 MHz	8.0182 kHz (CODEC_MCLK/1408)	8.0182 kHz (CODEC_MCLK/1408)	0	1011	0	CODEC_MCLK/4
		8.0182 kHz (CODEC_MCLK/1408)	44.1 kHz (CODEC_MCLK/256)	0	1010	0	CODEC_MCLK/4
		11.025 kHz (CODEC_MCLK/1024)	11.025 kHz (CODEC_MCLK/1024)	0	1100	0	CODEC_MCLK/4
		22.05 kHz (CODEC_MCLK/512)	22.05 kHz (CODEC_MCLK/512)	0	1101	0	CODEC_MCLK/4
		44.1 kHz (CODEC_MCLK/256)	8.0182 kHz (CODEC_MCLK/1408)	0	1001	0	CODEC_MCLK/4
		44.1 kHz (CODEC_MCLK/256)	44.1 kHz (CODEC_MCLK/256)	0	1000	0	CODEC_MCLK/4
		88.2 kHz (CODEC_MCLK/128)	88.2 kHz (CODEC_MCLK/128)	0	1111	0	CODEC_MCLK/2
18.432 MHz	36.864 MHz	8 kHz (CODEC_MCLK/2304)	8 kHz (CODEC_MCLK/2304)	0	0011	1	CODEC_MCLK/6
		8 kHz (CODEC_MCLK/2304)	48 kHz (CODEC_MCLK/384)	0	0010	1	CODEC_MCLK/6
		12 kHz (CODEC_MCLK/1536)	12 kHz (CODEC_MCLK/1536)	0	0100	1	CODEC_MCLK/6
		16 kHz (CODEC_MCLK/1152)	16 kHz (CODEC_MCLK/1152)	0	0101	1	CODEC_MCLK/6
		24 kHz (CODEC_MCLK/768)	24 kHz (CODEC_MCLK/768)	0	1110	1	CODEC_MCLK/6
		32 kHz (CODEC_MCLK/576)	32 kHz (CODEC_MCLK/576)	0	0110	1	CODEC_MCLK/6
		48 kHz (CODEC_MCLK/384)	48 kHz (CODEC_MCLK/384)	0	0000	1	CODEC_MCLK/6
		48 kHz (CODEC_MCLK/384)	8 kHz (CODEC_MCLK/2304)	0	0001	1	CODEC_MCLK/6
		96 kHz (CODEC_MCLK/192)	96 kHz (CODEC_MCLK/192)	0	0111	1	CODEC_MCLK/3
16.9344 MHz	33.8688 MHz	8.0182 kHz (CODEC_MCLK/2112)	8.0182 kHz (CODEC_MCLK/2112)	0	1011	1	CODEC_MCLK/6
		8.0182 kHz (CODEC_MCLK/2112)	44.1 kHz (CODEC_MCLK/384)	0	1010	1	CODEC_MCLK/6
		11.025 kHz (CODEC_MCLK/1536)	11.025 kHz (CODEC_MCLK/1536)	0	1100	1	CODEC_MCLK/6
		22.05 kHz (CODEC_MCLK/768)	22.05 kHz (CODEC_MCLK/768)	0	1101	1	CODEC_MCLK/6
		44.1 kHz (CODEC_MCLK/384)	8.0182 kHz (CODEC_MCLK/2112)	0	1001	1	CODEC_MCLK/6
		44.1 kHz (CODEC_MCLK/384)	44.1 kHz (CODEC_MCLK/384)	0	1000	1	CODEC_MCLK/6
		88.2 kHz (CODEC_MCLK/192)	88.2 kHz (CODEC_MCLK/192)	0	1111	1	CODEC_MCLK/3

[1] CODEC_BCLK frequency is for master mode and slave right-justified mode only.

SOFTWARE CONTROL INTERFACE

The software control interface provides access to the programmer-selectable control registers and can operate with a 2-wire (TWI) or 3-wire (SPI) interface, depending on the setting of the CMODE pin. If the CMODE pin is set to 0, the 2-wire interface is selected; if 1, the 3-wire interface is selected.

Within each control register is a control data-word consisting of 16 bits, MSB first. Bit B15 to Bit B9 are the register map address, and Bit B8 to Bit B0 are register data for the associated register map.

When 2-wire (TWI) mode is selected, CSDA generates the serial control data-word; CSCL clocks the serial data; and CSB determines the TWI device address. If the CSB pin is set to 0, the address selected is 0011010; if 1, the address is 0011011.

When 3-wire (SPI) mode is selected, CSDA generates the control data-word, CSCL clocks the control data-word into the codec, and CSB latches in the control data-word.

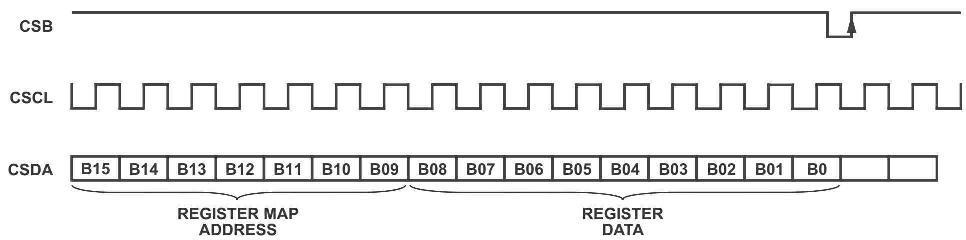

Figure 11. Codec SPI Serial Interface

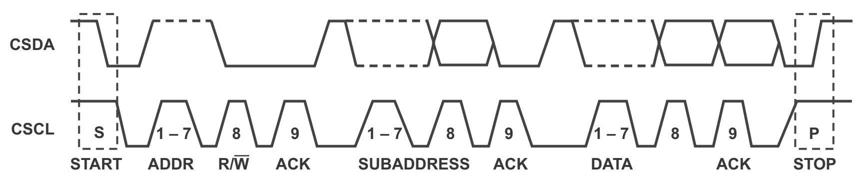

Figure 12. Codec TWI Serial Interface

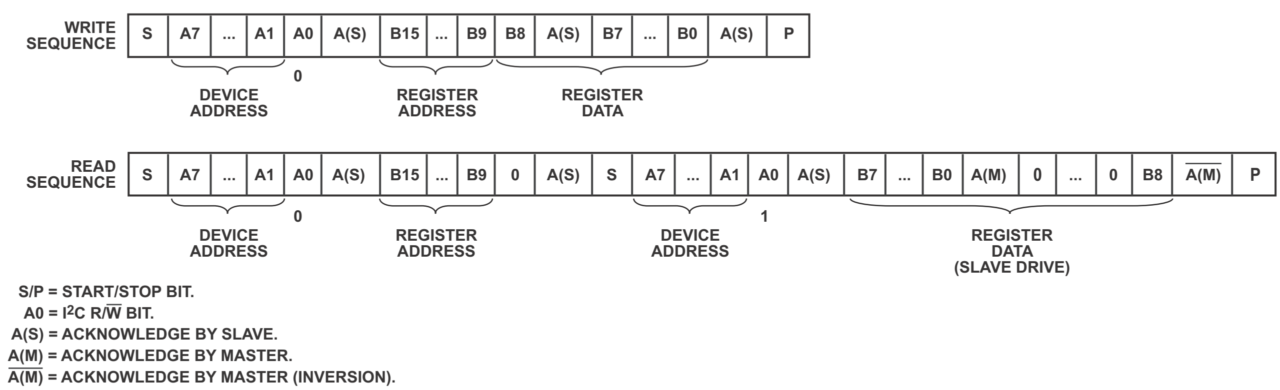

Figure 13. Codec TWI Write and Read Sequences

Figure 14 on Page 13 and Figure 15 on Page 14 describe alternative external connections for SPI or TWI control of the ADSP-BF52xC codec. The figures are the same except for the shaded area in each.

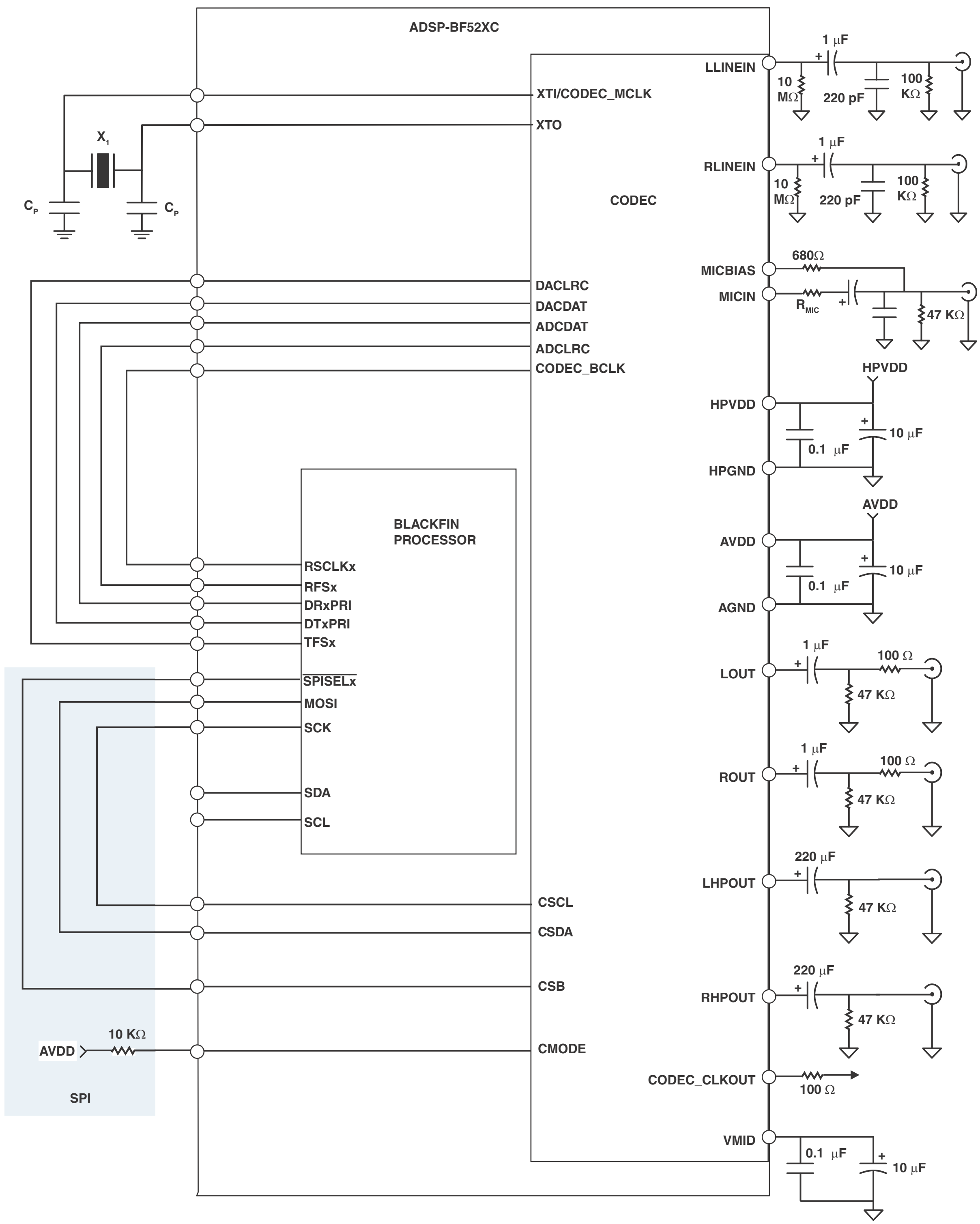

Figure 14. Recommended Application Circuit Using SPI Control

BIT DESCRIPTIONS

Table 4 through Table 14 on Page 20 describe each bit in the control registers.

Table 4. Register 0 Left-Channel ADC Input Volume

Bit Name	Bits	Description	Settings
LRINBOTH	B8	Left-to-right line input ADC data load control	0 = disable simultaneous loading of left-channel ADC data to right-channel register (default)
			1 = enable simultaneous loading of left-channel ADC data to right-channel register
LINMUTE	B7	Left-channel input mute	0 = disable mute
			1 = enable mute on data path to ADC (default)
LINVOL	B[5:0]	Left-channel PGA volume control	00 0000 = −34.5 dB
			… 1.5 dB step up
			01 0111 = 0 dB (default)
			… 1.5 dB step up
			01 1111 = 12 dB
			10 0000 = 13.5 dB
			10 0001 = 15 dB
			10 0010 = 16.5 dB
			10 0011 = 18 dB
			10 0100 = 19.5 dB
			10 0101 = 21 dB
			10 0110 = 22.5 dB
			10 0111 = 24 dB
			10 1000 = 25.5 dB
			10 1001 = 27 dB
			10 1010 = 28.5 dB
			10 1011 = 30 dB
			10 1100 = 31.5 dB
			10 1101 = 33 dB
			11 1111 to 10 1101 = 33 dB

Table 11. Register 7 Digital Audio I/F

Bit Name	Bits	Description	Settings
BCLKINV	B7	CODEC_BCLK inversion control	0 = CODEC_BCLK not inverted (default)
			1 = CODEC_BCLK inverted
MS	B6	Master mode enable	0 = enable slave mode (default)
			1 = enable master mode
LRSWAP	B5	Swap DAC data control	0 = output left- and right-channel data as normal (default)
			1 = swap left- and right-channel DAC data in audio interface
LRP	B4	Polarity control for clocks in right-justified, left-justified, and I^2S modes	0 = normal DACLRC and ADCLRC (default), or processor Submode 1
			1 = invert DACLRC and ADCLRC polarity, or processor Submode 2
WL [1:0]	B[3:2]	Data-word length control	00 = 16 bits
			01 = 20 bits
			10 = 24 bits (default)
			11 = 32 bits
FORMAT [1:0]	B[1:0]	Digital audio input format control	00 = right justified
			01 = left justified
			10 = I^2S mode (default)
			11 = processor mode

Table 12. Register 8 Sampling Rate

Bit Name	Bits	Description	Settings
CLKODIV2	B7	CODEC_CLKOUT divider select	0 = CODEC_CLKOUT is codec clock (default)
			1 = CODEC_CLKOUT is codec clock divided by 2
CLKDIV2	B6	Codec clock divide select	0 = codec clock is CODEC_MCLK (default)
			1= codec clock is CODEC_MCLK divided by 2
SR [3:0]	B[5:2]	Clock setting condition	See Table 1 on Page 9 and Table 2 on Page 10
BOSR	B1	Base oversampling rate	USB mode:
			0 = support for 250 × f_S based clock (default)
			1 = support for 272 × f_S based clock
			Normal mode:
			0 = support for 256 × f_S based clock (default)
			1 = support for 384 × f_S based clock
USB	B0	USB mode select	0 = normal mode enable (default)
			1 = USB mode enable

Table 13. Register 9 Active

Bit Name	Bit	Description	Settings
ACTIVE	B0	Digital core activation control	0 = disable digital core (default)
			1 = activate digital core

Table 14. Register 10 Software Reset

Bit Name	Bit	Description	Settings
RESET [8:0]	B[8:0]	Write all 0s to this register to set all registers to their default settings. Other data written to this register has no effect.	0 = reset (default)

SPECIFICATIONS

$T_{Ambient}$ = 25°C, AVDD = VDDEXT = 3.3 V, HPVDD = 3.3 V, 1 kHz signal, f_S = 48 kHz, PGA gain = 0 dB, 24-bit audio data, unless otherwise noted.

OPERATING CONDITIONS

See operating conditions in the published ADSP-BF52xC data sheet.

Parameter	Conditions	Min	Typical	Max	Unit
AVDD[1]		1.8	3.3	3.6	V
HPVDD		1.8	3.3	3.6	V

[1] Note that AVDD must equal HPVDD.

CODEC ELECTRICAL CHARACTERISTICS

Parameter	Conditions	Min	Typical	Max	Unit
Line Input					
Input Signal Level (0 dB)			AVDD/3.3		V(rms)
Input Impedance	PGA gain = 0 dB		200		kΩ
	PGA gain = +33 dB		10		kΩ
	PGA gain = –34.5 dB		480		kΩ
Input Capacitance			10		pF
Signal-to-Noise Ratio (A-Weighted)	PGA gain = 0 dB, AVDD = 3.3 V	82	87		dB
	PGA gain = 0 dB, AVDD = 1.8 V		84		dB
Total Harmonic Distortion (THD)	–1 dBFS input, AVDD = 3.3 V	–80	–84		dB
	–1 dBFS input, AVDD = 1.8 V		–71	–60	dB
Channel Separation[1]			80		dB
Programmable Gain		–34.5	0	+33.5	dB
Gain Step			1.5		dB
Mute Attenuation			–80		dB
Microphone Input					
Input Signal Level			1		V(rms)
Signal-to-Noise Ratio (A-Weighted)	Microphone gain = 0 dB (R_{SOURCE} = 40 kΩ)		85		dB
Total Harmonic Distortion	–1 dBFS input, 0 dB gain, AVDD = 3.3 V		–75		dB
	–1 dBFS input, 0 dB gain, AVDD = 1.8 V		–65		dB
Power Supply Rejection Ratio			50		dB
Mute Attenuation			80		dB
Input Resistance			10		kΩ
Input Capacitance			10		pF
Microphone Bias					
Bias Voltage			0.75 × AVDD		V
Bias Current Source				3	mA
Noise in the Signal Bandwidth	20 Hz to 20 kHz		40		nV/√Hz

Parameter	Conditions	Min	Typical	Max	Unit
Line Output					
DAC	−1 dBFS input DAC + line output				
Full-Scale Output			AVDD/3.3		V(rms)
Signal-to-Noise Ratio (A-Weighted)	AVDD = 3.3 V	90	95		dB
	AVDD = 1.8 V	85	88		dB
THD + N	AVDD = 3.3 V		–80	–70	dB
	AVDD = 1.8 V		–80	–70	dB
Power Supply Rejection Ratio			50		dB
Channel Separation			80		dB
Headphone Output					
Full-Scale Output Voltage			AVDD/3.3		V(rms)
Maximum Output Power	R_L = 32 Ω		30		mW
	R_L = 16 Ω		60		mW
Signal-to-Noise Ratio (A-Weighted)	AVDD = 3.3 V	90	94		dB
	AVDD = 1.8 V	80	85		dB
THD + N	HPOUT = 10 mW		–65		dB
	HPOUT = 20 mW		–60		dB
Power Supply Rejection Ratio			50		dB
Mute Attenuation			80		dB
LIne Input To Line Output					
Full-Scale Output Voltage			AVDD/3.3		V(rms)
Signal-to-Noise Ratio (A-Weighted)	AVDD = 3.3 V		92		dB
	AVDD = 1.8 V		86		dB
Total Harmonic Distortion	AVDD = 3.3 V		–80		dB
	AVDD = 1.8 V		–80		dB
Power Supply Rejection			50		dB
Microphone Input To Headphone Output					
Full-Scale Output Voltage			AVDD/3.3		V(rms)
Signal-to-Noise Ratio (A-Weighted)	AVDD = 3.3 V		94		dB
	AVDD = 1.8 V		88		dB
Power Supply Rejection Ratio			50		dB
Programmable Attenuation		6		15	dB
Gain Step			3		dB
Mute Attenuation			80		dB

[1] Guaranteed but not tested.

POWER CONSUMPTION

These current consumption values are for the codec alone. Please refer to the published ADSP-BF52x processor data sheet for the additional current consumption of the Blackfin processor.

Table 16. Power Consumption

Mode	POWEROFF	CLKOUTPD	OSCPD	OUTPD	DACPD	ADCPD	MICPD	LINEINPD	(1.8V) AVDD	(1.8V) HPVDD	(1.8V) V_{DDEXT}[1]	(3.3V) AVDD	(3.3V) HPVDD	(3.3V) V_{DDEXT}[1]	Unit
Record and Playback	0	0	0	0	0	0	0	0	7.4	1.5	6.3	14.8	2.0	12.0	mA
Playback Only															
Oscillator Enabled	0	0	0	0	0	1	1	1	3.1	1.30	3.0	4.7	2.0	6.1	mA
External Clock	0	1	1	0	0	1	1	1	2.9	1.2	3.0	4.7	2.0	6.1	mA
Record Only															
Line Oscillator	0	0	0	1	1	0	1	0	2.4	N/A	3.7	4.3	N/A	7.4	mA
Line Clock	0	0	1	1	1	0	1	0	2.5	N/A	3.8	4.3	N/A	7.4	mA
Microphone 1	0	0	0	1	1	0	0	1	3.6	N/A	1.9	9.4	N/A	3.6	mA
Microphone 2	0	0	1	1	1	0	0	1	3.6	N/A	1.8	9.4	N/A	3.6	mA
Sidetone (Microphone-to-Headphone Output)															
Internally Generated Clock	0	0	0	0	1	1	0	1	2.3	1.0	2.0	7.9	2.0	4.0	mA
External Clock	0	0	1	0	1	1	0	1	2.3	1.0	2.0	7.9	2.0	4.0	mA
Analog Bypass (Line Input or Line Output)															
Internally Generated Line	0	0	0	0	1	1	1	0	0.9	1.0	2.0	1.8	2.0	4.0	mA
External Line	0	0	1	0	1	1	1	0	0.9	1.0	2.0	1.8	2.0	4.0	mA
Power-Down															
Clock Stopped	1	1	1	1	1	1	1	1	3.1	6.3	3.8	9.4	6.3	12.3	µA

[1] V_{DDEXT} here refers to the total of the codec's DCVDD and DBVDD signals and does not include VDDExt supplies in the Blackfin device.

TIMING SPECIFICATIONS

TWI Timing

Table 17. TWI Timing

Parameter		Test Conditions[1]	Min	Max	Unit
t_{SCS}	Start condition setup time		600		ns
t_{SCH}	Start condition hold time		600		ns
t_{PH}	CSCL pulse width high		600		ns
t_{PL}	CSCL pulse width low		1.3		µs
f_{SCL}	CSCL frequency		0	526	kHz
t_{DS}	Data setup time		100		ns
t_{DH}	Data hold time			900	ns
t_{RT}	CSDA and CSCL rise time			300	ns
t_{FT}	CSDA and CSCL fall time			300	ns
t_{HCS}	Stop condition setup time		600		ns

[1] AVDD, HPVDD, V_{DDEXT} = 3.3 V, AGND = 0 V, T_A = +25°C, Slave Mode, f_S = 48 kHz, XTI/CODEC_MCLK = 256 × f_S unless otherwise stated.

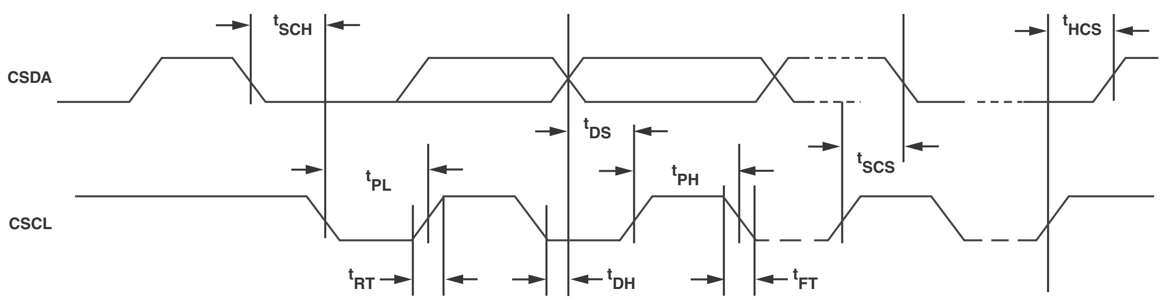

Figure 18. TWI Timing

SPI Timing

Table 18. SPI Timing

Parameter		Test Conditions[1]	Min	Max	Unit
t_{DSU}	CSDA to CSCL setup time		20		ns
t_{DHO}	CSCL to CSDA hold time		20		ns
t_{SCH}	CSCL pulse width high		20		ns
t_{SCL}	CSCL pulse width low		20		ns
t_{SCS}	CSCL rising edge to CSB rising edge		60		ns
t_{CSS}	CSB rising to CSCL rising		20		ns
t_{CSH}	CSB pulse width high		20		ns
t_{CSL}	CSB pulse width low		20		ns
t_{PS}	Pulse width of spikes to be suppressed		0	5	ns

[1] AVDD, HPVDD, V_{DDEXT} = 3.3 V, AGND = 0 V, T_A = +25°C, Slave Mode, f_S = 48 kHz, XTI/CODEC_MCLK = 256 × f_S unless otherwise stated.

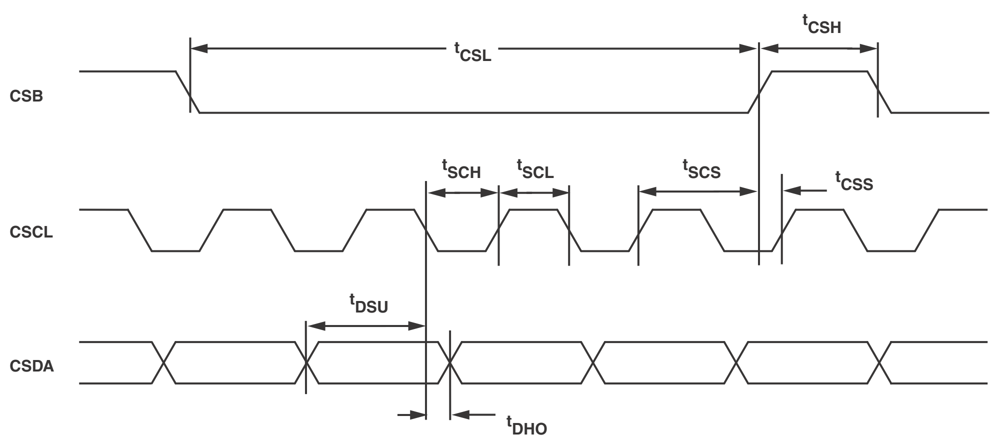

Figure 19. SPI Timing

Digital Filter Characteristics

Table 22. Digital Filter Characteristics

Parameter	Conditions	Min	Typical	Max	Unit
ADC FILTER					
Pass Band	±0.04 dB	0		$0.445 \times f_S$	Hz
	–6 dB		$0.5 \times f_S$		Hz
Pass Band Ripple				±0.04	dB
Stop Band		$0.555 \times f_S$			Hz
Stop Band Attenuation	$f > 0.567 \times f_S$	–61			dB
High-Pass Filter Corner Frequency	–3 dB		3.7		Hz
	–0.5 dB		10.4		Hz
	–0.1 dB		21.6		Hz
DAC FILTER					
Pass Band	±0.04 dB	0		$0.445 \times f_S$	Hz
	–6 dB		$0.5 \times f_S$		Hz
Pass Band Ripple				±0.04	dB
Stop Band		$0.555 \times f_S$			Hz
Stop Band Attenuation	$f > 0.565 \times f_S$	–61			dB
Codec Clock Tolerance					
Frequency Range		8.0		13.8	MHz
Jitter Tolerance			50		pS

CONVERTER FILTER RESPONSE

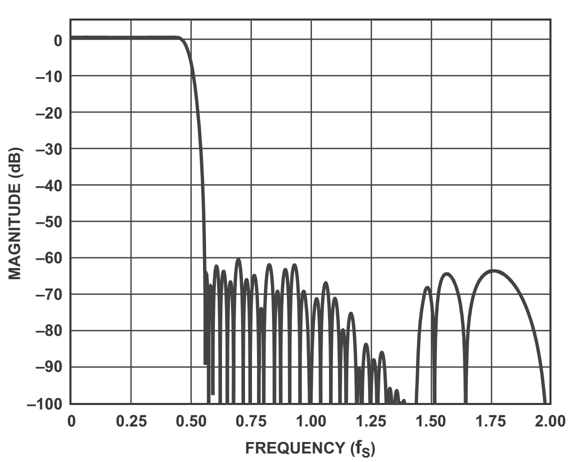

Figure 23. ADC Digital Filter Frequency Response, Sampling Rate = 48 kHz

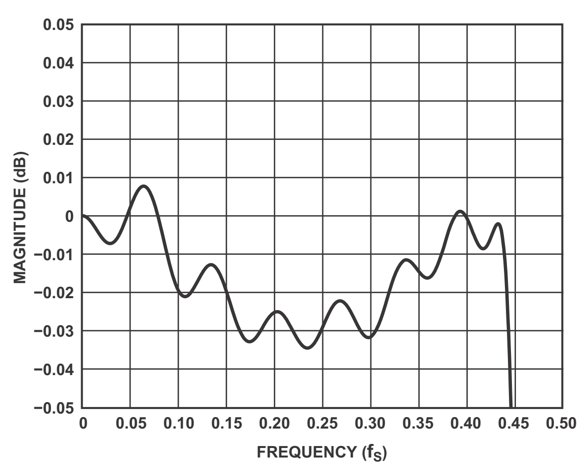

Figure 24. ADC Digital Filter Ripple, Sampling Rate = 48 kHz

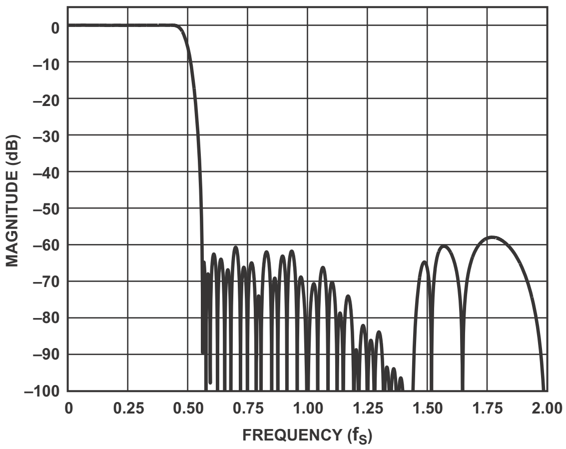

Figure 25. DAC Digital Filter Frequency Response, Sampling Rate = 48 kHz

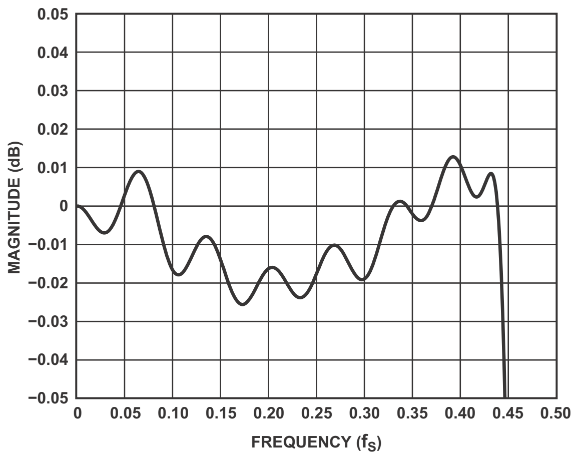

Figure 26. DAC Digital Filter Ripple, Sampling Rate = 48 kHz

DIGITAL DE-EMPHASIS

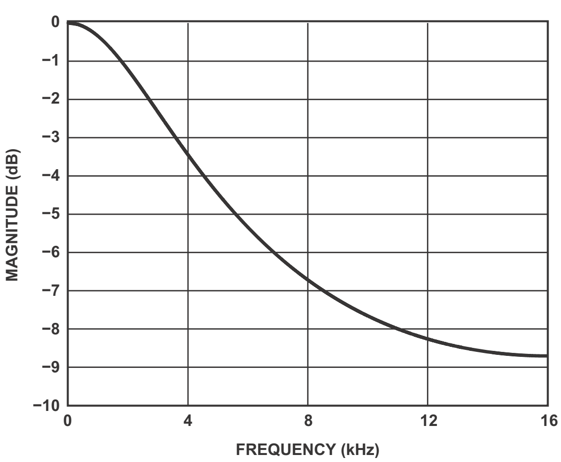

Figure 27. De-Emphasis Frequency Response, Sampling Rate = 32 kHz

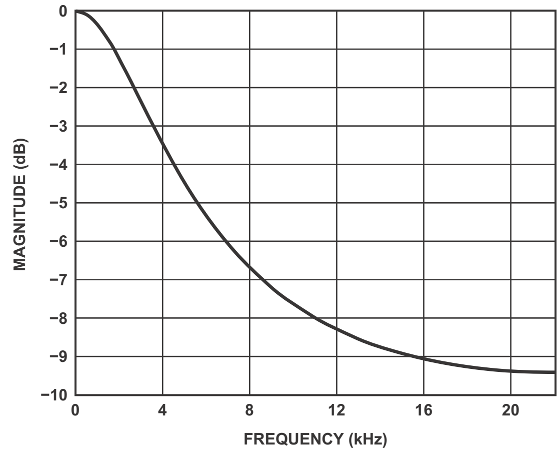

Figure 28. De-Emphasis Frequency Response, Sampling Rate = 44.1 kHz

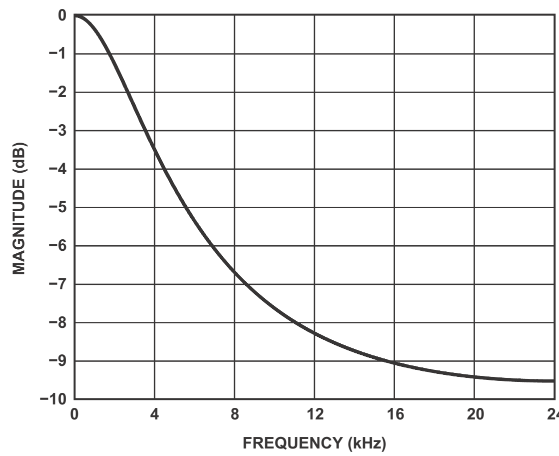

Figure 29. De-Emphasis Frequency Response, Sampling Rate = 48 kHz

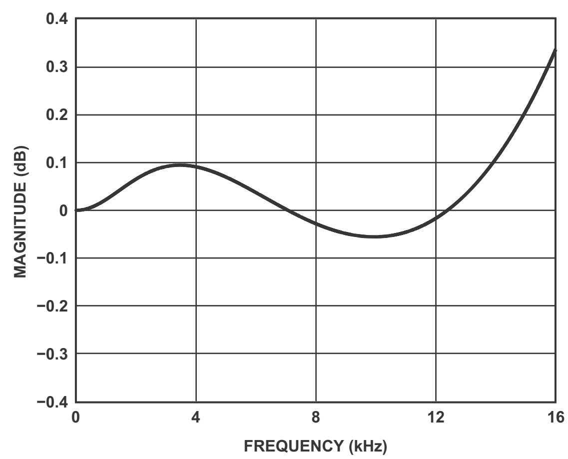

Figure 30. De-Emphasis Error, Sampling Rate = 32 kHz

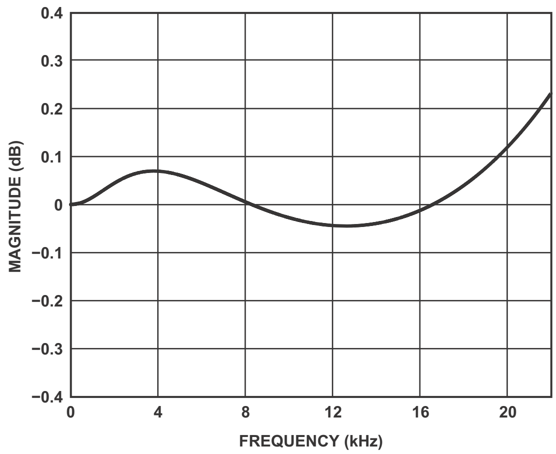

Figure 31. De-Emphasis Error, Sampling Rate = 44.1 kHz

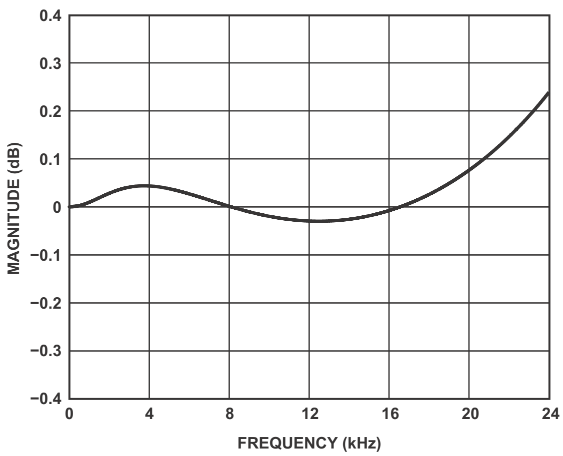

Figure 32. De-Emphasis Error, Sampling Rate = 48 kHz

289-BALL CSP_BGA BALL ASSIGNMENT

Signals added or changed to the ADSP-BF52xC processor for the embedded codec are shown in Table 23 and Table 24. Please refer to the published ADSP-BF52x processor data sheet for descriptions of additional signals for the processor.

Table 23. 289-Ball CSP_BGA Ball Assignment (Alphabetically)

Signal	Ball No.	Signal	Ball No.
ADCDAT	A16	HPGND	G17
ADCLRC	A15	HPVDD	G16[1]
AGND	H22	LHPOUT	B20
AVDD	J22[1]	LLINEIN	E23
CMODE	E22	LOUT	F22
CODEC_BCLK	A19	MICBIAS	H23
CODEC_CLKOUT	D22	MICIN	J23
CSB	D23	RHPOUT	B21
CSCL	B23	RLINEIN	F23
CSDA	C23	ROUT	G22
CVDD	H17[1]	VMID	G23
DACDAT	A18	XTI/CODEC_MCLK	A22
DACLRC	A17	XTO	A21

[1] For ADSP-BF52x processor (without internal codec) compatibility, connect this ball to V_{DDEXT}.

Table 24. 289-Ball CSP_BGA Ball Assignment (Numerically)

Ball No.	Signal	Ball No.	Signal
A15	ADCLRC	E22	CMODE
A16	ADCDAT	E23	LLINEIN
A17	DACLRC	F22	LOUT
A18	DACDAT	F23	RLINEIN
A19	CODEC_BCLK	G16[1]	HPVDD
A21	XTO	G17	HPGND
A22	XTI/CODEC_MCLK	G22	ROUT
B20	LHPOUT	G23	VMID
B21	RHPOUT	H17[1]	CVDD
B23	CSCL	H22	AGND
C23	CSDA	H23	MICBIAS
D22	CODEC_CLKOUT	J22[1]	AVDD
D23	CSB	J23	MICIN

[1] For ADSP-BF52x processor (without internal codec) compatibility, connect this ball to V_{DDEXT}.

Figure 34 shows the bottom view of the ADSP-BF52xC processor ball configuration.

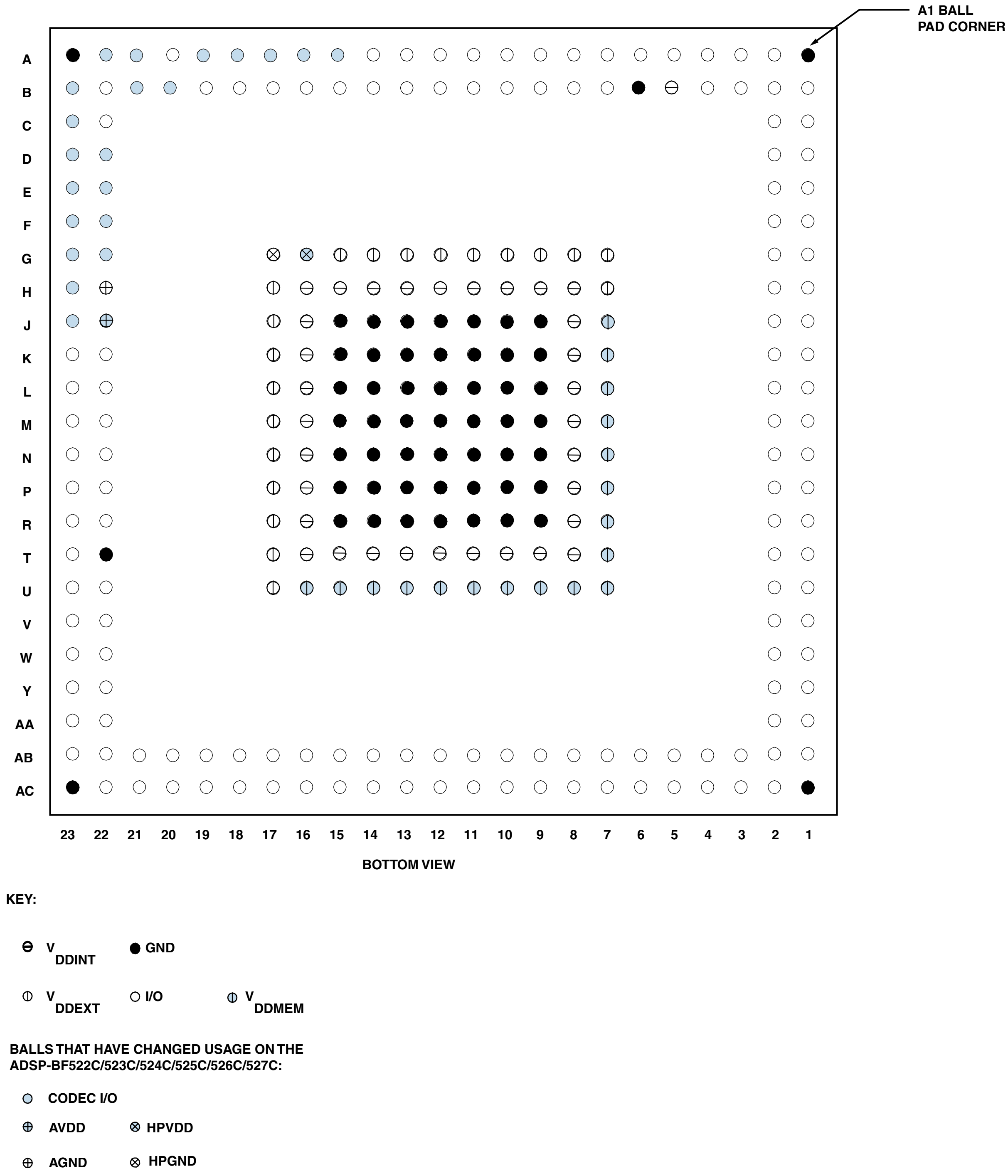

Figure 34. ADSP-BF52xC Processor Ball Configuration (Bottom View)

OUTLINE DIMENSIONS

Dimensions in Figure 35, 289-Ball CSP_BGA (BC-289-2) are shown in millimeters.

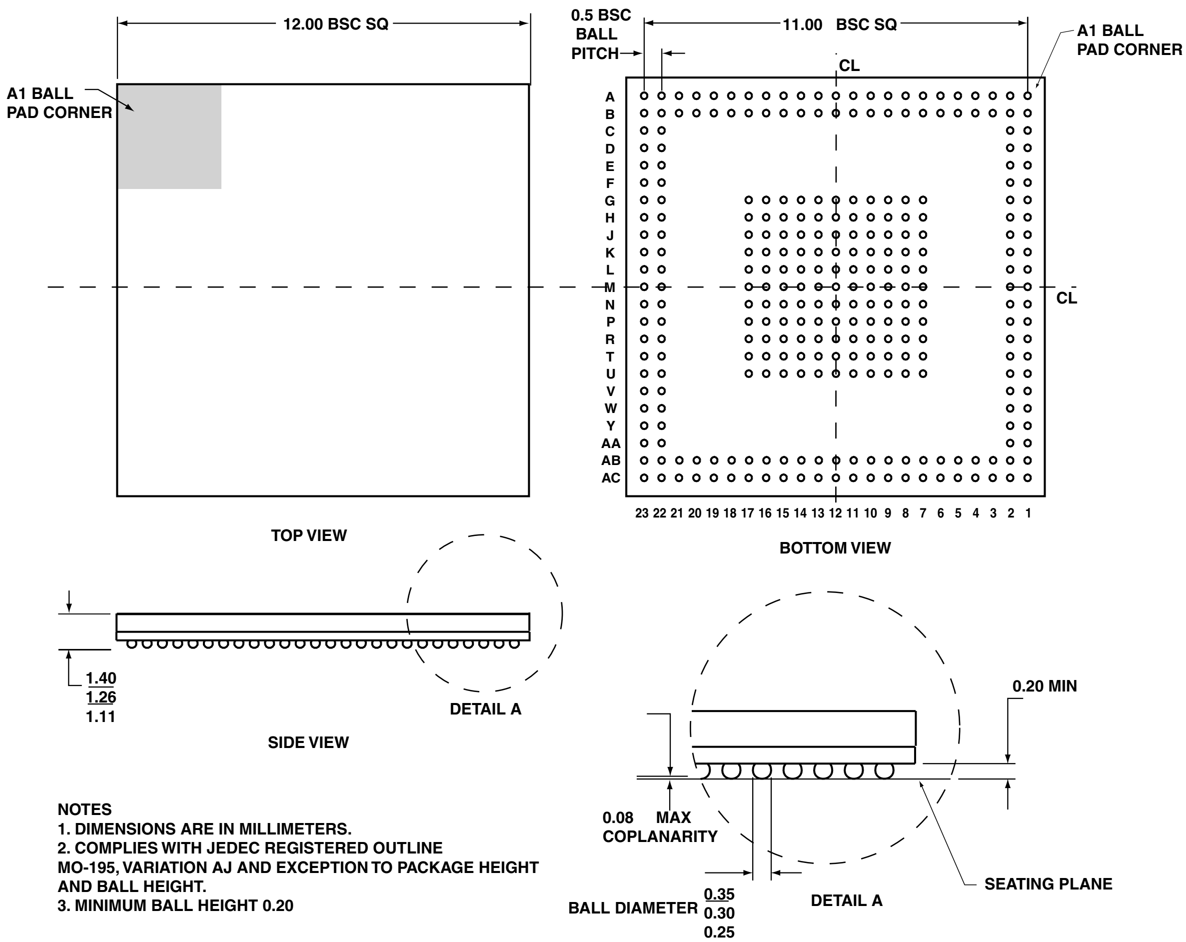

Figure 35. 289-Ball CSP_BGA (BC-289-2)

ORDERING GUIDE

Model[1]	Temperature Range[2]	Instruction Rate (Max)	Package Description	Package Option
ADSP-BF522KBCZ-3C2	0°C to +70°C	300 MHz	289-Ball Chip Scale Package Ball Grid Array (CSP_BGA)	BC-289-2
ADSP-BF522KBCZ-4C2	0°C to +70°C	400 MHz	289-Ball Chip Scale Package Ball Grid Array (CSP_BGA)	BC-289-2
ADSP-BF523KBCZ-5C2	0°C to +70°C	533 MHz	289-Ball Chip Scale Package Ball Grid Array (CSP_BGA)	BC-289-2
ADSP-BF523KBCZ-6C2	0°C to +70°C	600 MHz	289-Ball Chip Scale Package Ball Grid Array (CSP_BGA)	BC-289-2
ADSP-BF524KBCZ-3C2	0°C to +70°C	300 MHz	289-Ball Chip Scale Package Ball Grid Array (CSP_BGA)	BC-289-2
ADSP-BF524KBCZ-4C2	0°C to +70°C	400 MHz	289-Ball Chip Scale Package Ball Grid Array (CSP_BGA)	BC-289-2
ADSP-BF525KBCZ-5C2	0°C to +70°C	533 MHz	289-Ball Chip Scale Package Ball Grid Array (CSP_BGA)	BC-289-2
ADSP-BF525KBCZ-6C2	0°C to +70°C	600 MHz	289-Ball Chip Scale Package Ball Grid Array (CSP_BGA)	BC-289-2
ADSP-BF526KBCZ-3C2	0°C to +70°C	300 MHz	289-Ball Chip Scale Package Ball Grid Array (CSP_BGA)	BC-289-2
ADSP-BF526KBCZ-4C2	0°C to +70°C	400 MHz	289-Ball Chip Scale Package Ball Grid Array (CSP_BGA)	BC-289-2
ADSP-BF527KBCZ-5C2	0°C to +70°C	533 MHz	289-Ball Chip Scale Package Ball Grid Array (CSP_BGA)	BC-289-2
ADSP-BF527KBCZ-6C2	0°C to +70°C	600 MHz	289-Ball Chip Scale Package Ball Grid Array (CSP_BGA)	BC-289-2

[1] Z = RoHS Compliant Part.

[2] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 21 for junction temperature (T_J) specification which is the only temperature specification.

D06876-0-3/10(A)