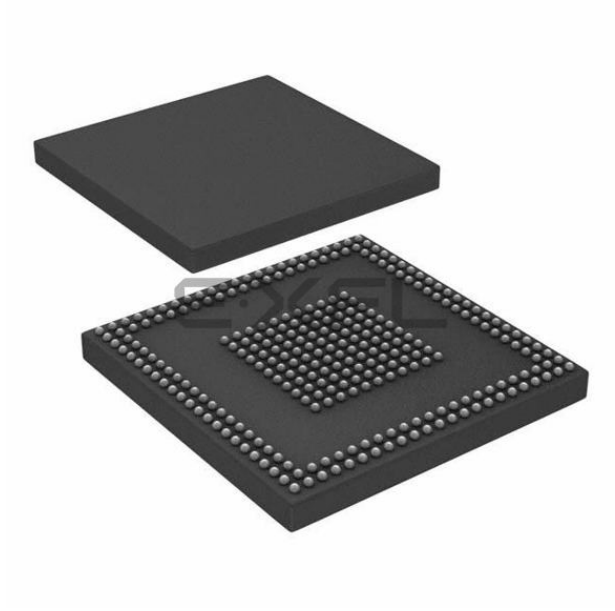

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	DMA, Ethernet, I²C, PPI, SPI, SPORT, UART, USB
Clock Rate	300MHz
Non-Volatile Memory	ROM (32kB)
On-Chip RAM	132kB
Voltage - I/O	1.8V, 2.5V, 3.3V
Voltage - Core	1.30V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	289-LFBGA, CSPBGA
Supplier Device Package	289-CSPBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf526kbcz-3c2

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REVISION HISTORY

3/10—Rev. 0 to Rev. A

Revised the following figures.
Recommended Application Circuit Using SPI Control 13
Recommended Application Circuit Using TWI Control .. 14

Added Sampling Rate = 48 kHz to all figures in
Converter Filter Response 30

Revised Ordering Guide 36

To allow an external device to generate the central reference clock, apply the external clock signal directly through the XTI/CODEC_MCLK input pin. In this configuration, the oscillator circuit of the codec can be powered down by using the OSCPD bit (Register R6, Bit D5) to reduce power consumption.

To accommodate applications with very high frequency master clocks, the internal core reference clock of the codec can be set to either CODEC_MCLK or CODEC_MCLK divided by 2. This is enabled by adjusting the setting of the CLKDIV2 bit (Register R8, Bit D6). The CODEC_CLKOUT pin can also drive external clock sources with either the codec clock signal or codec clock divided by 2 by enabling the CLKODIV2 bit (Register R8, Bit D7).

ADC AND DAC

The codec contains a pair of oversampling Σ-Δ ADCs. The maximum ADC full-scale input level is 1.0 V_{rms} when AVDD = 3.3 V. If the input signal to the ADC exceeds this level, data overloading occurs and causes audible distortion.

The ADC can accept analog audio input from either the stereo line inputs or the monaural microphone input. Note that the ADC can only accept input from a single source, so the programmer must choose either the line inputs or the microphone input using the INSEL bit (Register R4, Bit D2). The digital data from the ADC output, once converted, is processed using the ADC filters.

Complementary to the Σ-Δ ADC channels, the codec contains a pair of oversampling DACs that convert the digital audio data from the internal DAC filters into an analog audio signal. The DAC output can also be muted by setting the DACMU bit (Register R5, Bit D3) in the control register.

ADC HIGH-PASS AND DAC DE-EMPHASIS FILTERS

The ADC and DAC employ separate digital filters that perform 24-bit signal processing. The digital filters are used for both record and playback modes and are optimized for each individual sampling rate used.

For recording mode operations, the unprocessed data from the ADC enters the ADC filters and is converted to the appropriate sampling frequency, then is output to the digital audio interface.

For playback mode operations, the DAC filters convert the digital audio interface data to oversampled data using a sampling rate selected by the programmer. The oversampled data is processed by the DAC and sent to the analog output mixer by enabling the DACSEL (Register R4, Bit D4).

Programmers have the option of setting up the device so that any dc offset in the input source signal is automatically detected and removed. To accomplish this, enable the digital high-pass filter (see Table 22 on Page 30 for characteristics) contained in the ADC digital filters by using the ADCHPD bit (Register R5, Bit D0).

In addition, programmers can implement digital de-emphasis by using the DEEMPH bits (Register R5, Bit D1 and Bit D2).

ANALOG AUDIO INTERFACES

The codec includes stereo single-ended line inputs and a monaural microphone input to the on-board ADC. Either the line inputs or the microphone input, but not both simultaneously, can be connected to the ADC by setting the INSEL bit (Register R4, Bit D2).

The codec also includes line and headphone outputs from the on-board DAC. The line or microphone inputs can be routed and mixed directly to the output terminals.

Stereo Line and Monaural Microphone Inputs

The single-ended stereo line inputs (RLINEIN and LLINEIN) are internally biased to VMID by way of a voltage divider between AVDD and AGND (see Figure 2). The line input signal can be connected to the internal ADC and, if desired, routed directly to the outputs via the bypass path by using the BYPASS bit (Register R4, Bit D3).

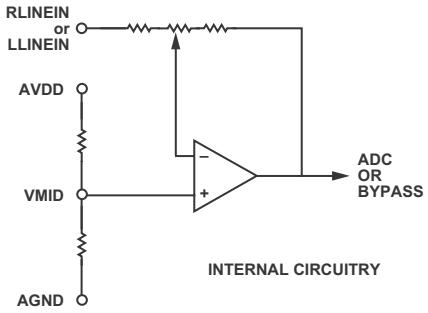


Figure 2. Line Input to ADC

The line input volume can be adjusted from –34.5 dB to +33 dB in steps of +1.5 dB by setting the LINVOL (Register R0, Bit D0 to Bit D5) and RINVOL (Register R1, Bit D0 to Bit D5) bits. By default the volume is independently adjustable for both right and left line inputs. However, if the LRINBOTH or RLINBOTH bit is programmed, both LINVOL and RINVOL are loaded with the same value. The programmer can also set the LINMUTE (Register R0, Bit D7) and RINMUTE (Register R1, Bit D7) bits to mute the line input signal to the ADC.

The high impedance, low capacitance monaural microphone input pin (MICIN, shown in Figure 3) has two gain stages and a microphone bias level (MICBIAS) that is internally biased to the VMID voltage level by way of a voltage divider between AVDD and AGND. The microphone input signal can be connected to the internal ADC and, if desired, routed directly to the outputs via the sidetone path by using the SIDETONE bit (Register R4, Bit D5).

The programmer can simultaneously load the volume control of both channels by writing to the LRHPBOTH (Register R2, Bit D8) and RLHPBOTH (Register R3, Bit D8) bits of the left- or right-channel DAC volume registers.

The maximum output level of the headphone outputs is 1.0 V rms when AVDD and HPVDD = 3.3 V. To suppress audible pops and clicks, the headphone and line outputs are held at the VMID dc voltage level when the device is set to standby mode or when the headphone outputs are muted.

The stereo line outputs of the codec, the LOUT and ROUT pins, can drive a load impedance of 10 kΩ and 50 pF. The line output signal levels are not adjustable at the output mixer, which has a fixed gain of 0 dB. The maximum output level of the line outputs is 1.0 V rms when AVDD = 3.3 V.

DIGITAL AUDIO INTERFACE

The digital audio input can support the following digital audio communication protocols: right-justified mode, left-justified mode, I²S mode, and frame sync mode. See Figure 6 on Page 6 through Figure 10 on Page 7.

The mode selection is performed by writing to the FORMAT bits of the digital audio interface register (Register R7, Bit D1 and Bit D0). All modes are MSB first and operate with data of 16 to 32 bits.

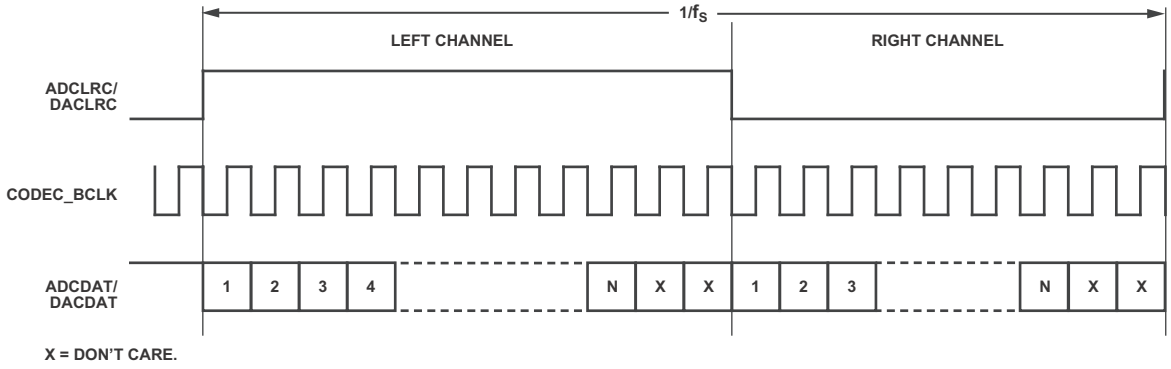


Figure 6. Left-Justified Audio Input Mode

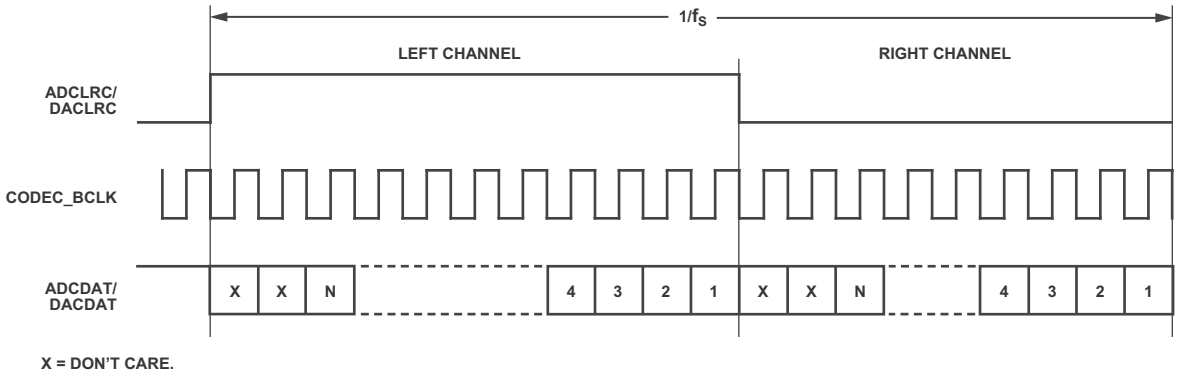


Figure 7. Right-Justified Audio Input Mode

Recording Mode

The digital audio interface sends the ADC digital filter data to the ADCDAT output pin for recording. The ADCDAT data stream multiplexes the left- and right-channel audio data in the time domain. The ADCLRC clock signal separates left- and right-channel digital audio frames on the ADCDAT lines.

The CODEC_BCLK signal clocks the digital audio data within the frames. The CODEC_BCLK signal is either an input or an output depending on whether the codec is in master or slave mode. During a recording operation, ADCDAT and ADCLRC must be synchronous to the CODEC_BCLK signal to avoid data corruption.

Playback Mode

The digital audio interface receives data on the DACDAT input pin for playback. The digital audio data stream on the DACDAT pin is time-domain-multiplexed left and right channel audio data. The DACLRC clock signal separates left and right channel digital audio frames on the DACDAT lines.

The CODEC_BCLK signal clocks the digital audio data within the frames. The CODEC_BCLK signal is either an input or an output depending on whether the codec is in master or slave mode. During a playback operation, DACDAT and DACLRC must be synchronous to the CODEC_BCLK signal to avoid data corruption.

Digital Audio Data Sampling Rate

To accommodate a wide variety of commonly used DAC and ADC sampling rates, the codec allows for two modes of operation, normal and USB, selected by the USB bit (Register R8, Bit D0).

The sampling rate is generated as a fixed divider from the CODEC_MCLK signal. Because all audio processing references the CODEC_MCLK signal, corruption of this signal will corrupt the quality of the audio at the codec output. The ADCLRC/ADCDAT/CODEC_BCLK or DACLRC/DACDAT/CODEC_BCLK signals must be synchronized with CODEC_MCLK in the digital audio interface circuit.

CODEC_MCLK must be faster or equal to the CODEC_BCLK frequency to guarantee that no data is lost during data synchronization. The CODEC_BCLK frequency should be greater than the sampling rate × word length × 2. Ensuring that the CODEC_BCLK frequency is greater than this, guarantees that all valid data bits are captured by the digital audio interface circuitry. For example, if a 32 kHz digital audio sampling rate with a 32-bit word length is desired, CODEC_BCLK = 2.048 MHz.

Normal Mode

In normal mode, the codec supports digital audio sampling rates from 8 kHz to 96 kHz. Normal mode supports 256 × f_S and 384 × f_S based clocks. To select the desired sampling rate, the programmer must set the appropriate sampling rate register in the SR control bits (Register R8, Bit D2 to Bit D5) and match this selection to the core clock frequency that is pulsed on the CODEC_MCLK pin. See Table 1 for sampling rates in normal mode.

Table 1. Sampling Rate Lookup Table, Normal Mode (USB Disabled)

CODEC_MCLK (CLKDIV2 = 0)	CODEC_MCLK (CLKDIV2 = 1)	ADC Sampling Rate (ADCLRC)	DAC Sampling Rate (DACLRC)	USB	SR [3:0]	BOSR	CODEC_BCLK (MS = 1)[1]
12.288 MHz	24.576 MHz	8 kHz (CODEC_MCLK/1536)	8 kHz (CODEC_MCLK/1536)	0	0011	0	CODEC_MCLK/4
		8 kHz (CODEC_MCLK/1536)	48 kHz (CODEC_MCLK/256)	0	0010	0	CODEC_MCLK/4
		12 kHz (CODEC_MCLK/1024)	12 kHz (CODEC_MCLK/1024)	0	0100	0	CODEC_MCLK/4
		16 kHz (CODEC_MCLK/768)	16 kHz (CODEC_MCLK/768)	0	0101	0	CODEC_MCLK/4
		24 kHz (CODEC_MCLK/512)	24 kHz (CODEC_MCLK/512)	0	1110	0	CODEC_MCLK/4
		32 kHz (CODEC_MCLK/384)	32 kHz (CODEC_MCLK/384)	0	0110	0	CODEC_MCLK/4
		48 kHz (CODEC_MCLK/256)	8 kHz (CODEC_MCLK/1536)	0	0001	0	CODEC_MCLK/4
		48 kHz (CODEC_MCLK/256)	48 kHz (CODEC_MCLK/256)	0	0000	0	CODEC_MCLK/4
		96 kHz (CODEC_MCLK/128)	96 kHz (CODEC_MCLK/128)	0	0111	0	CODEC_MCLK/2
11.2896 MHz	22.5792 MHz	8.0182 kHz (CODEC_MCLK/1408)	8.0182 kHz (CODEC_MCLK/1408)	0	1011	0	CODEC_MCLK/4
		8.0182 kHz (CODEC_MCLK/1408)	44.1 kHz (CODEC_MCLK/256)	0	1010	0	CODEC_MCLK/4
		11.025 kHz (CODEC_MCLK/1024)	11.025 kHz (CODEC_MCLK/1024)	0	1100	0	CODEC_MCLK/4
		22.05 kHz (CODEC_MCLK/512)	22.05 kHz (CODEC_MCLK/512)	0	1101	0	CODEC_MCLK/4
		44.1 kHz (CODEC_MCLK/256)	8.0182 kHz (CODEC_MCLK/1408)	0	1001	0	CODEC_MCLK/4
		44.1 kHz (CODEC_MCLK/256)	44.1 kHz (CODEC_MCLK/256)	0	1000	0	CODEC_MCLK/4
		88.2 kHz (CODEC_MCLK/128)	88.2 kHz (CODEC_MCLK/128)	0	1111	0	CODEC_MCLK/2
18.432 MHz	36.864 MHz	8 kHz (CODEC_MCLK/2304)	8 kHz (CODEC_MCLK/2304)	0	0011	1	CODEC_MCLK/6
		8 kHz (CODEC_MCLK/2304)	48 kHz (CODEC_MCLK/384)	0	0010	1	CODEC_MCLK/6
		12 kHz (CODEC_MCLK/1536)	12 kHz (CODEC_MCLK/1536)	0	0100	1	CODEC_MCLK/6
		16 kHz (CODEC_MCLK/1152)	16 kHz (CODEC_MCLK/1152)	0	0101	1	CODEC_MCLK/6
		24 kHz (CODEC_MCLK/768)	24 kHz (CODEC_MCLK/768)	0	1110	1	CODEC_MCLK/6
		32 kHz (CODEC_MCLK/576)	32 kHz (CODEC_MCLK/576)	0	0110	1	CODEC_MCLK/6
		48 kHz (CODEC_MCLK/384)	48 kHz (CODEC_MCLK/384)	0	0000	1	CODEC_MCLK/6
		48 kHz (CODEC_MCLK/384)	8 kHz (CODEC_MCLK/2304)	0	0001	1	CODEC_MCLK/6
		96 kHz (CODEC_MCLK/192)	96 kHz (CODEC_MCLK/192)	0	0111	1	CODEC_MCLK/3
16.9344 MHz	33.8688 MHz	8.0182 kHz (CODEC_MCLK/2112)	8.0182 kHz (CODEC_MCLK/2112)	0	1011	1	CODEC_MCLK/6
		8.0182 kHz (CODEC_MCLK/2112)	44.1 kHz (CODEC_MCLK/384)	0	1010	1	CODEC_MCLK/6
		11.025 kHz (CODEC_MCLK/1536)	11.025 kHz (CODEC_MCLK/1536)	0	1100	1	CODEC_MCLK/6
		22.05 kHz (CODEC_MCLK/768)	22.05 kHz (CODEC_MCLK/768)	0	1101	1	CODEC_MCLK/6
		44.1 kHz (CODEC_MCLK/384)	8.0182 kHz (CODEC_MCLK/2112)	0	1001	1	CODEC_MCLK/6
		44.1 kHz (CODEC_MCLK/384)	44.1 kHz (CODEC_MCLK/384)	0	1000	1	CODEC_MCLK/6
		88.2 kHz (CODEC_MCLK/192)	88.2 kHz (CODEC_MCLK/192)	0	1111	1	CODEC_MCLK/3

[1] CODEC_BCLK frequency is for master mode and slave right-justified mode only.

USB Mode

In USB mode, the codec supports digital audio sampling rates from 8 kHz to 96 kHz. USB mode is enabled on the codec to support the common universal serial bus (USB) clock rate of 12 MHz, or to support 24 MHz if the CLKDIV2 control register bit is activated. The programmer must set the appropriate sampling rate in the SR control bits (Register R8, Bit D2 to Bit D5). See Table 2 for sampling rates in USB mode.

Table 2. Sampling Rate Lookup Table, USB Mode (USB Enabled)

CODEC_MCLK (CLKDIV2 = 0)	CODEC_MCLK (CLKDIV2 = 1)	ADC Sampling Rate (ADCLRC)	DAC Sampling Rate (DACLRC)	USB	SR [3:0]	BOSR	CODEC_BCLK (MS = 1)[1]
12.000 MHz	24.000 MHz	8 kHz (CODEC_MCLK/1500)	8 kHz (CODEC_MCLK/1500)	1	0011	0	CODEC_MCLK
		8 kHz (CODEC_MCLK/1500)	48 kHz (CODEC_MCLK/250)	1	0010	0	CODEC_MCLK
		8.0214 kHz (CODEC_MCLK/1496)	8.0214 kHz (CODEC_MCLK/1496)	1	1011	1	CODEC_MCLK
		8.0214 kHz (CODEC_MCLK/1496)	44.118 kHz (CODEC_MCLK/272)	1	1010	1	CODEC_MCLK
		11.0259 kHz (CODEC_MCLK/1088)	11.0259 kHz (CODEC_MCLK/1088)	1	1100	1	CODEC_MCLK
		12 kHz (CODEC_MCLK/1000)	12 kHz (CODEC_MCLK/1000)	1	1000	0	CODEC_MCLK
		16 kHz (CODEC_MCLK/750)	16 kHz (CODEC_MCLK/750)	1	1010	0	CODEC_MCLK
		22.0588 kHz (CODEC_MCLK/544)	22.0588 kHz (CODEC_MCLK/544)	1	1101	1	CODEC_MCLK
		24 kHz (CODEC_MCLK/500)	24 kHz (CODEC_MCLK/500)	1	1110	0	CODEC_MCLK
		32 kHz (CODEC_MCLK/375)	32 kHz (CODEC_MCLK/375)	1	0110	0	CODEC_MCLK
		44.118 kHz (CODEC_MCLK/272)	8.0214 kHz (CODEC_MCLK/1496)	1	1001	1	CODEC_MCLK
		44.118 kHz (CODEC_MCLK/272)	44.118 kHz (CODEC_MCLK/272)	1	1000	1	CODEC_MCLK
		48 kHz (CODEC_MCLK/250)	8 kHz (CODEC_MCLK/1500)	1	0001	0	CODEC_MCLK
		48 kHz (CODEC_MCLK/250)	48 kHz (CODEC_MCLK/250)	1	0000	0	CODEC_MCLK
		88.235 kHz (CODEC_MCLK/136)	88.235 kHz (CODEC_MCLK/136)	1	1111	1	CODEC_MCLK
		96 kHz (CODEC_MCLK/125)	96 kHz (CODEC_MCLK/125)	1	0111	0	CODEC_MCLK

[1] CODEC_BCLK frequency is for master mode and slave right-justified mode only.

SOFTWARE CONTROL INTERFACE

The software control interface provides access to the programmer-selectable control registers and can operate with a 2-wire (TWI) or 3-wire (SPI) interface, depending on the setting of the CMODE pin. If the CMODE pin is set to 0, the 2-wire interface is selected; if 1, the 3-wire interface is selected.

Within each control register is a control data-word consisting of 16 bits, MSB first. Bit B15 to Bit B9 are the register map address, and Bit B8 to Bit B0 are register data for the associated register map.

When 2-wire (TWI) mode is selected, CSDA generates the serial control data-word; CSCL clocks the serial data; and CSB determines the TWI device address. If the CSB pin is set to 0, the address selected is 0011010; if 1, the address is 0011011.

When 3-wire (SPI) mode is selected, CSDA generates the control data-word, CSCL clocks the control data-word into the codec, and CSB latches in the control data-word.

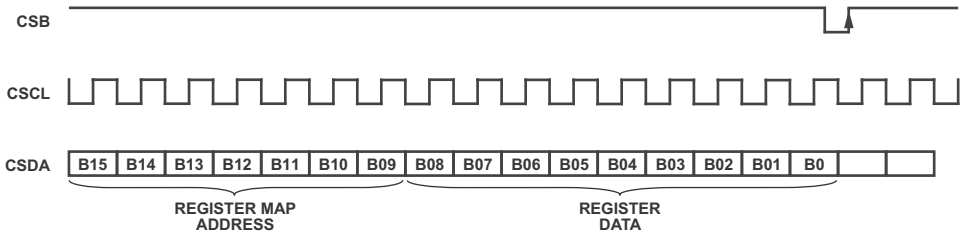


Figure 11. Codec SPI Serial Interface

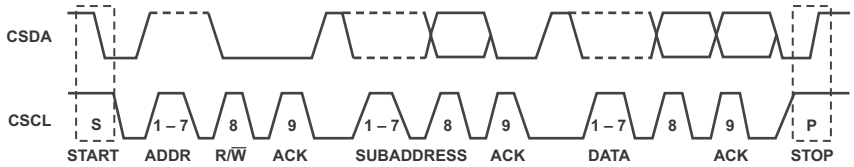
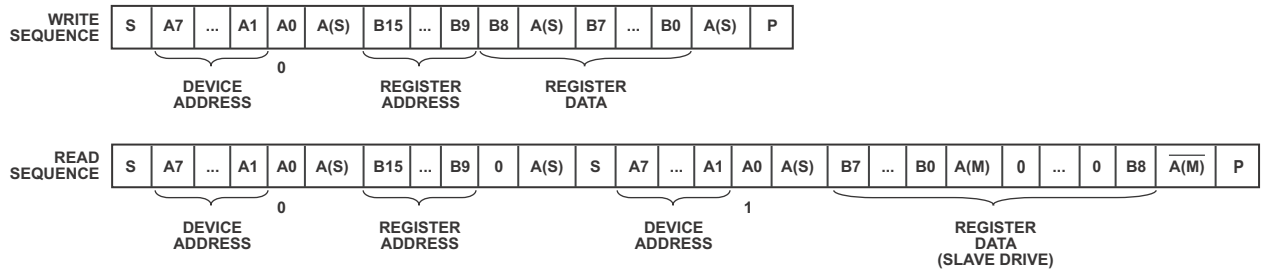


Figure 12. Codec TWI Serial Interface



S/P = START/STOP BIT.
A0 = I²C R/$\overline{W}$ BIT.
A(S) = ACKNOWLEDGE BY SLAVE.
A(M) = ACKNOWLEDGE BY MASTER.
$\overline{A(M)}$ = ACKNOWLEDGE BY MASTER (INVERSION).

Figure 13. Codec TWI Write and Read Sequences

CODEC PIN DESCRIPTIONS

Table 3 shows the signals added to the ADSP-BF52xC processor for the embedded codec. Please refer to the published ADSP-BF52x data sheet for descriptions of other signals for the processor.

Table 3. Codec Pin Descriptions

Pin Name	Type	Function	Pull-Up/Down
Codec			
CODEC_CLKOUT	O	Codec Clock Output	None
CODEC_BCLK	I/O	Codec Digital Audio Bit Clock	Internal Pull-down[1]
DACDAT	I	Codec Digital Audio Data (DAC) Input	None
DACLRC	I/O	Codec DAC Sample Rate Left/Right Clock	Internal Pull-down[1]
ADCDAT	O	Codec ADC Digital Audio Data Output	None
ADCLRC	I/O	Codec ADC Sample Rate Left/Right Clock	Internal Pull-down[1]
CMODE	I	Codec Control Interface Selection	Internal Pull-up[1]
CSB	I	Codec Chip Select Interface Address Selection	Internal Pull-up[1]
CSDA	I/O	Codec Data Input	None
CSCL	I/O	Codec Data Clock	None
XTI/CODEC_MCLK	I	Codec Crystal Input/ Clock Input	None
XTO	O	Codec Crystal Output	None
LHPOUT	O	Codec Left Channel Headphone Output (Analog Output)	None
RHPOUT	O	Codec Right Channel Headphone Output (Analog Output)	None
LOUT	O	Codec Left Channel Line Output (Analog Output)	None
ROUT	O	Codec Right Channel Line Output (Analog Output)	None
VMID	O	Codec Mid-rail Reference Decoupling Point (Analog Output)	None
MICBIAS	O	Codec Electret Microphone Bias (Analog Output)	None
MICIN	I	Codec Microphone Input; (Analog Input, AC Coupled)	None
RLINEIN	I	Codec Right Channel Line Input (Analog Input, AC Coupled)	None
LLINEIN	I	Codec Left Channel Line Input (Analog Input, AC Coupled)	None
AVDD	P	Codec Analog V_{DD}	N/A
AGND	P	Codec Analog Ground	N/A
CVDD	P	Codec Digital V_{DD}	N/A
HPVDD	P	Codec Analog Headphone V_{DD}	N/A
HPGND	P	Codec Headphone Ground	N/A

[1] To conserve power, the pull-up/pull-down is only present when the control register interface is active (= 0).

Figure 14 on Page 13 and Figure 15 on Page 14 describe alternative external connections for SPI or TWI control of the ADSP-BF52xC codec. The figures are the same except for the shaded area in each.

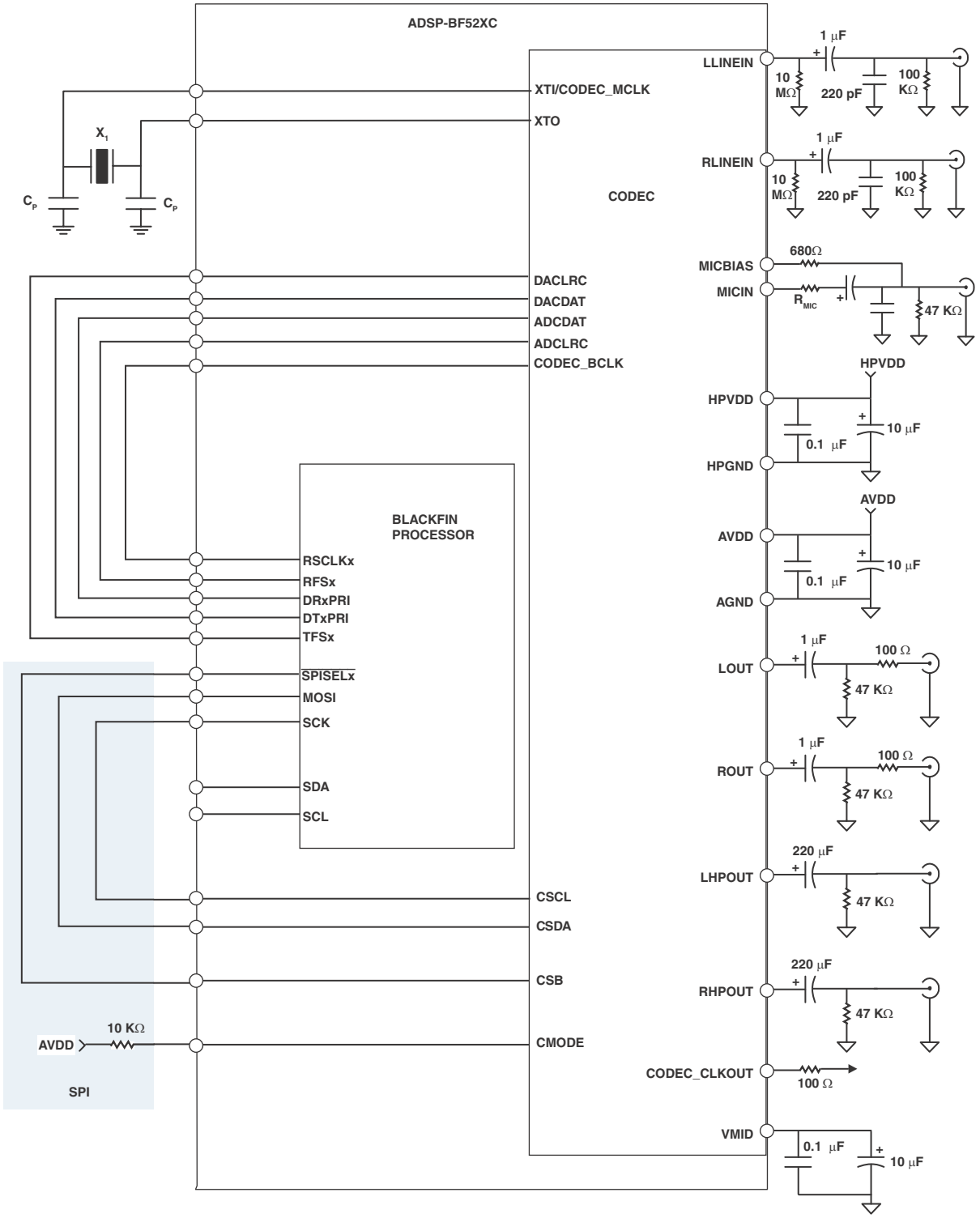


Figure 14. Recommended Application Circuit Using SPI Control

Table 5. Register 1 Right-Channel ADC Input Volume

Bit Name	Bits	Description	Settings
RLINBOTH	B8	Right-to-left line input ADC data load control	0 = disable simultaneous loading of right-channel ADC data to left-channel register (default)
			1 = enable simultaneous loading of right-channel ADC data to left-channel register
RINMUTE	B7	Right-channel input mute	0 = disable mute
			1 = enable mute on data path to ADC (default)
RINVOL	B[5:0]	Right-channel PGA volume control	00 0000 = –34.5 dB
			… 1.5 dB step up
			01 0111 = 0 dB (default)
			… 1.5 dB step up
			01 1111 = 12 dB
			10 0000 = 13.5 dB
			10 0001 = 15 dB
			10 0010 = 16.5 dB
			10 0011 = 18 dB
			10 0100 = 19.5 dB
			10 0101 = 21 dB
			10 0110 = 22.5 dB
			10 0111 = 24 dB
			10 1000 = 25.5 dB
			10 1001 = 27 dB
			10 1010 = 28.5 dB
			10 1011 = 30 dB
			10 1100 = 31.5 dB
			10 1101 = 33 dB
			11 1111 to 10 1101 = 33 dB

Table 6. Register 2 Left-Channel DAC Volume

Bit Name	Bits	Description	Settings
LRHPBOTH	B8	Left-to-right headphone volume load control	0 = disable simultaneous loading of left-channel headphone volume data to right-channel register (default)
			1 = enable simultaneous loading of left-channel headphone volume data to right-channel register
LZCEN	B7	Left-channel zero cross detect enable	0 = disable (default) 1 = enable
LHPVOL	B[6:0]	Left-channel headphone volume control	000 0000 to 010 1111 = mute
			011 0000 = –73 dB
			…
			111 1001 = 0 dB (default)
			… 1 dB steps up to
			111 1111 = +6 dB

Table 11. Register 7 Digital Audio I/F

Bit Name	Bits	Description	Settings
BCLKINV	B7	CODEC_BCLK inversion control	0 = CODEC_BCLK not inverted (default)
			1 = CODEC_BCLK inverted
MS	B6	Master mode enable	0 = enable slave mode (default)
			1 = enable master mode
LRSWAP	B5	Swap DAC data control	0 = output left- and right-channel data as normal (default)
			1 = swap left- and right-channel DAC data in audio interface
LRP	B4	Polarity control for clocks in right-justified, left-justified, and I^2S modes	0 = normal DACLRC and ADCLRC (default), or processor Submode 1
			1 = invert DACLRC and ADCLRC polarity, or processor Submode 2
WL [1:0]	B[3:2]	Data-word length control	00 = 16 bits
			01 = 20 bits
			10 = 24 bits (default)
			11 = 32 bits
FORMAT [1:0]	B[1:0]	Digital audio input format control	00 = right justified
			01 = left justified
			10 = I^2S mode (default)
			11 = processor mode

Table 12. Register 8 Sampling Rate

Bit Name	Bits	Description	Settings
CLKODIV2	B7	CODEC_CLKOUT divider select	0 = CODEC_CLKOUT is codec clock (default)
			1 = CODEC_CLKOUT is codec clock divided by 2
CLKDIV2	B6	Codec clock divide select	0 = codec clock is CODEC_MCLK (default)
			1= codec clock is CODEC_MCLK divided by 2
SR [3:0]	B[5:2]	Clock setting condition	See Table 1 on Page 9 and Table 2 on Page 10
BOSR	B1	Base oversampling rate	USB mode:
			0 = support for 250 × f_S based clock (default)
			1 = support for 272 × f_S based clock
			Normal mode:
			0 = support for 256 × f_S based clock (default)
			1 = support for 384 × f_S based clock
USB	B0	USB mode select	0 = normal mode enable (default)
			1 = USB mode enable

Table 13. Register 9 Active

Bit Name	Bit	Description	Settings
ACTIVE	B0	Digital core activation control	0 = disable digital core (default)
			1 = activate digital core

Table 14. Register 10 Software Reset

Bit Name	Bit	Description	Settings
RESET [8:0]	B[8:0]	Write all 0s to this register to set all registers to their default settings. Other data written to this register has no effect.	0 = reset (default)

ABSOLUTE MAXIMUM RATINGS

See absolute maximum ratings in the published ADSP-BF52x processor data sheet.

ESD SENSITIVITY

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PACKAGE INFORMATION

The information presented in Figure 17 and Table 15 provides details about the package branding for the ADSP-BF52xC processor. For a complete listing of product availability, see Ordering Guide on Page 36.

Figure 17. Product Information on Package

Table 15. Package Brand Information

Brand Key	Field Description
t	Temperature Range
pp	Package Type
Z	Lead Free Option
ccc	See Ordering Guide
vvvvvv.x	Assembly Lot Code
n.n	Silicon Revision
yyww	Date Code

Digital Audio Interface Slave Mode Timing

Table 19. Digital Audio Interface Slave Mode Timing

Parameter		Test Conditions[1]	Min	Max	Unit
t_{DS}	DACDAT setup time from CODEC_BCLK rising edge		10		ns
t_{DH}	DACDAT hold time from CODEC_BCLK rising edge		10		ns
t_{LRSU}	ADCLRC/DACLRC setup time to CODEC_BCLK rising edge		10		ns
t_{LRH}	ADCLRC/DACLRC hold time to CODEC_BCLK rising edge		10		ns
t_{DD}	ADCDAT propagation delay from CODEC_BCLK falling edge (external load of 70 pF)			30	ns
t_{BCH}	CODEC_BCLK pulse width high		25		ns
t_{BCL}	CODEC_BCLK pulse width low		25		ns
t_{BCY}	CODEC_BCLK cycle time		50		ns

[1] AVDD, HPVDD, V_{DDEXT} = 3.3 V, AGND = 0 V, T_A = +25°C, Slave Mode, f_S = 48 kHz, XTI/CODEC_MCLK = 256 × f_S unless otherwise stated.

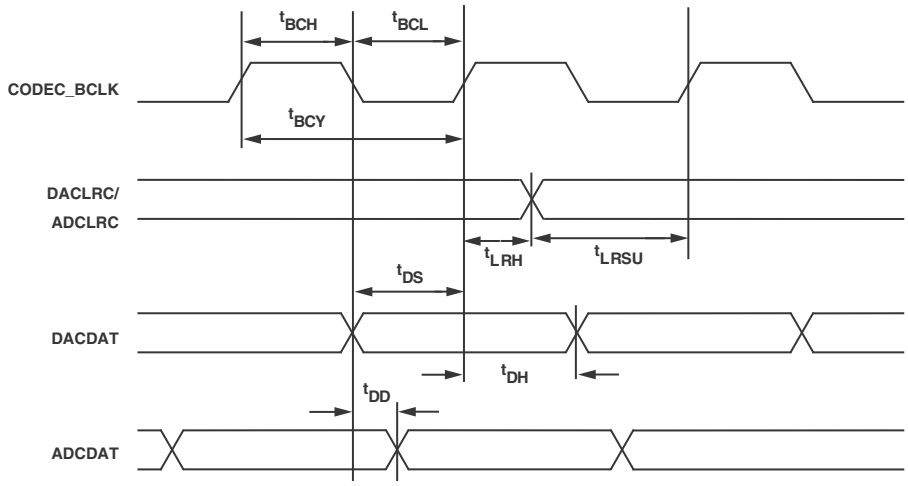


Figure 20. Digital Audio Interface Slave Mode Timing

Digital Audio Interface Master Mode Timing

Table 20. Digital Audio Interface Master Mode Timing

Parameter		Test Conditions[1]	Min	Max	Unit
t_{DST}	DACDAT setup time to CODEC_BCLK rising edge		30		ns
t_{DHT}	DACDAT hold time to CODEC_BCLK rising edge		10		ns
t_{DL}	ADCLRC/DACLRC propagation delay from CODEC_BCLK falling edge			10	ns
t_{DDA}	ADCDAT propagation delay from CODEC_BCLK falling edge			10	ns
t_{BCLKR}	CODEC_BCLK rising time (10 pF load)		10		ns
t_{BCLKF}	CODEC_BCLK falling time (10 pF load)		10		ns
t_{BCLKDS}	CODEC_BCLK duty cycle (normal and USB mode)		45:55	55:45	

[1] AVDD, HPVDD, V_{DDEXT} = 3.3 V, AGND = 0 V, T_A = +25°C, Slave Mode, f_S = 48 kHz, XTI/CODEC_MCLK = 256 × f_S unless otherwise stated.

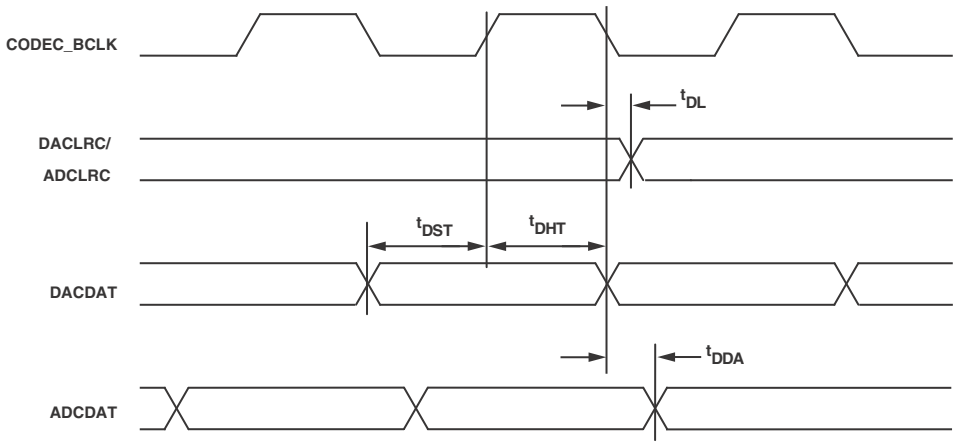


Figure 21. Digital Audio Interface Master Mode Timing

Digital Filter Characteristics

Table 22. Digital Filter Characteristics

Parameter	Conditions	Min	Typical	Max	Unit
ADC FILTER					
Pass Band	±0.04 dB	0		$0.445 \times f_S$	Hz
	–6 dB		$0.5 \times f_S$		Hz
Pass Band Ripple				±0.04	dB
Stop Band		$0.555 \times f_S$			Hz
Stop Band Attenuation	$f > 0.567 \times f_S$	–61			dB
High-Pass Filter Corner Frequency	–3 dB		3.7		Hz
	–0.5 dB		10.4		Hz
	–0.1 dB		21.6		Hz
DAC FILTER					
Pass Band	±0.04 dB	0		$0.445 \times f_S$	Hz
	–6 dB		$0.5 \times f_S$		Hz
Pass Band Ripple				±0.04	dB
Stop Band		$0.555 \times f_S$			Hz
Stop Band Attenuation	$f > 0.565 \times f_S$	–61			dB
Codec Clock Tolerance					
Frequency Range		8.0		13.8	MHz
Jitter Tolerance			50		pS

CONVERTER FILTER RESPONSE

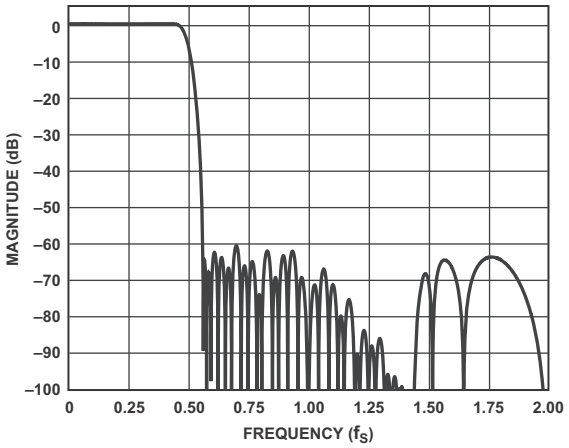


Figure 23. ADC Digital Filter Frequency Response, Sampling Rate = 48 kHz

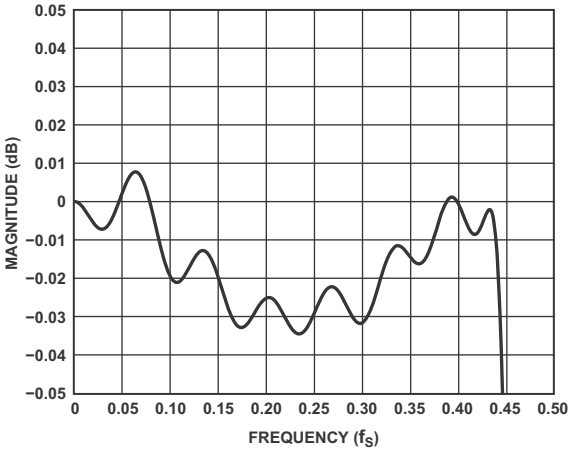


Figure 24. ADC Digital Filter Ripple, Sampling Rate = 48 kHz

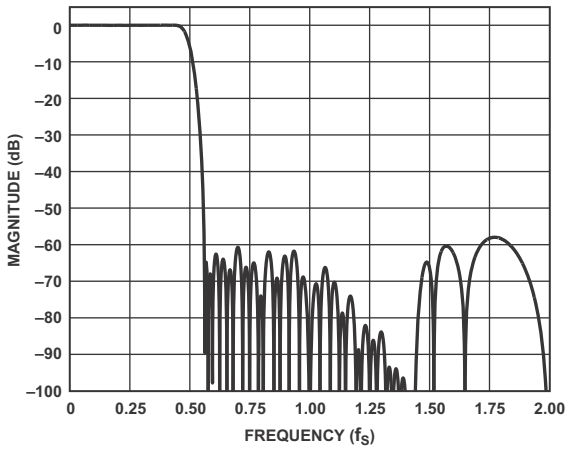


Figure 25. DAC Digital Filter Frequency Response, Sampling Rate = 48 kHz

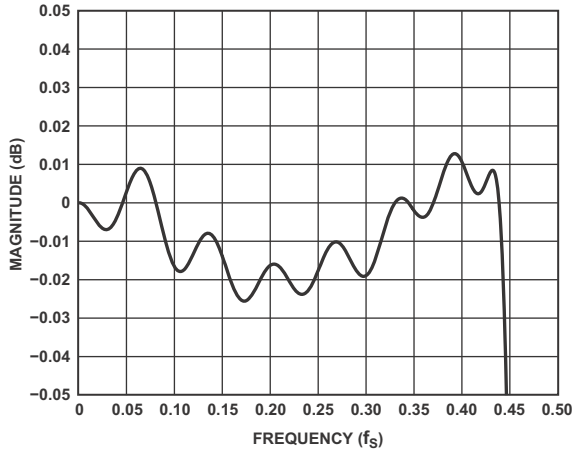


Figure 26. DAC Digital Filter Ripple, Sampling Rate = 48 kHz

DIGITAL DE-EMPHASIS

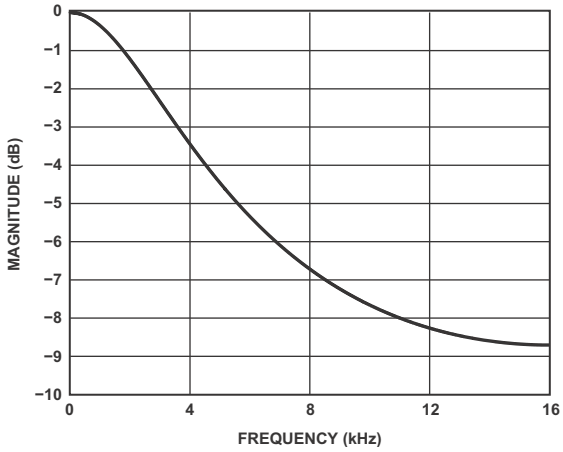


Figure 27. De-Emphasis Frequency Response, Sampling Rate = 32 kHz

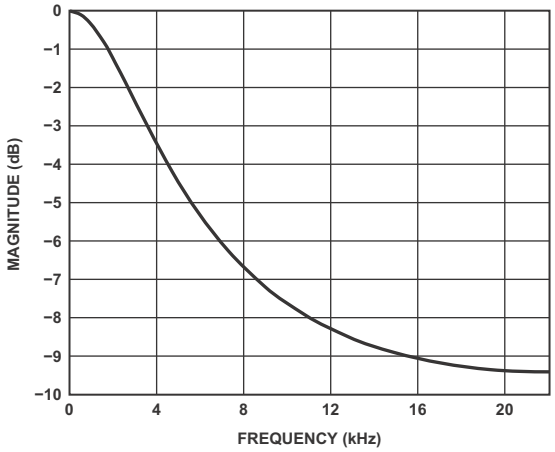


Figure 28. De-Emphasis Frequency Response, Sampling Rate = 44.1 kHz

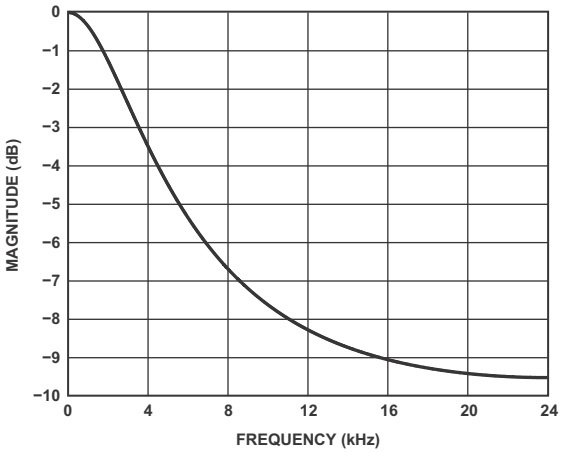


Figure 29. De-Emphasis Frequency Response, Sampling Rate = 48 kHz

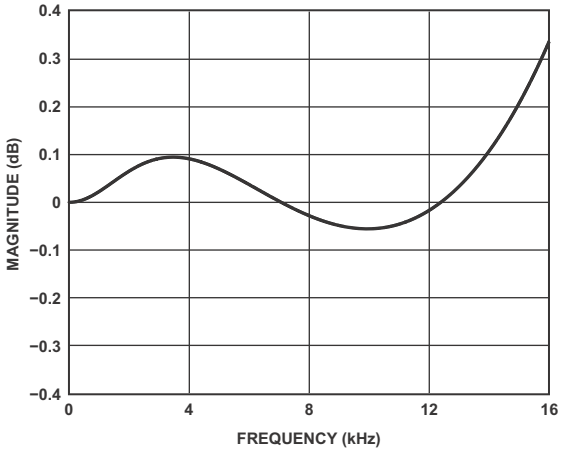


Figure 30. De-Emphasis Error, Sampling Rate = 32 kHz

Figure 33 shows the top view of the ADSP-BF52xC processor ball configuration.

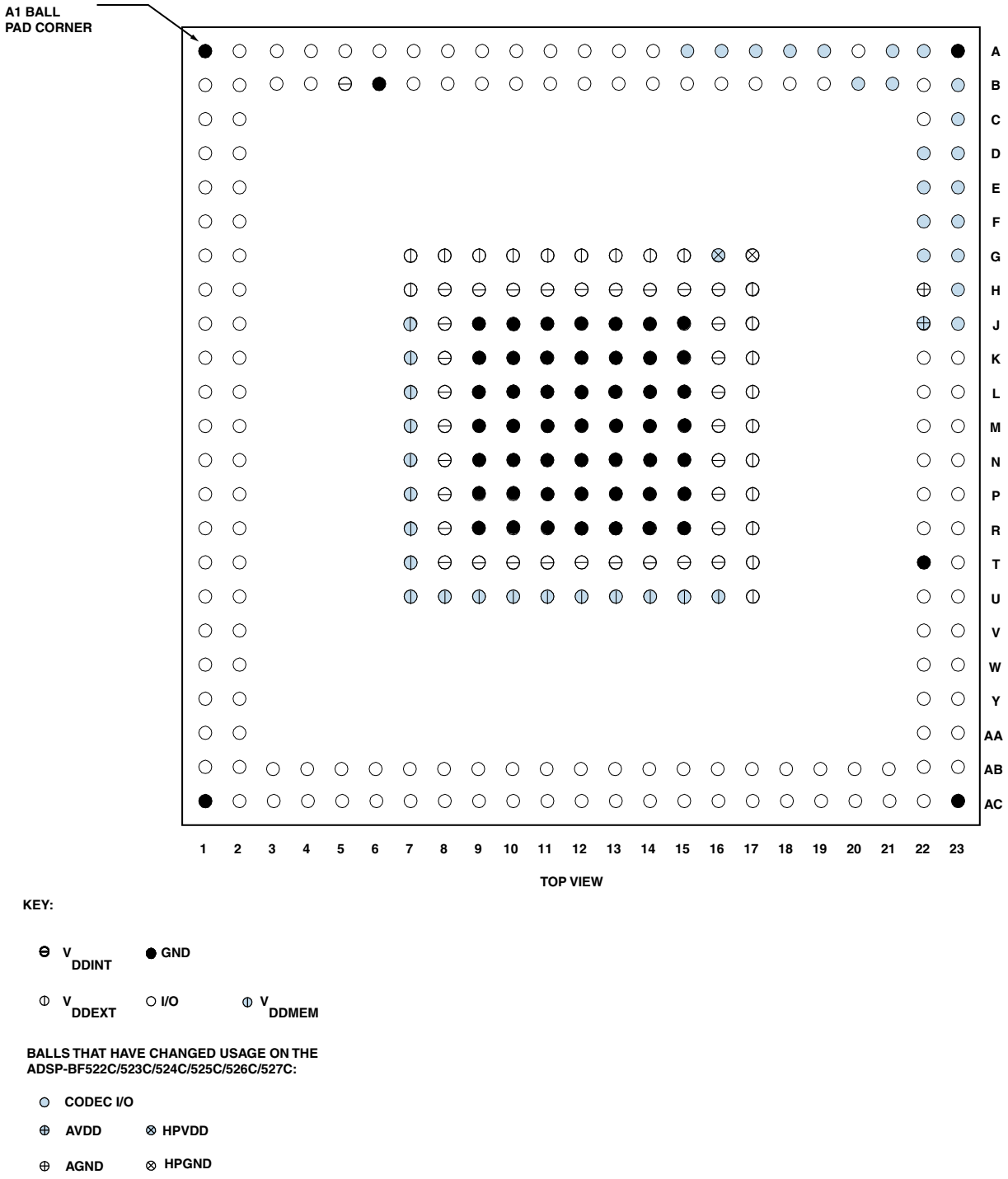


Figure 33. ADSP-BF52xC Processor Ball Configuration (Top View)

Figure 34 shows the bottom view of the ADSP-BF52xC processor ball configuration.

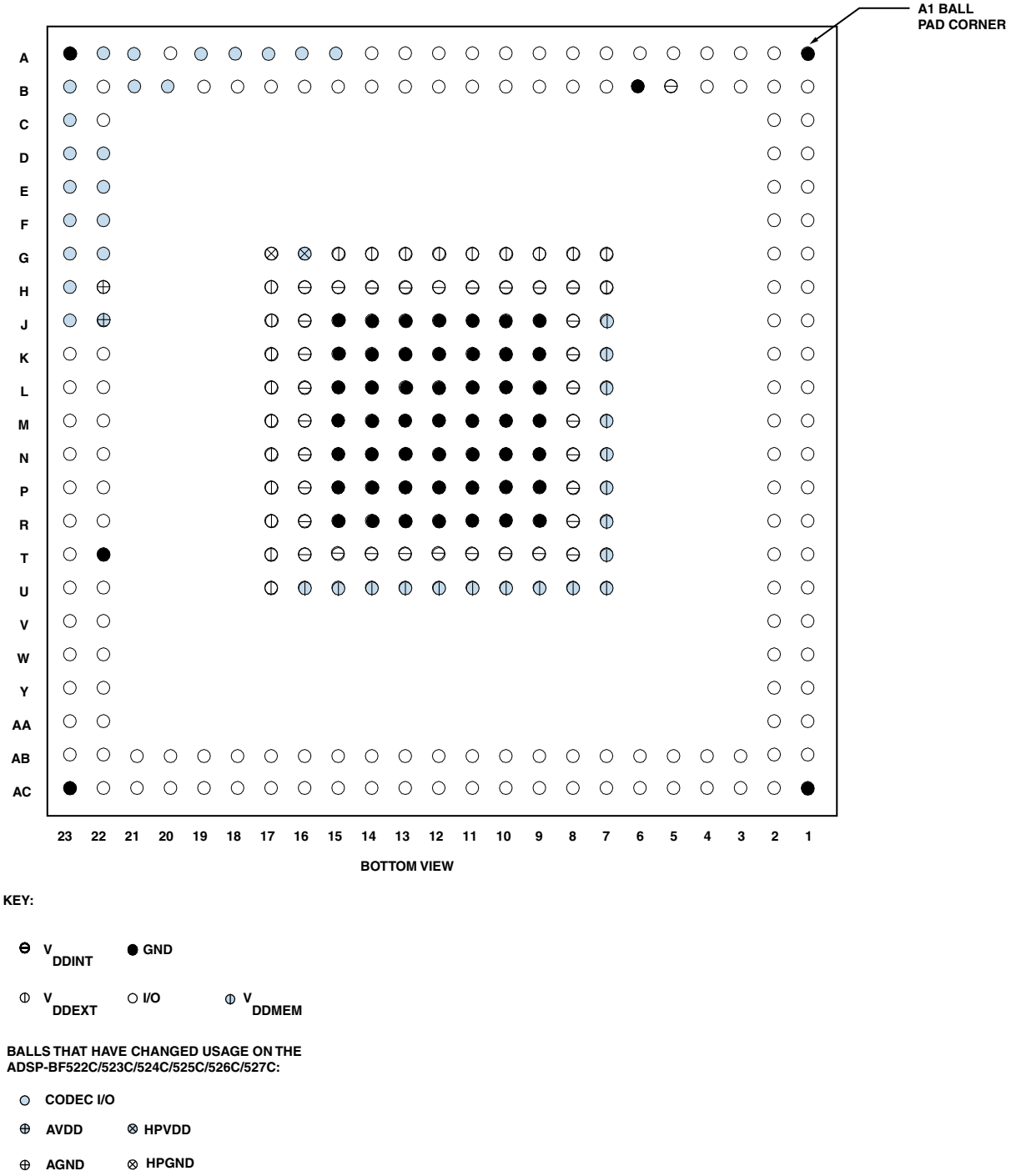


Figure 34. ADSP-BF52xC Processor Ball Configuration (Bottom View)

OUTLINE DIMENSIONS

Dimensions in Figure 35, 289-Ball CSP_BGA (BC-289-2) are shown in millimeters.

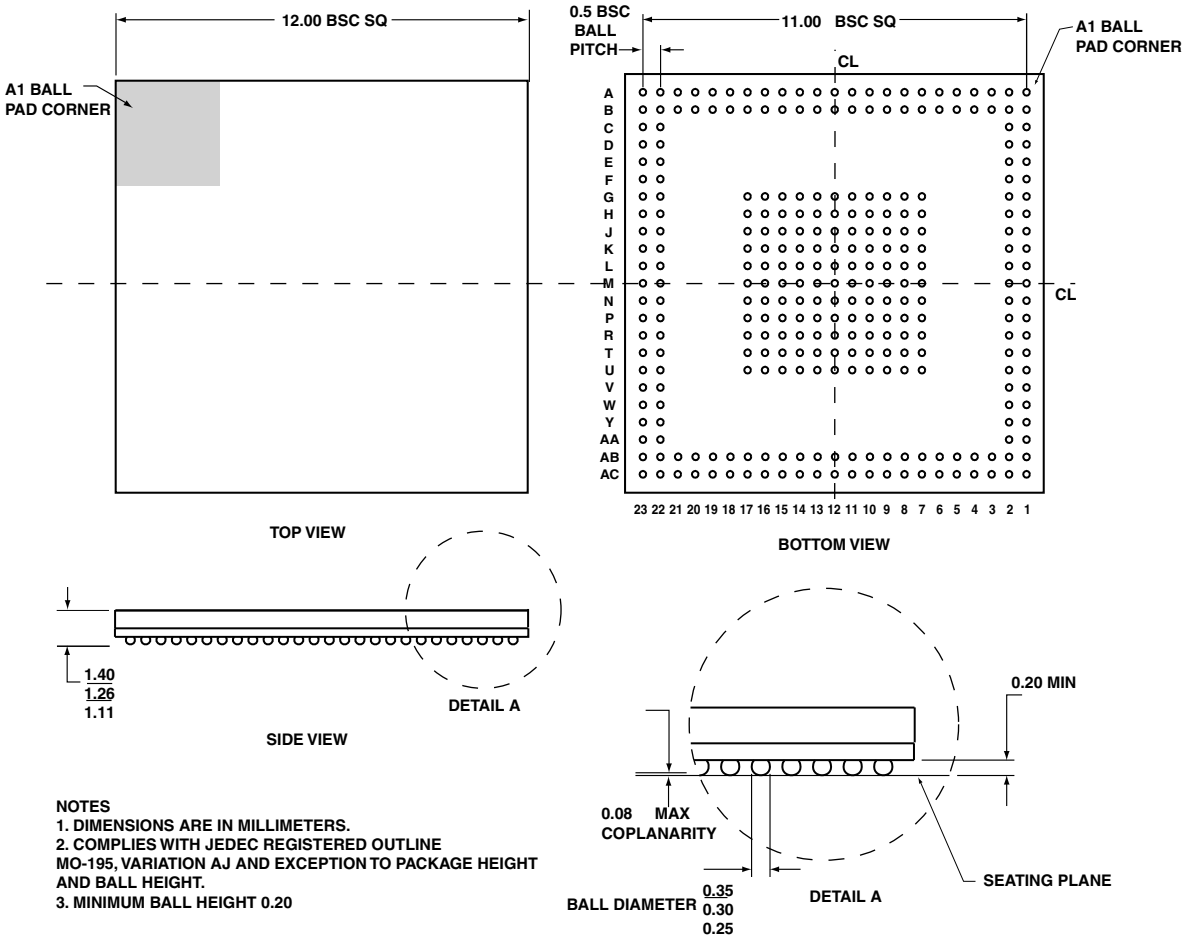


Figure 35. 289-Ball CSP_BGA (BC-289-2)

ORDERING GUIDE

Model[1]	Temperature Range[2]	Instruction Rate (Max)	Package Description	Package Option
ADSP-BF522KBCZ-3C2	0°C to +70°C	300 MHz	289-Ball Chip Scale Package Ball Grid Array (CSP_BGA)	BC-289-2
ADSP-BF522KBCZ-4C2	0°C to +70°C	400 MHz	289-Ball Chip Scale Package Ball Grid Array (CSP_BGA)	BC-289-2
ADSP-BF523KBCZ-5C2	0°C to +70°C	533 MHz	289-Ball Chip Scale Package Ball Grid Array (CSP_BGA)	BC-289-2
ADSP-BF523KBCZ-6C2	0°C to +70°C	600 MHz	289-Ball Chip Scale Package Ball Grid Array (CSP_BGA)	BC-289-2
ADSP-BF524KBCZ-3C2	0°C to +70°C	300 MHz	289-Ball Chip Scale Package Ball Grid Array (CSP_BGA)	BC-289-2
ADSP-BF524KBCZ-4C2	0°C to +70°C	400 MHz	289-Ball Chip Scale Package Ball Grid Array (CSP_BGA)	BC-289-2
ADSP-BF525KBCZ-5C2	0°C to +70°C	533 MHz	289-Ball Chip Scale Package Ball Grid Array (CSP_BGA)	BC-289-2
ADSP-BF525KBCZ-6C2	0°C to +70°C	600 MHz	289-Ball Chip Scale Package Ball Grid Array (CSP_BGA)	BC-289-2
ADSP-BF526KBCZ-3C2	0°C to +70°C	300 MHz	289-Ball Chip Scale Package Ball Grid Array (CSP_BGA)	BC-289-2
ADSP-BF526KBCZ-4C2	0°C to +70°C	400 MHz	289-Ball Chip Scale Package Ball Grid Array (CSP_BGA)	BC-289-2
ADSP-BF527KBCZ-5C2	0°C to +70°C	533 MHz	289-Ball Chip Scale Package Ball Grid Array (CSP_BGA)	BC-289-2
ADSP-BF527KBCZ-6C2	0°C to +70°C	600 MHz	289-Ball Chip Scale Package Ball Grid Array (CSP_BGA)	BC-289-2

[1] Z = RoHS Compliant Part.

[2] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 21 for junction temperature (T_J) specification which is the only temperature specification.

D06876-0-3/10(A)