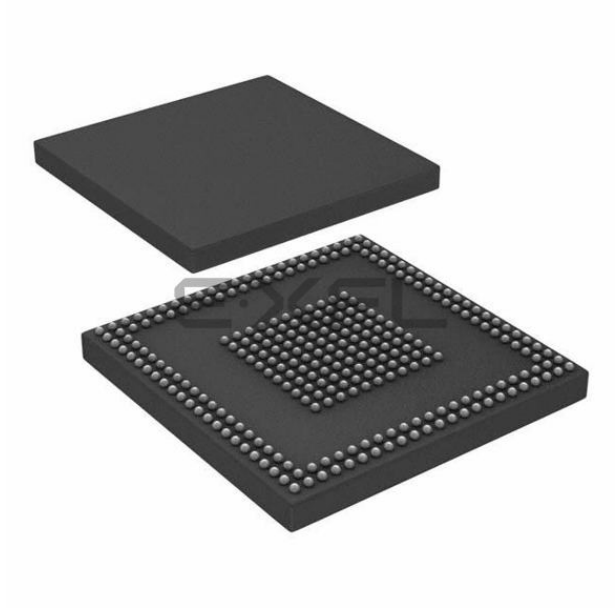

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	DMA, Ethernet, I²C, PPI, SPI, SPORT, UART, USB
Clock Rate	600MHz
Non-Volatile Memory	ROM (32kB)
On-Chip RAM	132kB
Voltage - I/O	1.8V, 2.5V, 3.3V
Voltage - Core	1.10V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	289-LFBGA, CSPBGA
Supplier Device Package	289-CSPBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf527kbcz-6c2

TABLE OF CONTENTS

REVISION HISTORY

3/10—Rev. 0 to Rev. A

Revised the following figures.
Recommended Application Circuit Using SPI Control 13
Recommended Application Circuit Using TWI Control .. 14

Added Sampling Rate = 48 kHz to all figures in
Converter Filter Response 30

Revised Ordering Guide 36

GENERAL DESCRIPTION

This document describes the differences between the ADSP-BF52xC and the ADSP-BF52x standard Blackfin® product. Please refer to the published ADSP-BF52x data sheet for general description and specifications. This document only describes the differences from that data sheet.

The ADSP-BF52xC processors add a low power, high quality stereo audio codec for portable digital audio applications with one set of stereo programmable gain amplifier (PGA) line inputs and one monaural microphone input. It features two 24-bit analog-to-digital converter (ADC) channels and two 24-bit digital-to-analog (DAC) converter channels.

The codec can operate as a master or a slave. It supports various master clock frequencies, including 12 MHz or 24 MHz for USB devices; standard 256 × f_S or 384 × f_S based rates, such as 12.288 MHz and 24.576 MHz; and many common audio sampling rates, such as 96 kHz, 88.2 kHz, 48 kHz, 44.1 kHz, 32 kHz, 24 kHz, 22.05 kHz, 16 kHz, 12 kHz, 11.025 kHz, and 8 kHz.

The codec can operate at power supplies as low as 1.8 V for the analog circuitry and as low as 1.8 V for the digital circuitry. The maximum voltage supply is 3.6 V for all supplies.

The codec software-programmable stereo output options provide the programmer with many application possibilities because the device can be used as a headphone driver or as a speaker driver. Its volume control functions provide a large range of gain control of the audio signal.

CODEC DESCRIPTION

The ADSP-BF52xC codec contains a central clock source, called the codec master clock (CODEC_MCLK) that produces a reference clock for all internal audio data processing and synchronization. When using an external clock source to drive the CODEC_MCLK pin, care should be taken to select a clock source with less than 50 ps of jitter. Without careful generation of the CODEC_MCLK signal, the digital audio quality will suffer.

To enable the codec to generate the central reference clock in a system, connect a crystal oscillator between the XTI/CODEC_MCLK input pin and the XTO output pin.

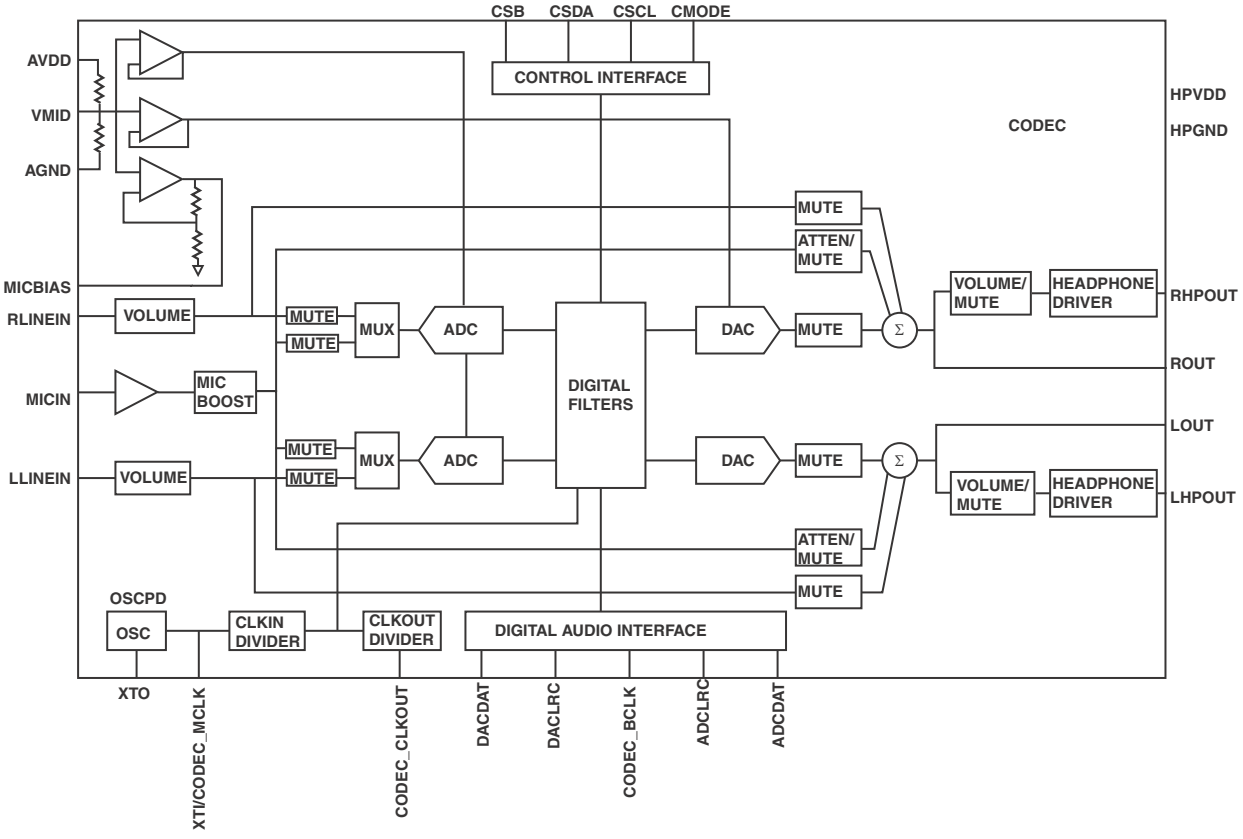


Figure 1. Codec Block Diagram

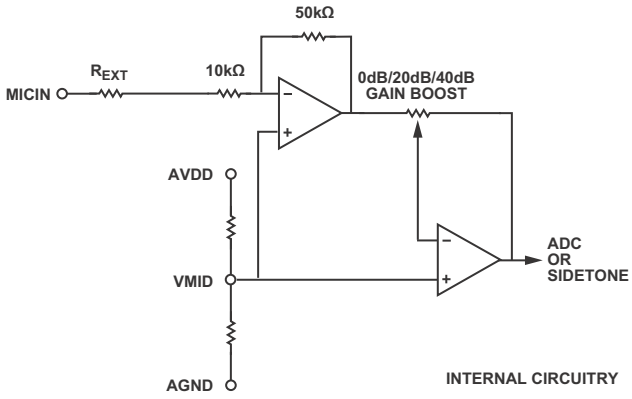


Figure 3. Microphone Input to ADC

The first gain stage is composed of a low noise operational amplifier set to an inverting configuration with integrated 50 kΩ feedback and 10 kΩ input resistors. The default microphone input signal gain is 14 dB. An external resistor (R_{EXT}) can be connected in series with the MICIN pin to reduce the first-stage gain of the microphone input signal to as low as 0 dB by using the following equation:

Microphone Input Gain = 50 kΩ/(10 kΩ + R_{EXT})

The second-stage gain of the microphone signal path is derived from the internal microphone boost circuitry. The available settings are 0 dB, 20 dB, and 40 dB and are controlled by the MICBOOST (Register R4, Bit D0) and MICBOOST2 (Register R4, Bit D8) bits. To achieve 20 dB of secondary gain boost, the programmer can select either MICBOOST or MICBOOST2. To achieve 40 dB of secondary microphone signal gain, the programmer must select both MICBOOST and MICBOOST2.

The MUTEMIC bit (Register R4, Bit D1) mutes the microphone input signal to the ADC.

When using either the line or microphone inputs, the maximum full-scale input to the ADC is 1.0 V rms when AVDD = 3.3 V. Do not apply an input voltage larger than full-scale to avoid overloading the ADC, which causes distortion of sound and deterioration of audio quality. For best sound quality in both microphone and line inputs, gain should be carefully configured so that the ADC receives a signal equal to its full-scale. This maximizes the signal-to-noise ratio for best total audio quality.

Bypass and Sidetone Paths to Output

The line and microphone inputs can be routed and mixed directly to the output terminals by programming the SIDETONE (Register R4, Bit D5) and BYPASS (Register R4, Bit D3) registers. In both modes, the analog input signal is routed directly to the output terminals and is not digitally converted. The bypass signal at the output mixer is the same level as the output of the PGA associated with each line input.

The sidetone signal at the output mixer can be attenuated from –6 dB to –15 dB in steps of –3 dB by configuring the SIDEATT (Register R4, Bit D6 and Bit D7) control register bits. The selected level of attenuation occurs after the initial microphone signal amplification from the microphone first and second stage gains.

Line and Headphone Outputs

The DAC outputs, the microphone (the sidetone path), and the line inputs (the bypass path) are summed at an output mixer (see Figure 4). This output signal is then applied to both the stereo line outputs and stereo headphone outputs.

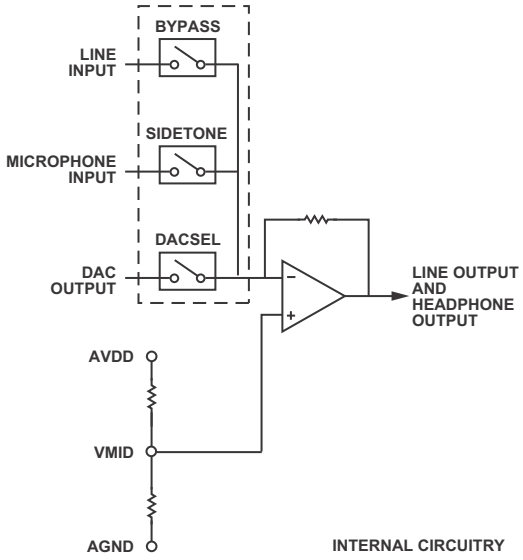


Figure 4. Output Signal Chain

The codec has a set of efficient headphone amplifier outputs, LHPOUT and RHPOUT, that are able to drive 16 Ω or 32 Ω headphones (shown in Figure 5).

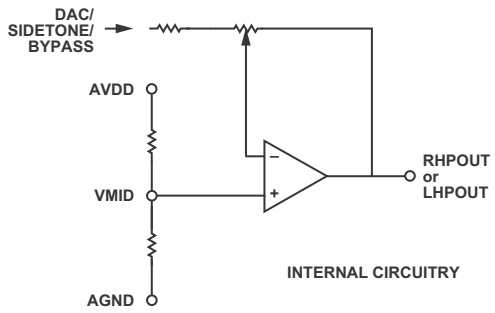


Figure 5. Headphone Output

Like the line inputs, the LHPOUT and RHPOUT volumes, by default, are independently adjusted by setting the LHPVOL (Register R2, Bit D0 to Bit D6) and RHPVOL (Register R3, Bit D0 to Bit D6) bits of the headphone output control registers. The headphone outputs can be muted by writing codes less than 0110000 to the LHPVOL and RHPVOL bits.

The programmer can simultaneously load the volume control of both channels by writing to the LRHPBOTH (Register R2, Bit D8) and RLHPBOTH (Register R3, Bit D8) bits of the left- or right-channel DAC volume registers.

The maximum output level of the headphone outputs is 1.0 V rms when AVDD and HPVDD = 3.3 V. To suppress audible pops and clicks, the headphone and line outputs are held at the VMID dc voltage level when the device is set to standby mode or when the headphone outputs are muted.

The stereo line outputs of the codec, the LOUT and ROUT pins, can drive a load impedance of 10 kΩ and 50 pF. The line output signal levels are not adjustable at the output mixer, which has a fixed gain of 0 dB. The maximum output level of the line outputs is 1.0 V rms when AVDD = 3.3 V.

DIGITAL AUDIO INTERFACE

The digital audio input can support the following digital audio communication protocols: right-justified mode, left-justified mode, I²S mode, and frame sync mode. See Figure 6 on Page 6 through Figure 10 on Page 7.

The mode selection is performed by writing to the FORMAT bits of the digital audio interface register (Register R7, Bit D1 and Bit D0). All modes are MSB first and operate with data of 16 to 32 bits.

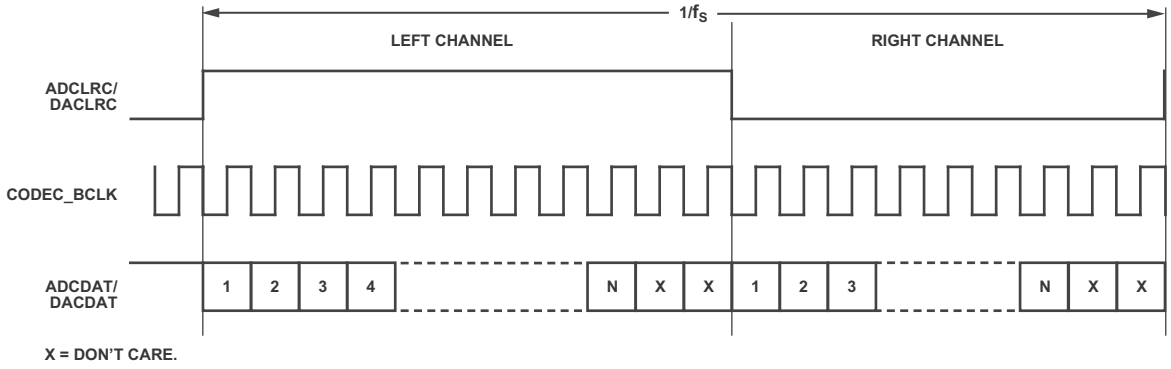


Figure 6. Left-Justified Audio Input Mode

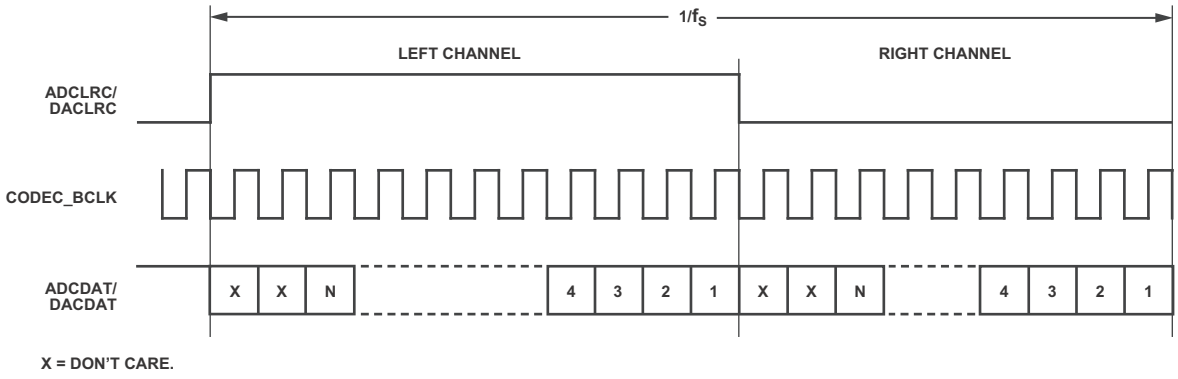


Figure 7. Right-Justified Audio Input Mode

Recording Mode

The digital audio interface sends the ADC digital filter data to the ADCDAT output pin for recording. The ADCDAT data stream multiplexes the left- and right-channel audio data in the time domain. The ADCLRC clock signal separates left- and right-channel digital audio frames on the ADCDAT lines.

The CODEC_BCLK signal clocks the digital audio data within the frames. The CODEC_BCLK signal is either an input or an output depending on whether the codec is in master or slave mode. During a recording operation, ADCDAT and ADCLRC must be synchronous to the CODEC_BCLK signal to avoid data corruption.

Playback Mode

The digital audio interface receives data on the DACDAT input pin for playback. The digital audio data stream on the DACDAT pin is time-domain-multiplexed left and right channel audio data. The DACLRC clock signal separates left and right channel digital audio frames on the DACDAT lines.

The CODEC_BCLK signal clocks the digital audio data within the frames. The CODEC_BCLK signal is either an input or an output depending on whether the codec is in master or slave mode. During a playback operation, DACDAT and DACLRC must be synchronous to the CODEC_BCLK signal to avoid data corruption.

Digital Audio Data Sampling Rate

To accommodate a wide variety of commonly used DAC and ADC sampling rates, the codec allows for two modes of operation, normal and USB, selected by the USB bit (Register R8, Bit D0).

The sampling rate is generated as a fixed divider from the CODEC_MCLK signal. Because all audio processing references the CODEC_MCLK signal, corruption of this signal will corrupt the quality of the audio at the codec output. The ADCLRC/ADCDAT/CODEC_BCLK or DACLRC/DACDAT/CODEC_BCLK signals must be synchronized with CODEC_MCLK in the digital audio interface circuit.

CODEC_MCLK must be faster or equal to the CODEC_BCLK frequency to guarantee that no data is lost during data synchronization. The CODEC_BCLK frequency should be greater than the sampling rate × word length × 2. Ensuring that the CODEC_BCLK frequency is greater than this, guarantees that all valid data bits are captured by the digital audio interface circuitry. For example, if a 32 kHz digital audio sampling rate with a 32-bit word length is desired, CODEC_BCLK = 2.048 MHz.

Normal Mode

In normal mode, the codec supports digital audio sampling rates from 8 kHz to 96 kHz. Normal mode supports 256 × f_S and 384 × f_S based clocks. To select the desired sampling rate, the programmer must set the appropriate sampling rate register in the SR control bits (Register R8, Bit D2 to Bit D5) and match this selection to the core clock frequency that is pulsed on the CODEC_MCLK pin. See Table 1 for sampling rates in normal mode.

Table 1. Sampling Rate Lookup Table, Normal Mode (USB Disabled)

CODEC_MCLK (CLKDIV2 = 0)	CODEC_MCLK (CLKDIV2 = 1)	ADC Sampling Rate (ADCLRC)	DAC Sampling Rate (DACLRC)	USB	SR [3:0]	BOSR	CODEC_BCLK (MS = 1)[1]
12.288 MHz	24.576 MHz	8 kHz (CODEC_MCLK/1536)	8 kHz (CODEC_MCLK/1536)	0	0011	0	CODEC_MCLK/4
		8 kHz (CODEC_MCLK/1536)	48 kHz (CODEC_MCLK/256)	0	0010	0	CODEC_MCLK/4
		12 kHz (CODEC_MCLK/1024)	12 kHz (CODEC_MCLK/1024)	0	0100	0	CODEC_MCLK/4
		16 kHz (CODEC_MCLK/768)	16 kHz (CODEC_MCLK/768)	0	0101	0	CODEC_MCLK/4
		24 kHz (CODEC_MCLK/512)	24 kHz (CODEC_MCLK/512)	0	1110	0	CODEC_MCLK/4
		32 kHz (CODEC_MCLK/384)	32 kHz (CODEC_MCLK/384)	0	0110	0	CODEC_MCLK/4
		48 kHz (CODEC_MCLK/256)	8 kHz (CODEC_MCLK/1536)	0	0001	0	CODEC_MCLK/4
		48 kHz (CODEC_MCLK/256)	48 kHz (CODEC_MCLK/256)	0	0000	0	CODEC_MCLK/4
		96 kHz (CODEC_MCLK/128)	96 kHz (CODEC_MCLK/128)	0	0111	0	CODEC_MCLK/2
11.2896 MHz	22.5792 MHz	8.0182 kHz (CODEC_MCLK/1408)	8.0182 kHz (CODEC_MCLK/1408)	0	1011	0	CODEC_MCLK/4
		8.0182 kHz (CODEC_MCLK/1408)	44.1 kHz (CODEC_MCLK/256)	0	1010	0	CODEC_MCLK/4
		11.025 kHz (CODEC_MCLK/1024)	11.025 kHz (CODEC_MCLK/1024)	0	1100	0	CODEC_MCLK/4
		22.05 kHz (CODEC_MCLK/512)	22.05 kHz (CODEC_MCLK/512)	0	1101	0	CODEC_MCLK/4
		44.1 kHz (CODEC_MCLK/256)	8.0182 kHz (CODEC_MCLK/1408)	0	1001	0	CODEC_MCLK/4
		44.1 kHz (CODEC_MCLK/256)	44.1 kHz (CODEC_MCLK/256)	0	1000	0	CODEC_MCLK/4
		88.2 kHz (CODEC_MCLK/128)	88.2 kHz (CODEC_MCLK/128)	0	1111	0	CODEC_MCLK/2
18.432 MHz	36.864 MHz	8 kHz (CODEC_MCLK/2304)	8 kHz (CODEC_MCLK/2304)	0	0011	1	CODEC_MCLK/6
		8 kHz (CODEC_MCLK/2304)	48 kHz (CODEC_MCLK/384)	0	0010	1	CODEC_MCLK/6
		12 kHz (CODEC_MCLK/1536)	12 kHz (CODEC_MCLK/1536)	0	0100	1	CODEC_MCLK/6
		16 kHz (CODEC_MCLK/1152)	16 kHz (CODEC_MCLK/1152)	0	0101	1	CODEC_MCLK/6
		24 kHz (CODEC_MCLK/768)	24 kHz (CODEC_MCLK/768)	0	1110	1	CODEC_MCLK/6
		32 kHz (CODEC_MCLK/576)	32 kHz (CODEC_MCLK/576)	0	0110	1	CODEC_MCLK/6
		48 kHz (CODEC_MCLK/384)	48 kHz (CODEC_MCLK/384)	0	0000	1	CODEC_MCLK/6
		48 kHz (CODEC_MCLK/384)	8 kHz (CODEC_MCLK/2304)	0	0001	1	CODEC_MCLK/6
		96 kHz (CODEC_MCLK/192)	96 kHz (CODEC_MCLK/192)	0	0111	1	CODEC_MCLK/3
16.9344 MHz	33.8688 MHz	8.0182 kHz (CODEC_MCLK/2112)	8.0182 kHz (CODEC_MCLK/2112)	0	1011	1	CODEC_MCLK/6
		8.0182 kHz (CODEC_MCLK/2112)	44.1 kHz (CODEC_MCLK/384)	0	1010	1	CODEC_MCLK/6
		11.025 kHz (CODEC_MCLK/1536)	11.025 kHz (CODEC_MCLK/1536)	0	1100	1	CODEC_MCLK/6
		22.05 kHz (CODEC_MCLK/768)	22.05 kHz (CODEC_MCLK/768)	0	1101	1	CODEC_MCLK/6
		44.1 kHz (CODEC_MCLK/384)	8.0182 kHz (CODEC_MCLK/2112)	0	1001	1	CODEC_MCLK/6
		44.1 kHz (CODEC_MCLK/384)	44.1 kHz (CODEC_MCLK/384)	0	1000	1	CODEC_MCLK/6
		88.2 kHz (CODEC_MCLK/192)	88.2 kHz (CODEC_MCLK/192)	0	1111	1	CODEC_MCLK/3

[1] CODEC_BCLK frequency is for master mode and slave right-justified mode only.

USB Mode

In USB mode, the codec supports digital audio sampling rates from 8 kHz to 96 kHz. USB mode is enabled on the codec to support the common universal serial bus (USB) clock rate of 12 MHz, or to support 24 MHz if the CLKDIV2 control register bit is activated. The programmer must set the appropriate sampling rate in the SR control bits (Register R8, Bit D2 to Bit D5). See Table 2 for sampling rates in USB mode.

Table 2. Sampling Rate Lookup Table, USB Mode (USB Enabled)

CODEC_MCLK (CLKDIV2 = 0)	CODEC_MCLK (CLKDIV2 = 1)	ADC Sampling Rate (ADCLRC)	DAC Sampling Rate (DACLRC)	USB	SR [3:0]	BOSR	CODEC_BCLK (MS = 1)[1]
12.000 MHz	24.000 MHz	8 kHz (CODEC_MCLK/1500)	8 kHz (CODEC_MCLK/1500)	1	0011	0	CODEC_MCLK
		8 kHz (CODEC_MCLK/1500)	48 kHz (CODEC_MCLK/250)	1	0010	0	CODEC_MCLK
		8.0214 kHz (CODEC_MCLK/1496)	8.0214 kHz (CODEC_MCLK/1496)	1	1011	1	CODEC_MCLK
		8.0214 kHz (CODEC_MCLK/1496)	44.118 kHz (CODEC_MCLK/272)	1	1010	1	CODEC_MCLK
		11.0259 kHz (CODEC_MCLK/1088)	11.0259 kHz (CODEC_MCLK/1088)	1	1100	1	CODEC_MCLK
		12 kHz (CODEC_MCLK/1000)	12 kHz (CODEC_MCLK/1000)	1	1000	0	CODEC_MCLK
		16 kHz (CODEC_MCLK/750)	16 kHz (CODEC_MCLK/750)	1	1010	0	CODEC_MCLK
		22.0588 kHz (CODEC_MCLK/544)	22.0588 kHz (CODEC_MCLK/544)	1	1101	1	CODEC_MCLK
		24 kHz (CODEC_MCLK/500)	24 kHz (CODEC_MCLK/500)	1	1110	0	CODEC_MCLK
		32 kHz (CODEC_MCLK/375)	32 kHz (CODEC_MCLK/375)	1	0110	0	CODEC_MCLK
		44.118 kHz (CODEC_MCLK/272)	8.0214 kHz (CODEC_MCLK/1496)	1	1001	1	CODEC_MCLK
		44.118 kHz (CODEC_MCLK/272)	44.118 kHz (CODEC_MCLK/272)	1	1000	1	CODEC_MCLK
		48 kHz (CODEC_MCLK/250)	8 kHz (CODEC_MCLK/1500)	1	0001	0	CODEC_MCLK
		48 kHz (CODEC_MCLK/250)	48 kHz (CODEC_MCLK/250)	1	0000	0	CODEC_MCLK
		88.235 kHz (CODEC_MCLK/136)	88.235 kHz (CODEC_MCLK/136)	1	1111	1	CODEC_MCLK
		96 kHz (CODEC_MCLK/125)	96 kHz (CODEC_MCLK/125)	1	0111	0	CODEC_MCLK

[1] CODEC_BCLK frequency is for master mode and slave right-justified mode only.

SOFTWARE CONTROL INTERFACE

The software control interface provides access to the programmer-selectable control registers and can operate with a 2-wire (TWI) or 3-wire (SPI) interface, depending on the setting of the CMODE pin. If the CMODE pin is set to 0, the 2-wire interface is selected; if 1, the 3-wire interface is selected.

Within each control register is a control data-word consisting of 16 bits, MSB first. Bit B15 to Bit B9 are the register map address, and Bit B8 to Bit B0 are register data for the associated register map.

When 2-wire (TWI) mode is selected, CSDA generates the serial control data-word; CSCL clocks the serial data; and CSB determines the TWI device address. If the CSB pin is set to 0, the address selected is 0011010; if 1, the address is 0011011.

When 3-wire (SPI) mode is selected, CSDA generates the control data-word, CSCL clocks the control data-word into the codec, and CSB latches in the control data-word.

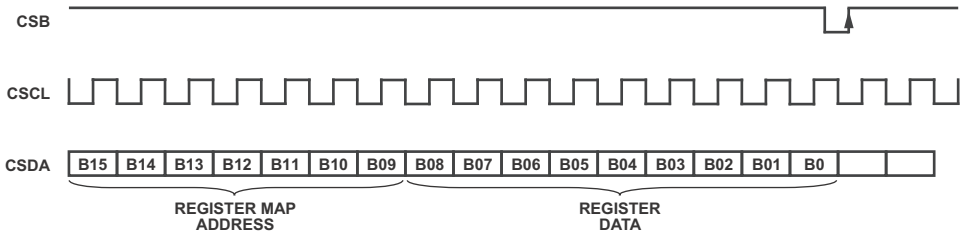


Figure 11. Codec SPI Serial Interface

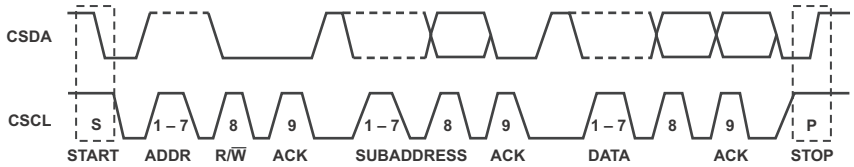
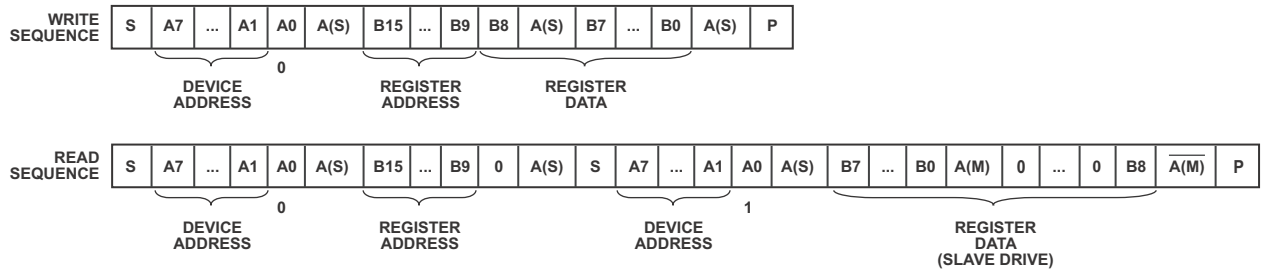


Figure 12. Codec TWI Serial Interface



S/P = START/STOP BIT.
A0 = I²C R/$\overline{W}$ BIT.
A(S) = ACKNOWLEDGE BY SLAVE.
A(M) = ACKNOWLEDGE BY MASTER.
$\overline{A(M)}$ = ACKNOWLEDGE BY MASTER (INVERSION).

Figure 13. Codec TWI Write and Read Sequences

CODEC PIN DESCRIPTIONS

Table 3 shows the signals added to the ADSP-BF52xC processor for the embedded codec. Please refer to the published ADSP-BF52x data sheet for descriptions of other signals for the processor.

Table 3. Codec Pin Descriptions

Pin Name	Type	Function	Pull-Up/Down
Codec			
CODEC_CLKOUT	O	Codec Clock Output	None
CODEC_BCLK	I/O	Codec Digital Audio Bit Clock	Internal Pull-down[1]
DACDAT	I	Codec Digital Audio Data (DAC) Input	None
DACLRC	I/O	Codec DAC Sample Rate Left/Right Clock	Internal Pull-down[1]
ADCDAT	O	Codec ADC Digital Audio Data Output	None
ADCLRC	I/O	Codec ADC Sample Rate Left/Right Clock	Internal Pull-down[1]
CMODE	I	Codec Control Interface Selection	Internal Pull-up[1]
CSB	I	Codec Chip Select Interface Address Selection	Internal Pull-up[1]
CSDA	I/O	Codec Data Input	None
CSCL	I/O	Codec Data Clock	None
XTI/CODEC_MCLK	I	Codec Crystal Input/ Clock Input	None
XTO	O	Codec Crystal Output	None
LHPOUT	O	Codec Left Channel Headphone Output (Analog Output)	None
RHPOUT	O	Codec Right Channel Headphone Output (Analog Output)	None
LOUT	O	Codec Left Channel Line Output (Analog Output)	None
ROUT	O	Codec Right Channel Line Output (Analog Output)	None
VMID	O	Codec Mid-rail Reference Decoupling Point (Analog Output)	None
MICBIAS	O	Codec Electret Microphone Bias (Analog Output)	None
MICIN	I	Codec Microphone Input; (Analog Input, AC Coupled)	None
RLINEIN	I	Codec Right Channel Line Input (Analog Input, AC Coupled)	None
LLINEIN	I	Codec Left Channel Line Input (Analog Input, AC Coupled)	None
AVDD	P	Codec Analog V_{DD}	N/A
AGND	P	Codec Analog Ground	N/A
CVDD	P	Codec Digital V_{DD}	N/A
HPVDD	P	Codec Analog Headphone V_{DD}	N/A
HPGND	P	Codec Headphone Ground	N/A

[1] To conserve power, the pull-up/pull-down is only present when the control register interface is active (= 0).

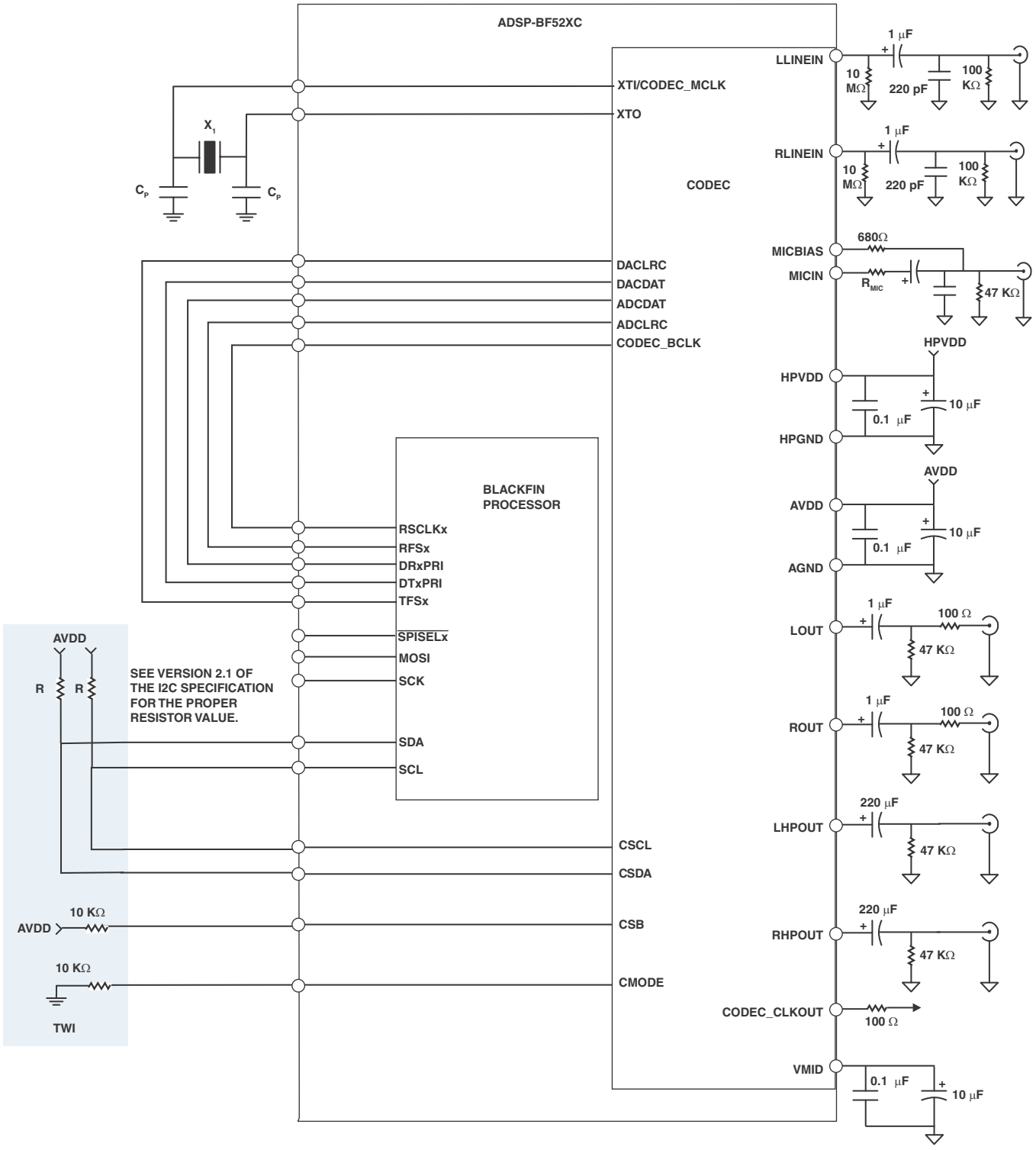


Figure 15. Recommended Application Circuit Using TWI Control

REGISTER DETAILS

Register	Address	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 0 Left-Channel ADC Input Volume on Page 16	0x00	LRINBOTH	LINMUTE	0	LINVOL					
		Default = 010010111								
Register 1 Right-Channel ADC Input Volume on Page 17	0x01	RLINBOTH	RINMUTE	0	RINVOL					
		Default = 010010111								
Register 2 Left-Channel DAC Volume on Page 17	0x02	LRHPBOTH	LZCEN	LHPVOL						
		Default = 001111001								
Register 3 Right-Channel DAC Volume on Page 18	0x03	RLHPBOTH	RZCEN	RHPVOL						
		Default = 001111001								
Register 4 Analog Audio Path on Page 18	0x04	MICBOOST2	SIDEATT[1:0]		SIDETONE	DACSEL	BYPASS	INSEL	MUTEMIC	MICBOOST
		Default = 000001010								
Register 5 Digital Audio Path on Page 19	0x05	0	0	0	0	HPOR	DACMU	DEEMPH[1:0]		ADC HPD
		Default = 000001000								
Register 6 Power Management on Page 19	0x06	0	POWEROFF	CLKOUTPD	OSCPD	OUTPD	DACPD	ADCPD	MICPD	LINEINPD
		Default = 010011111								
Register 7 Digital Audio I/F on Page 20	0x07	0	BCLKINV	MS	LRSWAP	LRP	WL[1:0]		FORMAT[1:0]	
		Default = 000001010								
Register 8 Sampling Rate on Page 20	0x08	0	CLKODIV2	CLKDIV2	SR[3:0]				BOSR	USB
		Default = 000000000								
Register 9 Active on Page 20	0x09	0	0	0	0	0	0	0	0	ACTIVE
		Default = 000000000								
Register 10 Software Reset on Page 20	0x0F	RESET								
		Default = 000000000								

Figure 16. Register Mapping

SPECIFICATIONS

$T_{Ambient}$ = 25°C, AVDD = VDDEXT = 3.3 V, HPVDD = 3.3 V, 1 kHz signal, f_S = 48 kHz, PGA gain = 0 dB, 24-bit audio data, unless otherwise noted.

OPERATING CONDITIONS

See operating conditions in the published ADSP-BF52xC data sheet.

Parameter	Conditions	Min	Typical	Max	Unit
AVDD[1]		1.8	3.3	3.6	V
HPVDD		1.8	3.3	3.6	V

[1] Note that AVDD must equal HPVDD.

CODEC ELECTRICAL CHARACTERISTICS

Parameter	Conditions	Min	Typical	Max	Unit
Line Input					
Input Signal Level (0 dB)			AVDD/3.3		V(rms)
Input Impedance	PGA gain = 0 dB		200		kΩ
	PGA gain = +33 dB		10		kΩ
	PGA gain = –34.5 dB		480		kΩ
Input Capacitance			10		pF
Signal-to-Noise Ratio (A-Weighted)	PGA gain = 0 dB, AVDD = 3.3 V	82	87		dB
	PGA gain = 0 dB, AVDD = 1.8 V		84		dB
Total Harmonic Distortion (THD)	–1 dBFS input, AVDD = 3.3 V	–80	–84		dB
	–1 dBFS input, AVDD = 1.8 V		–71	–60	dB
Channel Separation[1]			80		dB
Programmable Gain		–34.5	0	+33.5	dB
Gain Step			1.5		dB
Mute Attenuation			–80		dB
Microphone Input					
Input Signal Level			1		V(rms)
Signal-to-Noise Ratio (A-Weighted)	Microphone gain = 0 dB (R_{SOURCE} = 40 kΩ)		85		dB
Total Harmonic Distortion	–1 dBFS input, 0 dB gain, AVDD = 3.3 V		–75		dB
	–1 dBFS input, 0 dB gain, AVDD = 1.8 V		–65		dB
Power Supply Rejection Ratio			50		dB
Mute Attenuation			80		dB
Input Resistance			10		kΩ
Input Capacitance			10		pF
Microphone Bias					
Bias Voltage			0.75 × AVDD		V
Bias Current Source				3	mA
Noise in the Signal Bandwidth	20 Hz to 20 kHz		40		nV/√Hz

Parameter	Conditions	Min	Typical	Max	Unit
Line Output					
DAC	–1 dBFS input DAC + line output				
Full-Scale Output			AVDD/3.3		V(rms)
Signal-to-Noise Ratio (A-Weighted)	AVDD = 3.3 V	90	95		dB
	AVDD = 1.8 V	85	88		dB
THD + N	AVDD = 3.3 V		–80	–70	dB
	AVDD = 1.8 V		–80	–70	dB
Power Supply Rejection Ratio			50		dB
Channel Separation			80		dB
Headphone Output					
Full-Scale Output Voltage			AVDD/3.3		V(rms)
Maximum Output Power	R_L = 32 Ω		30		mW
	R_L = 16 Ω		60		mW
Signal-to-Noise Ratio (A-Weighted)	AVDD = 3.3 V	90	94		dB
	AVDD = 1.8 V	80	85		dB
THD + N	HPOUT = 10 mW		–65		dB
	HPOUT = 20 mW		–60		dB
Power Supply Rejection Ratio			50		dB
Mute Attenuation			80		dB
LIne Input To Line Output					
Full-Scale Output Voltage			AVDD/3.3		V(rms)
Signal-to-Noise Ratio (A-Weighted)	AVDD = 3.3 V		92		dB
	AVDD = 1.8 V		86		dB
Total Harmonic Distortion	AVDD = 3.3 V		–80		dB
	AVDD = 1.8 V		–80		dB
Power Supply Rejection			50		dB
Microphone Input To Headphone Output					
Full-Scale Output Voltage			AVDD/3.3		V(rms)
Signal-to-Noise Ratio (A-Weighted)	AVDD = 3.3 V		94		dB
	AVDD = 1.8 V		88		dB
Power Supply Rejection Ratio			50		dB
Programmable Attenuation		6		15	dB
Gain Step			3		dB
Mute Attenuation			80		dB

[1] Guaranteed but not tested.

ABSOLUTE MAXIMUM RATINGS

See absolute maximum ratings in the published ADSP-BF52x processor data sheet.

ESD SENSITIVITY

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PACKAGE INFORMATION

The information presented in Figure 17 and Table 15 provides details about the package branding for the ADSP-BF52xC processor. For a complete listing of product availability, see Ordering Guide on Page 36.

Figure 17. Product Information on Package

Table 15. Package Brand Information

Brand Key	Field Description
t	Temperature Range
pp	Package Type
Z	Lead Free Option
ccc	See Ordering Guide
vvvvvv.x	Assembly Lot Code
n.n	Silicon Revision
yyww	Date Code

TIMING SPECIFICATIONS

TWI Timing

Table 17. TWI Timing

Parameter		Test Conditions[1]	Min	Max	Unit
t_{SCS}	Start condition setup time		600		ns
t_{SCH}	Start condition hold time		600		ns
t_{PH}	CSCL pulse width high		600		ns
t_{PL}	CSCL pulse width low		1.3		µs
f_{SCL}	CSCL frequency		0	526	kHz
t_{DS}	Data setup time		100		ns
t_{DH}	Data hold time			900	ns
t_{RT}	CSDA and CSCL rise time			300	ns
t_{FT}	CSDA and CSCL fall time			300	ns
t_{HCS}	Stop condition setup time		600		ns

[1] AVDD, HPVDD, V_{DDEXT} = 3.3 V, AGND = 0 V, T_A = +25°C, Slave Mode, f_S = 48 kHz, XTI/CODEC_MCLK = 256 × f_S unless otherwise stated.

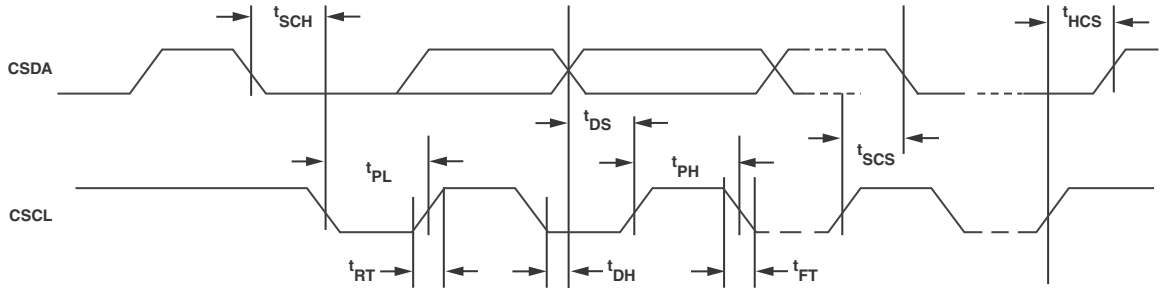


Figure 18. TWI Timing

Digital Audio Interface Slave Mode Timing

Table 19. Digital Audio Interface Slave Mode Timing

Parameter		Test Conditions[1]	Min	Max	Unit
t_{DS}	DACDAT setup time from CODEC_BCLK rising edge		10		ns
t_{DH}	DACDAT hold time from CODEC_BCLK rising edge		10		ns
t_{LRSU}	ADCLRC/DACLRC setup time to CODEC_BCLK rising edge		10		ns
t_{LRH}	ADCLRC/DACLRC hold time to CODEC_BCLK rising edge		10		ns
t_{DD}	ADCDAT propagation delay from CODEC_BCLK falling edge (external load of 70 pF)			30	ns
t_{BCH}	CODEC_BCLK pulse width high		25		ns
t_{BCL}	CODEC_BCLK pulse width low		25		ns
t_{BCY}	CODEC_BCLK cycle time		50		ns

[1] AVDD, HPVDD, V_{DDEXT} = 3.3 V, AGND = 0 V, T_A = +25°C, Slave Mode, f_S = 48 kHz, XTI/CODEC_MCLK = 256 × f_S unless otherwise stated.

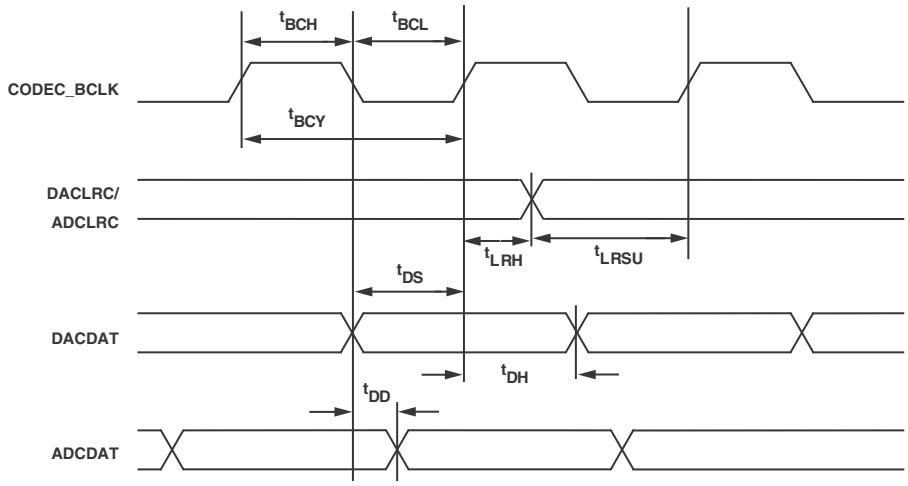


Figure 20. Digital Audio Interface Slave Mode Timing

Digital Audio Interface Master Mode Timing

Table 20. Digital Audio Interface Master Mode Timing

Parameter		Test Conditions[1]	Min	Max	Unit
t_{DST}	DACDAT setup time to CODEC_BCLK rising edge		30		ns
t_{DHT}	DACDAT hold time to CODEC_BCLK rising edge		10		ns
t_{DL}	ADCLRC/DACLRC propagation delay from CODEC_BCLK falling edge			10	ns
t_{DDA}	ADCDAT propagation delay from CODEC_BCLK falling edge			10	ns
t_{BCLKR}	CODEC_BCLK rising time (10 pF load)		10		ns
t_{BCLKF}	CODEC_BCLK falling time (10 pF load)		10		ns
t_{BCLKDS}	CODEC_BCLK duty cycle (normal and USB mode)		45:55	55:45	

[1] AVDD, HPVDD, V_{DDEXT} = 3.3 V, AGND = 0 V, T_A = +25°C, Slave Mode, f_S = 48 kHz, XTI/CODEC_MCLK = 256 × f_S unless otherwise stated.

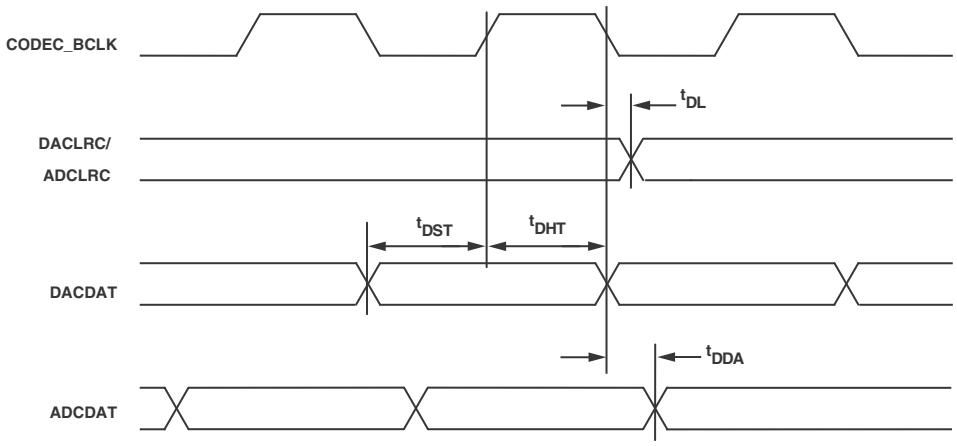


Figure 21. Digital Audio Interface Master Mode Timing

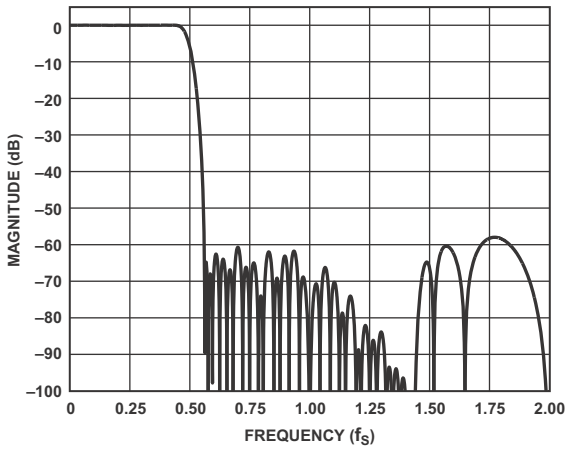


Figure 25. DAC Digital Filter Frequency Response, Sampling Rate = 48 kHz

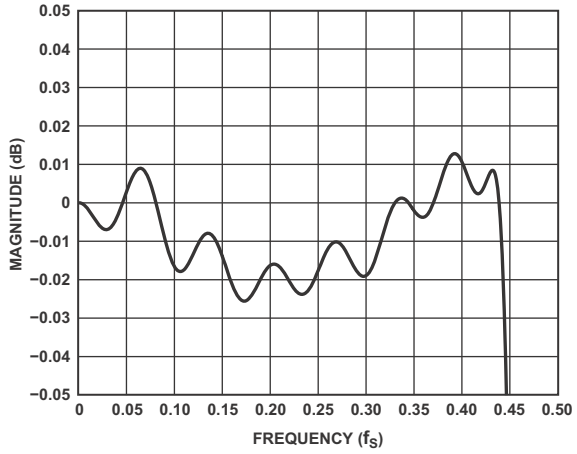


Figure 26. DAC Digital Filter Ripple, Sampling Rate = 48 kHz

DIGITAL DE-EMPHASIS

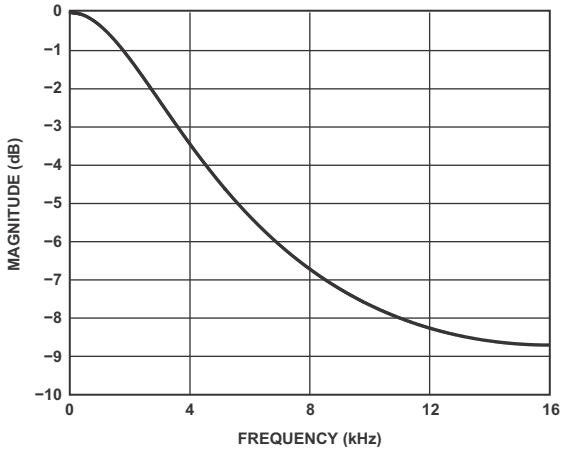


Figure 27. De-Emphasis Frequency Response, Sampling Rate = 32 kHz

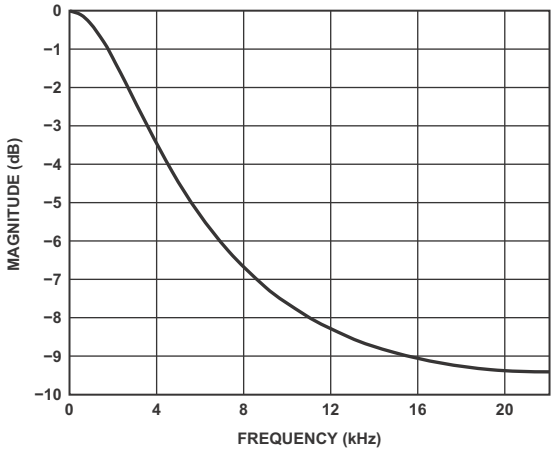


Figure 28. De-Emphasis Frequency Response, Sampling Rate = 44.1 kHz

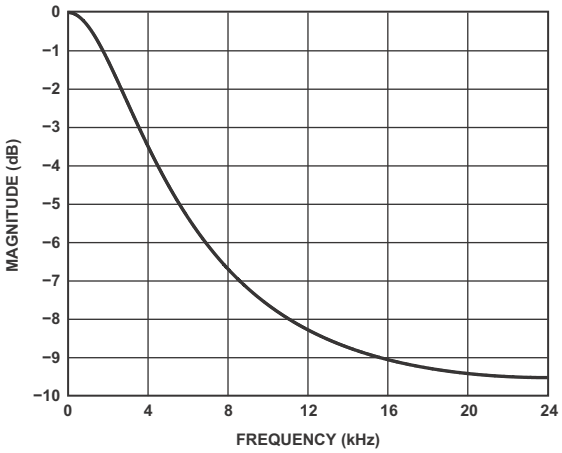


Figure 29. De-Emphasis Frequency Response, Sampling Rate = 48 kHz

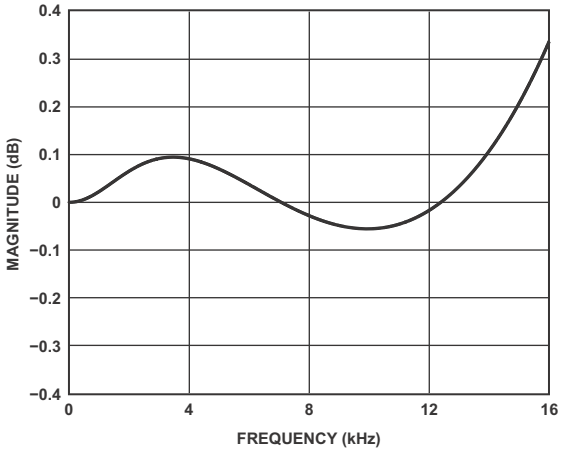


Figure 30. De-Emphasis Error, Sampling Rate = 32 kHz

Figure 33 shows the top view of the ADSP-BF52xC processor ball configuration.

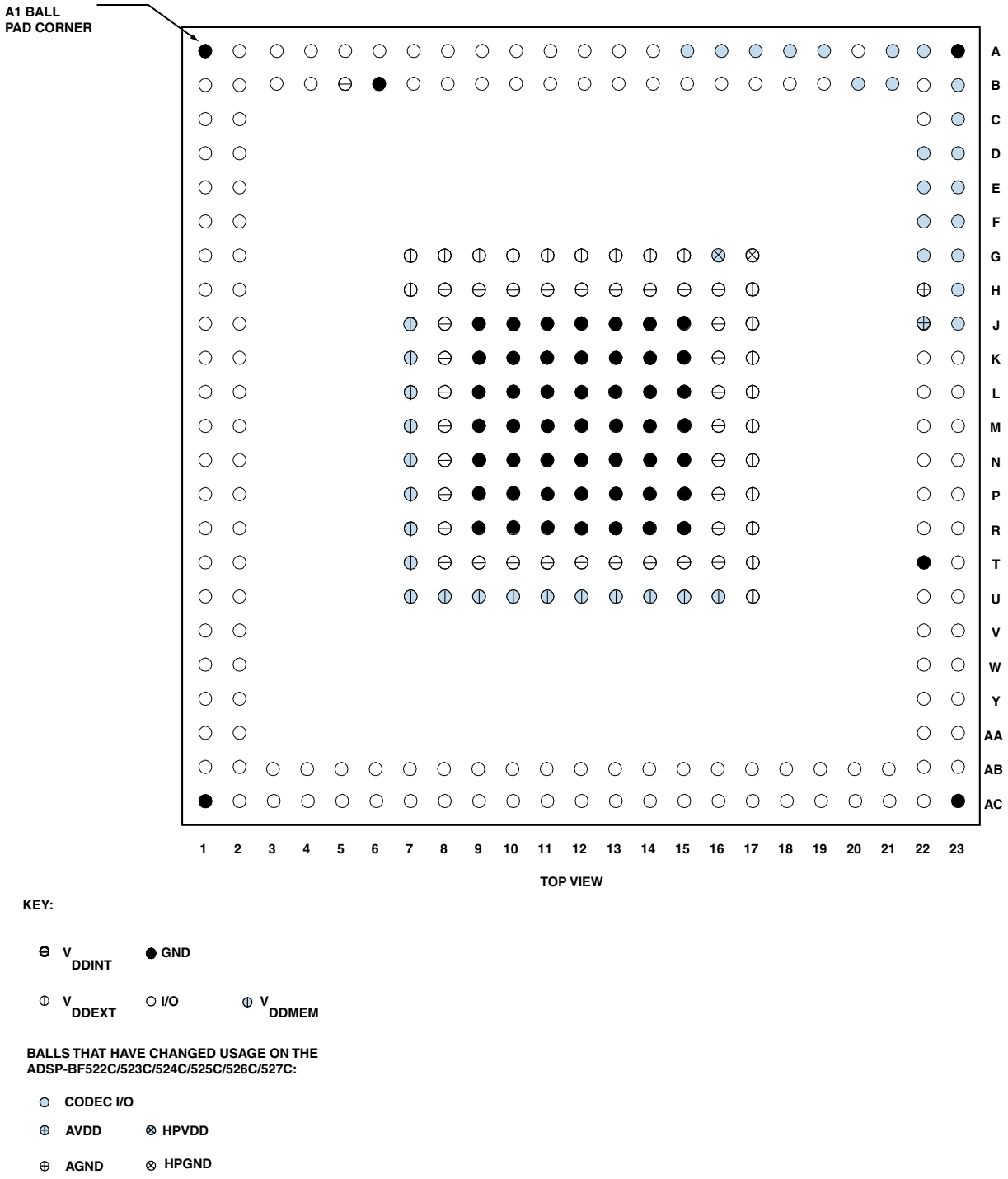


Figure 33. ADSP-BF52xC Processor Ball Configuration (Top View)

ORDERING GUIDE

Model[1]	Temperature Range[2]	Instruction Rate (Max)	Package Description	Package Option
ADSP-BF522KBCZ-3C2	0°C to +70°C	300 MHz	289-Ball Chip Scale Package Ball Grid Array (CSP_BGA)	BC-289-2
ADSP-BF522KBCZ-4C2	0°C to +70°C	400 MHz	289-Ball Chip Scale Package Ball Grid Array (CSP_BGA)	BC-289-2
ADSP-BF523KBCZ-5C2	0°C to +70°C	533 MHz	289-Ball Chip Scale Package Ball Grid Array (CSP_BGA)	BC-289-2
ADSP-BF523KBCZ-6C2	0°C to +70°C	600 MHz	289-Ball Chip Scale Package Ball Grid Array (CSP_BGA)	BC-289-2
ADSP-BF524KBCZ-3C2	0°C to +70°C	300 MHz	289-Ball Chip Scale Package Ball Grid Array (CSP_BGA)	BC-289-2
ADSP-BF524KBCZ-4C2	0°C to +70°C	400 MHz	289-Ball Chip Scale Package Ball Grid Array (CSP_BGA)	BC-289-2
ADSP-BF525KBCZ-5C2	0°C to +70°C	533 MHz	289-Ball Chip Scale Package Ball Grid Array (CSP_BGA)	BC-289-2
ADSP-BF525KBCZ-6C2	0°C to +70°C	600 MHz	289-Ball Chip Scale Package Ball Grid Array (CSP_BGA)	BC-289-2
ADSP-BF526KBCZ-3C2	0°C to +70°C	300 MHz	289-Ball Chip Scale Package Ball Grid Array (CSP_BGA)	BC-289-2
ADSP-BF526KBCZ-4C2	0°C to +70°C	400 MHz	289-Ball Chip Scale Package Ball Grid Array (CSP_BGA)	BC-289-2
ADSP-BF527KBCZ-5C2	0°C to +70°C	533 MHz	289-Ball Chip Scale Package Ball Grid Array (CSP_BGA)	BC-289-2
ADSP-BF527KBCZ-6C2	0°C to +70°C	600 MHz	289-Ball Chip Scale Package Ball Grid Array (CSP_BGA)	BC-289-2

[1] Z = RoHS Compliant Part.

[2] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 21 for junction temperature (T_J) specification which is the only temperature specification.

D06876-0-3/10(A)