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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	TriCore™
Core Size	32-Bit Single-Core
Speed	66MHz
Connectivity	CANbus, SPI, UART/USART
Peripherals	DMA, POR, WDT
Number of I/O	81
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	1.42V ~ 1.58V
Data Converters	A/D 36x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	PG-LQFP-176-2
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/ft1161128f66hlaaxp

1 Summary of Features

The TC1161/TC1162 has the following features:

- High-performance 32-bit super-scaler TriCore v1.3 CPU with 4-stage pipeline
  - Superior real-time performance
  - Strong bit handling
  - Fully integrated DSP capabilities
  - Single precision Floating Point Unit (FPU)
  - 66 MHz operation at full temperature range
- Multiple on-chip memories
  - 32 Kbyte Local Data Memory (SRAM)
  - 4 Kbyte Overlay Memory
  - 8 Kbyte Scratch-Pad RAM (SPRAM)
  - 8 Kbyte Instruction Cache (ICACHE)
  - 1024 Kbyte Program Flash (for instruction code and constant data)
  - 16 Kbyte Data Flash (e.g. 2 Kbyte EEPROM emulation)
  - 16 Kbyte Boot ROM
- 8-channel DMA Controller
- Fast-response interrupt system with 255 hardware priority arbitration levels serviced by CPU
- High-performance on-chip bus structure
  - 64-bit Local Memory Bus (LMB) to Flash memory
  - System Peripheral Bus (SPB) for interconnections of functional units
- Versatile on-chip Peripheral Units
  - Two Asynchronous/Synchronous Serial Channels (ASCs) with baudrate generator, parity, framing and overrun error detection
  - One High Speed Synchronous Serial Channel (SSC) with programmable data length and shift direction
  - One Micro Second Bus (MSC) interface for serial port expansion to external power devices
  - One high-speed Micro Link Interface (MLI) for serial inter-processor communication
  - One MultiCAN Module with two CAN nodes and 64 free assignable message objects for high efficiency data handling via FIFO buffering and gateway data transfer[1)]
  - One General Purpose Timer Array Module (GPTA) with a powerful set of digital signal filtering and timer functionality to realize autonomous and complex Input/Output management
  - One 16-channel Analog-to-Digital Converter unit (ADC) with selectable 8-bit, 10-bit, or 12-bit, supporting 32 input channels

1) Not applicable to TC1161

Ordering Information

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- The derivative itself, i.e. its function set, the temperature range, and the supply voltage
- The package and the type of delivery

For the available ordering codes for the TC1161/TC1162, please refer to the “Product Catalog Microcontrollers” that summarizes all available microcontroller variants.

This document describes the derivatives of the device. **Table 1-1** enumerates these derivatives and summarizes the differences.

Table 1-1 TC1161/TC1162 Derivative Synopsis

Derivative	Ambient Temperature Range
SAF-TC1161-128F66HL	T_A = -40°C to +85°C
SAF-TC1162-128F66HL	T_A = -40°C to +85°C

2.3 Pin Configuration

Figure 2-3 shows the TC1161/TC1162 pin configuration.

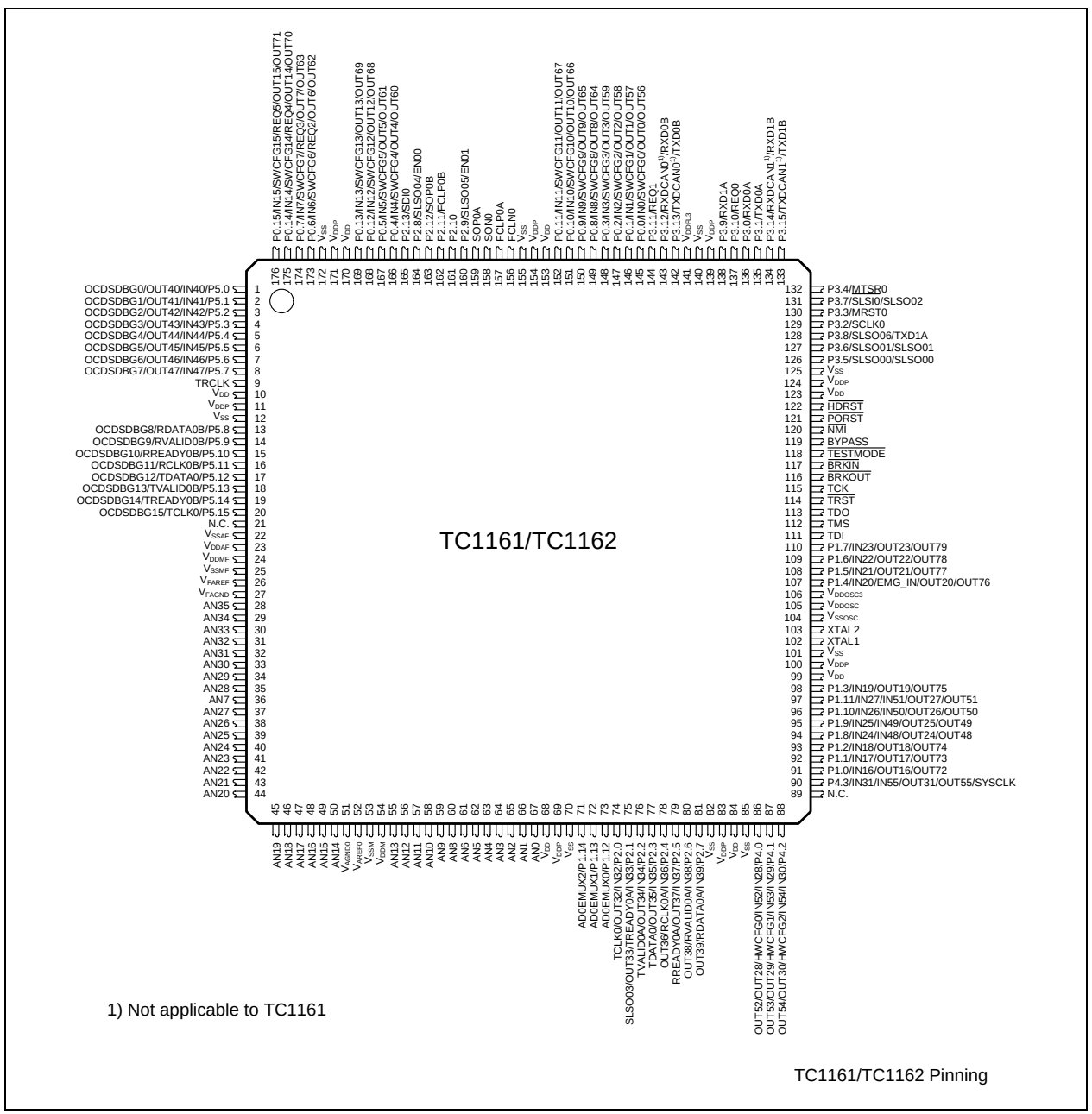

Figure 2-3 TC1161/TC1162 Pinning for PG-LQFP-176-2 Package

Table 2-2 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Driver Class	Power Supply	Functions	
P3		I/O		V_{DDP}	**Port 3** Port 3 is a 16-bit bi-directional general-purpose I/O port which can be alternatively used for ASC0/1, SSC0 and CAN[1] lines.	
P3.0	136		A2		RXD0A	ASC0 receiver inp./outp. A
P3.1	135		A2		TXD0A	ASC0 transmitter output A
					This pin is sampled at the rising edge of $\overline{\text{PORST}}$. If this pin and the BYPASS input pin are both active, then oscillator bypass mode is entered.	
P3.2	129		A2		SCLK0	SSC0 clock input/output
P3.3	130		A2		MRST0	SSC0 master receive input/ slave transmit output
P3.4	132		A2		MTSR0	SSC0 master transmit output/slave receive input
P3.5	126		A2		SLSO00	SSC0 slave select output 0
P3.6	127		A2		$\overline{\text{SLSO01}}$	SSC0 slave select output 1
P3.7	131		A2		$\overline{\text{SLSI0}}$	SSC0 slave select input
					SLSO02	SSC0 slave select output 2
P3.8	128		A2		SLSO06	SSC0 slave select output 6
					TXD1A	ASC1 transmitter output A
P3.9	138		A2		RXD1A	ASC1 receiver inp./outp. A
P3.10	137		A1		REQ0	External trigger input 0
P3.11	144		A1		REQ1	External trigger input 1
P3.12	143		A2		RXDCAN0[1]	CAN node 0 receiver input
					RXD0B	ASC0 receiver inp./outp. B
P3.13	142		A2		TXDCAN0[1]	CAN node 0 transm. output
					TXD0B	ASC0 transmitter output B
P3.14	134		A2		RXDCAN1[1]	CAN node 1 receiver input
					RXD1B	ASC1 receiver inp./outp. B
P3.15	133		A2		TXDCAN1[1]	CAN node 1 transm. output
					TXD1B	ASC1 transmitter output B

Table 2-2 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Driver Class	Power Supply	Functions
P4		I/O		V_{DDP}	**Port 4 / Hardware Configuration Inputs**
P4.[3:0]					HWCFG[3:0] Boot mode and boot location inputs; inputs are latched with the rising edge of HDRST. During normal operation, Port 4 pins may be used as alternate functions for GPTA or system clock output.
P4.0	86		A1		IN28 / OUT28 / IN52 / OUT52 line of GPTA
P4.1	87		A1		IN29 / OUT29 / IN53 / OUT53 line of GPTA
P4.2	88		A2		IN30 / OUT30 / IN54 / OUT54 line of GPTA
P4.3	90		A2		IN31 / OUT31 / IN55 / OUT55 line of GPTA SYSCLK System Clock Output

Table 2-2 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Driver Class	Power Supply	Functions
MSC0 Outputs					
			C	V_{DDP}	**LVDS MSC Clock and Data Outputs**[3]
FCLP0A	157	O			MSC0 Differential Driver Clock Output Positive A
FCLN0	156	O			MSC0 Differential Driver Clock Output Negative
SOP0A	159	O			MSC0 Differential Driver Serial Data Output Positive A
SON0	158	O			MSC0 Differential Driver Serial Data Output Negative

Table 2-2 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Driver Class	Power Supply	Functions
Power Supplies					
V_{DDM}	54	–	–	–	**ADC Analog Part Power Supply (3.3 V)**
V_{SSM}	53	–	–	–	**ADC Analog Part Ground for V_{DDM}**
V_{DDMF}	24	–	–	–	**FADC Analog Part Power Supply (3.3 V)**
V_{SSMF}	25	–	–	–	**FADC Analog Part Ground for V_{DDMF}**
V_{DDAF}	23	–	–	–	**FADC Analog Part Logic Power Supply (1.5 V)**
V_{SSAF}	22	–	–	–	**FADC Analog Part Logic Ground for V_{DDAF}**
V_{AREF0}	52	–	–	–	**ADC Reference Voltage**
V_{AGND0}	51	–	–	–	**ADC Reference Ground**
V_{FAREF}	26	–	–	–	**FADC Reference Voltage**
V_{FAGND}	27	–	–	–	**FADC Reference Ground**
V_{DDOSC}	105	–	–	–	**Main Oscillator and PLL Power Supply (1.5 V)**
V_{DDOSC3}	106	–	–	–	**Main Oscillator Power Supply (3.3 V)**
V_{SSOSC}	104	–	–	–	**Main Oscillator and PLL Ground**
V_{DDFL3}	141	–	–	–	**Power Supply for Flash (3.3 V)**
V_{DD}	10, 68, 84, 99, 123, 153, 170	–	–	–	**Core Power Supply (1.5 V)**

Table 2-2 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Driver Class	Power Supply	Functions
V_{DDP}	11, 69, 83, 100, 124, 154, 171, 139	–	–	–	**Port Power Supply (3.3 V)**
V_{SS}	12, 70, 85, 101, 125, 155, 172, 140, 82	–	–	–	**Ground**

1) Not applicable to TC1161
2) These pads are I/O pads with input only function. Its input characteristics are identical with the input characteristics as defined for class A pads.
3) In case of a power-fail condition (one or more power supply voltages drop below the specified voltage range), an undefined output driving level may occur at these pins.
4) Programmed by software as either break input or break output.
5) These pads are input only pads with input characteristics.
6) Input only pads with input spike filter.
7) Open drain pad with input spike filter.
8) The dual input reset system of TC1161/TC1162 assumes that the $\overline{\text{PORST}}$ reset pin is used for power on reset only.
9) Input only pads without input spike filter.

3.3 Memory Maps

This chapter gives an overview of the TC1161/TC1162 memory map and describes the address locations and access possibilities for the units, memories, and reserved areas as “seen” from different on-chip buses’ (SPB and LMB) point of view.

3.3.1 Architectural Address Map

Table 3-1 shows the overall architectural address map as defined for the TriCore and as implemented in TC1161/TC1162.

Table 3-1 TC1161/TC1162 Architectural Address Map

Segment	Contents	Size	Description
0-7	Global	8 x 256 Mbyte	Reserved (MMU space); cached
8	Global Memory	256 Mbyte	Reserved (246 Mbyte); PMU, Boot ROM; cached
9	Global Memory	256 Mbyte	FPI space; cached
10	Global Memory	256 Mbyte	Reserved (246 Mbyte), PMU, Boot ROM; non-cached
11	Global Memory	256 Mbyte	FPI space; non-cached
12	Local LMB Memory	256 Mbyte	Reserved; bottom 4 Mbyte visible from FPI bus in segment 14; cached
13	DMI	64 Mbyte	Local Data Memory RAM; non-cached
	PMI	64 Mbyte	Local Code Memory RAM; non-cached
	EXT_PER	96 Mbyte	Reserved; non-cached
	EXT_EMU	16 Mbyte	Reserved; non-cached
	BOOTROM	16 Mbyte	Boot ROM space, Boot ROM mirror; non-cached

Table 3-1 TC1161/TC1162 Architectural Address Map (cont'd)

Segment	Contents	Size	Description
14	EXTPER	128 Mbyte	Reserved; non-speculative; non-cached; no execution
	CPU[0 ..15] image region	16 x 8 Mbyte	Non-speculative; non-cached; no execution
15	LMB_PER CSFRs INT_PER	256 Mbyte	CSFRs of CPUs[0 ..15]; LMB & FPI Peripheral Space; non-speculative; non-cached; no execution

Table 3-3 SPB Address Map of Segment 0 to 14 (cont'd)

Segment	Address Range	Size	Description	Access Type	
				Read	Write
10	A000 0000$_H$ - A00F FFFF$_H$	1 Mbyte	Program Flash (PFLASH)	access	access[1]
	A010 0000$_H$ - A017 FFFF$_H$	≈ 0.5 Mbyte	Reserved	access[2]	access[1)2)]
	A017 8000$_H$ - A07F FFFF$_H$	6.5 Mbyte	Reserved	LMBBE & SPBBE	LMBBE
	A080 0000$_H$ - AFDF FFFF$_H$	246 Mbyte	Reserved	LMBBE & SPBBE	LMBBE
	AFE0 0000$_H$ - AFE0 1FFF$_H$	8 Kbyte	Data Flash (DFLASH) Bank 0	access	access[1]
	AFE0 2000$_H$ - AFE0 3FFF$_H$	8 Kbyte	Reserved	access[2]	access[1)2)]
	AFE0 4000$_H$ - AFE0 FFFF$_H$	48 Kbyte	Reserved	LMBBE & SPBBE	LMBBE
	AFE1 0000$_H$ - AFE1 1FFF$_H$	8 Kbyte	Data Flash (DFLASH) Bank 1	access	access[1]
	AFE1 2000$_H$ - AFE1 3FFF$_H$	8 Kbyte	Reserved	access[2]	access[1)2)]
	AFE1 4000$_H$ - AFF1 FFFF$_H$	1 Mbyte	Reserved	LMBBE & SPBBE	ignore
	AFF2 0000$_H$ - AFF5 FFFF$_H$	256 Kbyte	Reserved		
	AFF6 0000$_H$ - AFFF BFFF$_H$	624 Kbyte	Reserved		
	AFFF C000$_H$ - AFFF FFFF$_H$	16 Kbyte	Boot ROM (BROM)	access	
11	B000 0000$_H$ - BFFF FFFF$_H$	256 Mbyte	Reserved	SPBBE	SPBBE
12	C000 0000$_H$ - C000 0FFF$_H$	4 Kbyte	Overlay memory (OVRAM)	SPBBE	SPBBE
	C000 1000$_H$ - CFFF FFFF$_H$	≈ 256 Mbyte	Reserved	SPBBE	SPBBE

3.11 Micro Link Serial Bus Interface (MLI0)

The Micro Link Interface is a fast synchronous serial interface that allows data exchange between microcontrollers of the 32-bit AUDO microcontroller family without intervention of a CPU or other bus masters. **Figure 3-7** shows how two microcontrollers are typically connected together via their MLI interface. The MLI operates in both microcontrollers as a bus master on the system bus.

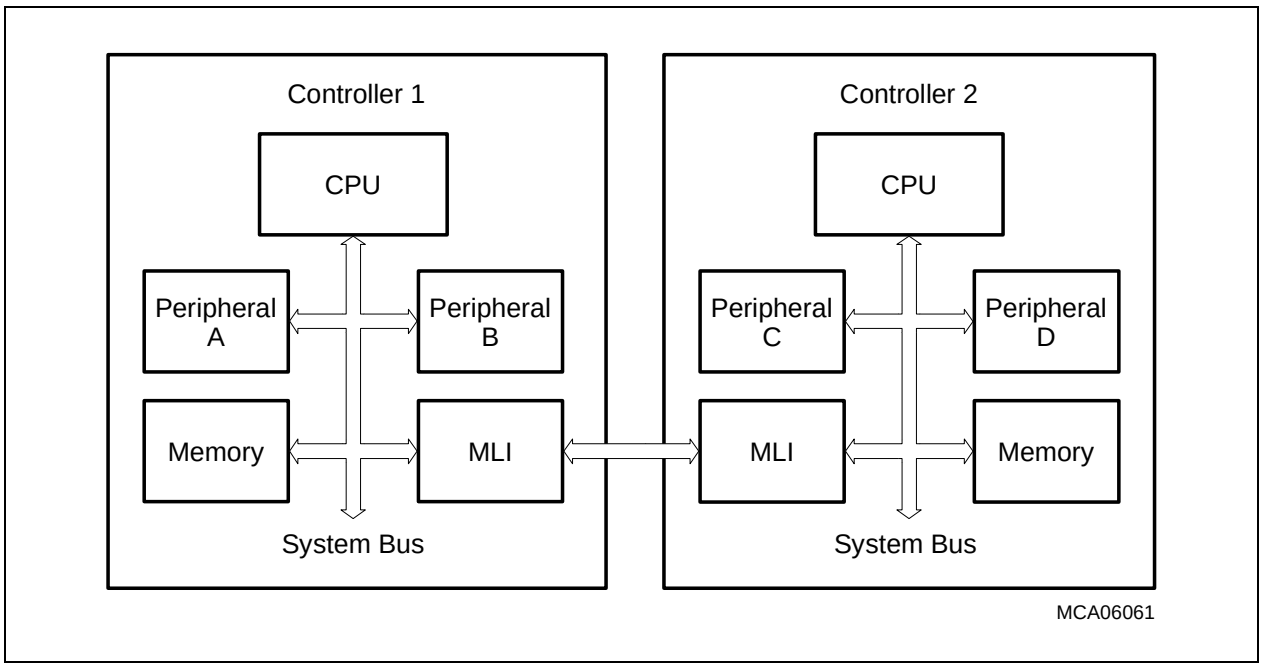

Figure 3-7 Typical Micro Link Interface Connection

Features

- Synchronous serial communication between MLI transmitters and MLI receivers located on the same or on different microcontroller devices
- Automatic data transfer/request transactions between local/remote controller
- Fully transparent read/write access supported (= remote programming)
- Complete address range of remote controller available
- Specific frame protocol to transfer commands, addresses and data
- Error control by parity bit
- 32-bit, 16-bit, and 8-bit data transfers
- Programmable baud rates
  - MLI transmitter baud rate: max. $f_{MLI}/2$ (= 33 Mbit/s @ 66 MHz module clock)
  - MLI receiver baud rate: max. f_{MLI}
- Multiple remote (slave) controllers are supported

MLI transmitter and MLI receiver communicate with other off-chip MLI receivers and MLI transmitters via a 4-line serial I/O bus each. Several I/O lines of these I/O buses are available outside the MLI module kernel as four-line output or input buses.

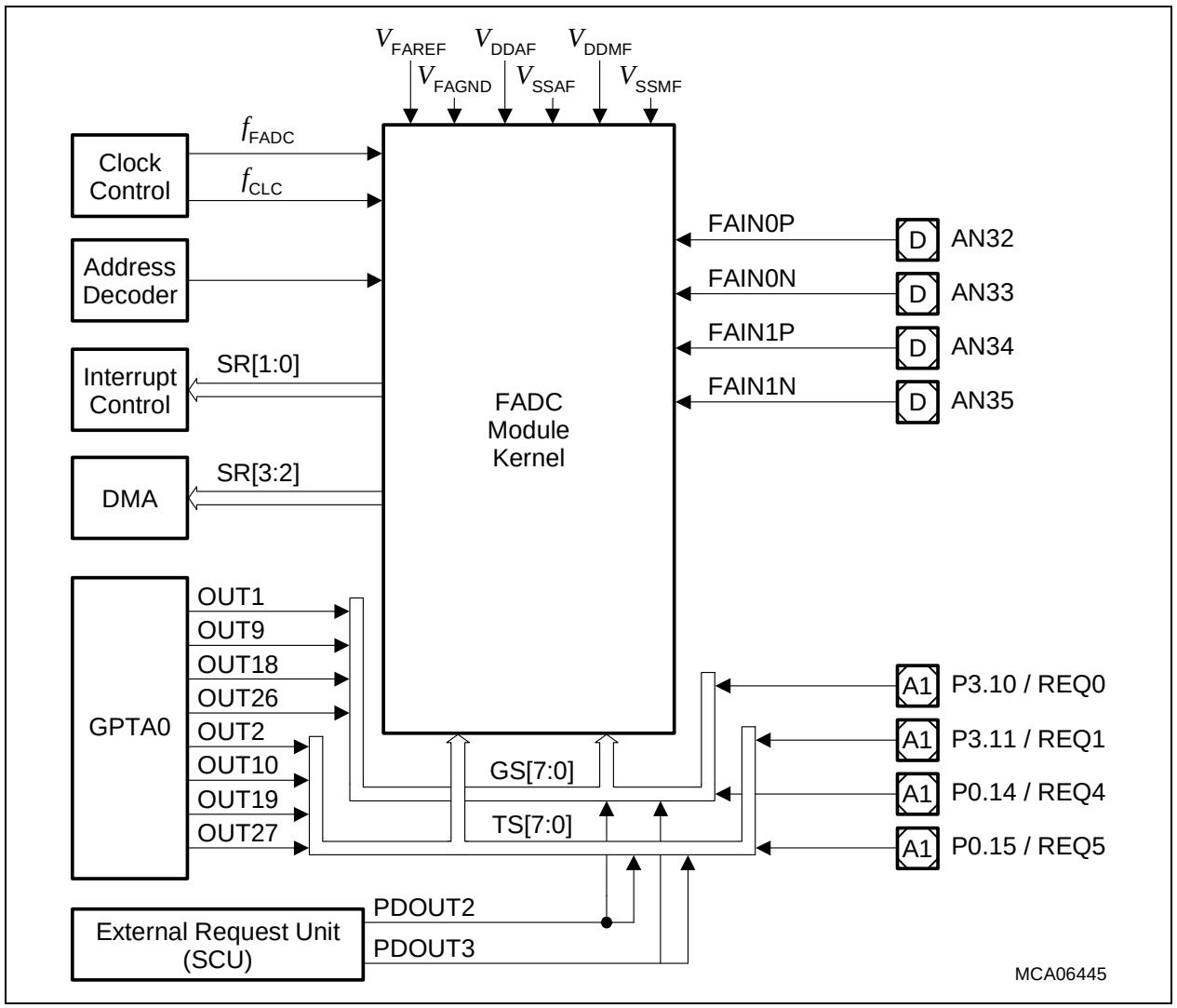

Figure 3-11 Block Diagram of the FADC Module

Features

- Extreme fast conversion, 21 cycles of f_{FADC} clock (318.2 ns @ f_{FADC} = 66 MHz)
- 10-bit A/D conversion
  - Higher resolution by averaging of consecutive conversions is supported
- Successive approximation conversion method
- Two differential input channels
- Offset and gain calibration support for each channel
- Differential input amplifier with programmable gain of 1, 2, 4 and 8 for each channel
- Free-running (Channel Timers) or triggered conversion modes
- Trigger and gating control for external signals
- Built-in Channel Timers for internal triggering
- Channel timer request periods independently selectable for each channel
- Selectable, programmable anti-aliasing and data reduction filter block

OCDS Level 1 Debug Support

The OCDS Level 1 debug support is mainly assigned for real-time software debugging purposes which have a demand for low-cost standard debugger hardware.

The OCDS Level 1 is based on a JTAG interface that is used by the external debug hardware to communicate with the system. The on-chip Cerberus module controls the interactions between the JTAG interface and the on-chip modules. The external debug hardware may become master of the internal buses, and read or write the on-chip register/memory resources. The Cerberus also makes it possible to define breakpoint and trigger conditions as well as to control user program execution (run/stop, break, single-step).

OCDS Level 2 Debug Support

The OCDS Level 2 debug support makes it possible to implement program tracing capabilities for enhanced debuggers by extending the OCDS Level 1 debug functionality with an additional 16-bit wide trace output port with trace clock. With the trace extension, the following four trace capabilities are provided (only one of the three trace capabilities can be selected at a time):

- Trace of the CPU program flow
- Trace of the DMA Controller transaction requests
- Trace of the DMA Controller Move Engine status information

15) I_{AREF_MAX} is valid for the minimum specified conversion time. The current flowing during an ADC conversion with a duration of up to t_C = 25µs can be calculated with the formula $I_{AREF\_MAX} = Q_{CONV}/t_C$. Every conversion needs a total charge of Q_{CONV} = 150pC from V_{AREF}.
All ADC conversions with a duration longer than t_C = 25µs consume an I_{AREF_MAX} = 6µA.

16) For the definition of the parameters see also **Figure 4-2**.

17) Applies to AIN0 and AIN1, when used as auxiliary reference inputs.

18) This represents an equivalent switched capacitance. This capacitance is not switched to the reference voltage at once. Instead of this smaller capacitances are successively switched to the reference voltage.

19) The sampling capacity of the conversion C-Network is pre-charged to V_{AREF}/2 before the sampling moment. Because of the parasitic elements the voltage measured at AINx is lower then V_{AREF}/2.

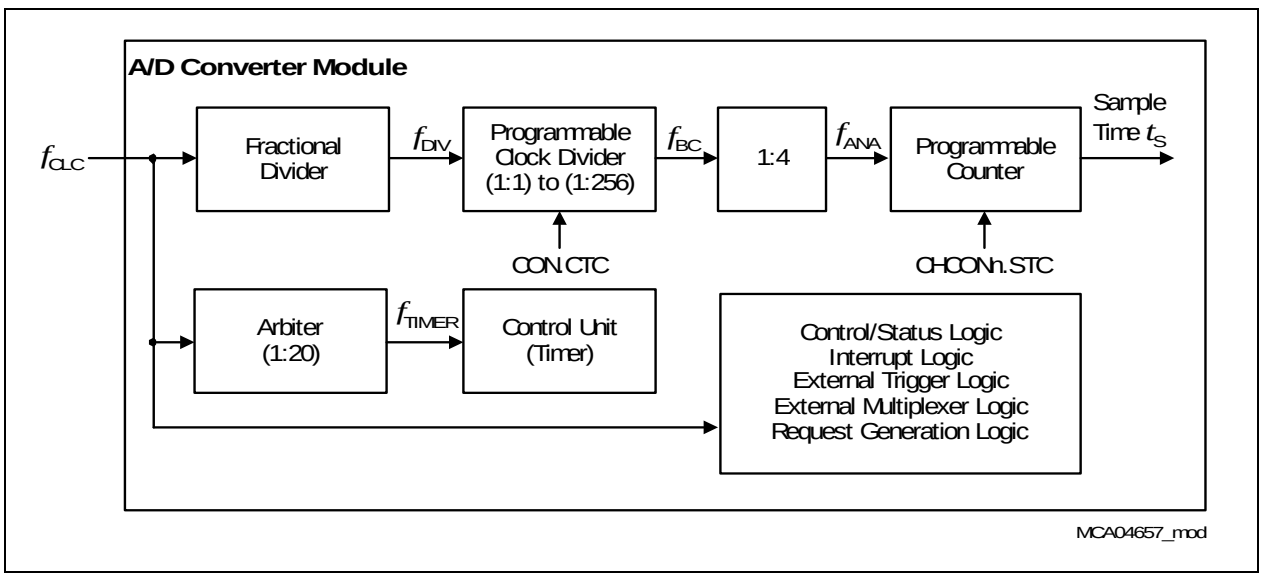

Figure 4-1 ADC0 Clock Circuit

Table 4-7 FADC Characteristics (cont'd)(Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Remarks Conditions
			Min.	Max.		
Analog supply currents	I_{DDMF}	SR	–	9	mA	–
	I_{DDAF}	SR	–	17	mA	10)
Input current at each V_{FAREF}	I_{FAREF}	CC	–	150	µA rms	Independent of conversion
Input leakage current at V_{FAREF} 11)	I_{FOZ2}	CC	–	±500	nA	0 V < V_{IN} < V_{DDMF}
Input leakage current at V_{FAGND}	I_{FOZ3}	CC		±8	µA	
Conversion time	t_C	CC	–	21	CLK of f_{ADC}	For 10-bit conv.
Converter Clock	f_{ADC}	CC	–	66	MHz	–
Input resistance of the analog voltage path (Rn, Rp)	R_{FAIN}	CC	100	200	kΩ	12)
Channel Amplifier Cutoff Frequency	f_{COFF}	CC	2		MHz	–
Settling Time of a Channel Amplifier after changing ENN or ENP	t_{SET}	CC		5	µsec	–

1) Calibration of the gain is possible for the gain of 1 and 2, and not possible for the gain of 4 and 8.

2) Callibration should be performed at each power-up. In case of continuous operation, callibration should be performed minimum once per week.

3) The offset error voltage drifts over the whole temperature range typically ±2 LSB.

4) Applies when the gain of the channel equals one. For the other gain settings, the offset error increases; it must be multiplied with the applied gain.

5) The leakage current definition is a continuous function, as shown in **Figure 4-5**. The numerical values defined determine the characteristic points of the given continuous linear approximation - they do not define step function.

6) Only one of these parameters is tested, the other is verified by design characterization.

7) Voltage overshoot to 4 V are permissible, provided the pulse duration is less than 100 µs and the cumulated summary of the pulses does not exceed 1 h.

8) Voltage overshoot to 1.7 V are permissible, provided the pulse duration is less than 100 µs and the cumulated sum of the pulses does not exceed 1 h.

9) A running conversion may become inexact in case of violating the normal operating conditions (voltage overshoots).

10) Current peaks of up to 40 mA with a duration of max. 2 ns may occur

4.2.4 Oscillator Pins

Figure 4-8 provides the characteristics of the oscillator pins in the TC1161/TC1162.

Table 4-8 Oscillator Pins Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit values		Unit	Test Conditions
			Min.	Max.		
Frequency Range	f_{OSC}	CC	4	25	MHz	–
Input low voltage at XTAL1[1)]	V_{ILX}	SR	-0.2	0.3 × V_{DDOSC3}	V	–
Input high voltage at XTAL1[1)]	V_{IHX}	SR	0.7 × V_{DDOSC3}	V_{DDOSC3} + 0.2	V	–
Input current at XTAL1	I_{IX1}	CC	–	±25	µA	0 V < V_{IN} < V_{DDOSC3}

1) If the XTAL1 pin is driven by a crystal, reaching a minimum amplitude (peak-to-peak) of 0.3 × V_{DDOSC3} is necessary.

Note: It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimal parameters for the oscillator operation. Please refer to the limits specified by the crystal supplier.

Note: The frequency of system clock f_{SYS} can be selected to be either f_{CPU} or $f_{CPU}/2$.

With rising number P of clock cycles the maximum jitter increases linearly up to a value of P that is defined by the K-factor of the PLL. Beyond this value of P the maximum accumulated jitter remains at a constant value. Further, a lower CPU clock frequency f_{CPU} results in a higher absolute maximum jitter value.

Figure 4-12 illustrates the jitter curve for several K/ f_{CPU} combinations.

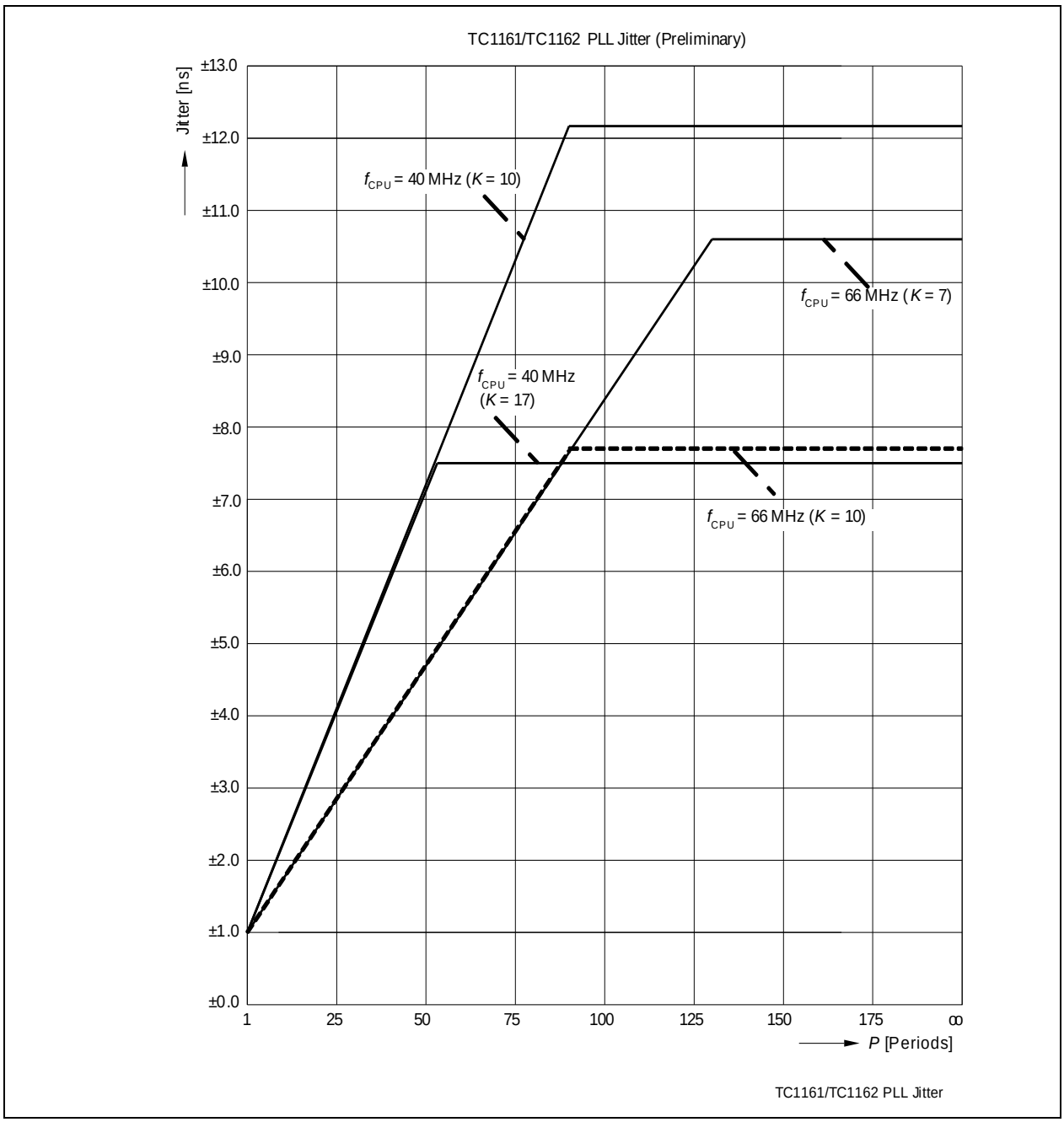

Figure 4-12 Approximated Maximum Accumulated PLL Jitter for Typical CPU Clock Frequencies f_{CPU} (overview)

5.3 Flash Memory Parameters

The data retention time of the TC1161/TC1162's Flash memory (i.e. the time after which stored data can still be retrieved) depends on the number of times the Flash memory has been erased and programmed.

Table 5-2 Flash Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Program Flash Retention Time, Physical Sector[1) 2)]	t_{RET}	15	–	years	Max. 1000 erase/program cycles
Program Flash Retention Time, Logical Sector[1)2)]	t_{RETL}	15	–	years	Max. 50 erase/program cycles
Data Flash Endurance (16 Kbyte)	N_E	15 000	–	–	Max. data retention time 2 years
Data Flash Endurance, EEPROM Emulation (8 × 2 Kbyte)	N_{E8}	120 000	–	–	Max. data retention time 2 years
Programming Time per Page[3)]	t_{PR}	–	5	ms	–
Program Flash Erase Time per 256-Kbyte sector	t_{ERP}	–	5	s	f_{CPU} = 66 MHz
Data Flash Erase Time per 8-Kbyte sector	t_{ERD}	–	312.5	ms	f_{CPU} = 66 MHz
Wake-up time	t_{WU}	$4300 \times 1/f_{CPU}$ + 40µs			

1) Storage and inactive time included.

2) At average weighted junction temperature T_J = 100 °C.

3) In case the Program Verify feature detects weak bits, these bits will be programmed once more. The reprogramming takes additional 5ms.

5.4 Quality Declaration

Table 5-3 shows the characteristics of the quality parameters in the TC1161/TC1162.

Table 5-3 Quality Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
ESD susceptibility according to Human Body Model (HBM)	V_{HBM}	–	2000	V	Conforming to EIA/JESD22-A114-B
ESD susceptibility of the LVDS pins	V_{HBM1}	–	500	V	–
ESD susceptibility according to Charged Device Model (CDM) pins	V_{CDM}	–	500	V	Conforming to JESD22-C101-C
Moisture Sensitivity Level (MSL)	–	–	3	–	Conforming to J-STD-020C for 240°C

*Note: Information about soldering can be found on the “package” information page under: **http://www.infineon.com/products**.*