Infineon Technologies - FT1162128F66HLAAXP Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	TriCore™
Core Size	32-Bit Single-Core
Speed	66MHz
Connectivity	CANbus, SPI, UART/USART
Peripherals	DMA, POR, WDT
Number of I/O	81
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	1.42V ~ 1.58V
Data Converters	A/D 36x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	PG-LQFP-176-2
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/ft1162128f66hlaaxp

TC1161/TC1162

32-Bit Single-Chip Microcontroller

TriCore

Microcontrollers

Never stop thinking

Preliminary

TC1161/TC1162 Data Sheet
Revision History: V1.0, 2008-04

Previous Version: V0.3 2007-03

Page	Subjects (major changes since last revision)
7	VSSOSC3 is deleted from the TC1161/TC1162 Logic Symbol.
8, 10	TDATA0 of Pin 17, TCLK0 of Pin 20, TCLK0 of Pin 74 and TDATA0 of Pin 77 are updated in the Pinning Diagram and Pin Definition and Functions Table.
51	Transmit DMA request in Block Diagram of ASC Interfaces is updated.
53	Alternate output functions in block diagram of SSC interfaces are updated.
59	Programmable baud rate of the MLI is updated.
60	TDATA0 and TCLK0 of the block diagram of MLI interfaces are updated.
71	The description for WDT double reset detection is updated.
108	The power sequencing details is updated.
119	MLI timing, maximum operating frequency limit is extended, t31 is added.
123	Thermal resistance junction leads is updated.

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mcdocu.comments@infineon.com

  - One 2-channel Fast Analog-to-Digital Converter unit (FADC) with concatenated comb filters for hardware data reduction: supporting 10-bit resolution, with minimum conversion time of 318.2 ns
- 32 analog input lines for ADC and FADC
- 81 digital general purpose I/O lines
- Digital I/O ports with 3.3 V capability
- On-chip debug support for OCDS Level 1 and 2 (CPU, DMA)
- Power Management System
- Clock Generation Unit with PLL
- Core supply voltage of 1.5 V
- I/O voltage of 3.3 V
- Full Industrial and Multi-Market temperature range: -40° to +85°C
- PG-LQFP-176-2 package

2.4 Pad Driver and Input Classes Overview

The TC1161/TC1162 provides different types and classes of input and output lines. For understanding of the abbreviations in **Table 2-2** starting at the next page, **Table 2-1** gives an overview on the pad type and class types.

Table 2-1 Pad Driver and Input Classes Overview

Class	Power Supply	Type	Sub Class	Speed Grade	Termination
A	3.3V	LVTTL I/O, LVTTL outputs	**A1** (e.g. GPIO)	6 MHz	No
			A2 (e.g. serial I/Os)	40 MHz	Series termination recommended
			A3 (e.g. BRKIN, BRKOUT)	66 MHz/	Yes, series termination
			A4 (e.g.Trace Clock)	66 MHz	Yes, series termination
C	3.3V	LVDS	–	50 MHz	Parallel termination
D		Analog input	–	–	–

Table 2-2 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Driver Class	Power Supply	Functions
Power Supplies					
V_{DDM}	54	–	–	–	**ADC Analog Part Power Supply (3.3 V)**
V_{SSM}	53	–	–	–	**ADC Analog Part Ground for V_{DDM}**
V_{DDMF}	24	–	–	–	**FADC Analog Part Power Supply (3.3 V)**
V_{SSMF}	25	–	–	–	**FADC Analog Part Ground for V_{DDMF}**
V_{DDAF}	23	–	–	–	**FADC Analog Part Logic Power Supply (1.5 V)**
V_{SSAF}	22	–	–	–	**FADC Analog Part Logic Ground for V_{DDAF}**
V_{AREF0}	52	–	–	–	**ADC Reference Voltage**
V_{AGND0}	51	–	–	–	**ADC Reference Ground**
V_{FAREF}	26	–	–	–	**FADC Reference Voltage**
V_{FAGND}	27	–	–	–	**FADC Reference Ground**
V_{DDOSC}	105	–	–	–	**Main Oscillator and PLL Power Supply (1.5 V)**
V_{DDOSC3}	106	–	–	–	**Main Oscillator Power Supply (3.3 V)**
V_{SSOSC}	104	–	–	–	**Main Oscillator and PLL Ground**
V_{DDFL3}	141	–	–	–	**Power Supply for Flash (3.3 V)**
V_{DD}	10, 68, 84, 99, 123, 153, 170	–	–	–	**Core Power Supply (1.5 V)**

Segment 14

From the SPB point of view (DMA and Cerberus), this memory segment allows accesses to the PMU Overlay memory (OVRAM), the DMI Local Data RAM (LDRAM), and the PMI scratch-pad RAM (SPRAM).

From the CPU point of view (PMI and DMI), this memory segment is reserved in the TC1161/TC1162.

Segment 15

From the SPB point of view (DMA and Cerberus), this memory segment allows accesses to all SFRs and CSFRs, and the MLI transfer windows.

From the CPU point of view (PMI and DMI), this memory segment allows accesses to all SFRs and CSFRs, and the MLI transfer windows.

3.3.4 Address Map of the FPI Bus System

Table 3-3 and Table 3-4 shows the address maps of the FPI Bus System.

3.3.4.1 Segments 0 to 14

Table 3-3 shows the address maps of segments 0 to 14 as it is seen from the SPB bus masters, DMA and OCDS.

Table 3-3 SPB Address Map of Segment 0 to 14

Segment	Address Range	Size	Description	Access Type	
				Read	Write
0-7	$0000\ 0000_H$ - $0000\ 0007_H$	8 byte	Reserved (virtual address space)	MPN trap	MPN trap
	$0000\ 0008_H$ - $7FFF\ FFFF_H$	8 × 256 Mbyte		SPBBE	SPBBE

Table 3-3 SPB Address Map of Segment 0 to 14 (cont'd)

Segment	Address Range	Size	Description	Access Type	
				Read	Write
10	A000 0000$_H$ - A00F FFFF$_H$	1 Mbyte	Program Flash (PFLASH)	access	access[1]
	A010 0000$_H$ - A017 FFFF$_H$	≈ 0.5 Mbyte	Reserved	access[2]	access[1)2)]
	A017 8000$_H$ - A07F FFFF$_H$	6.5 Mbyte	Reserved	LMBBE & SPBBE	LMBBE
	A080 0000$_H$ - AFDF FFFF$_H$	246 Mbyte	Reserved	LMBBE & SPBBE	LMBBE
	AFE0 0000$_H$ - AFE0 1FFF$_H$	8 Kbyte	Data Flash (DFLASH) Bank 0	access	access[1]
	AFE0 2000$_H$ - AFE0 3FFF$_H$	8 Kbyte	Reserved	access[2]	access[1)2)]
	AFE0 4000$_H$ - AFE0 FFFF$_H$	48 Kbyte	Reserved	LMBBE & SPBBE	LMBBE
	AFE1 0000$_H$ - AFE1 1FFF$_H$	8 Kbyte	Data Flash (DFLASH) Bank 1	access	access[1]
	AFE1 2000$_H$ - AFE1 3FFF$_H$	8 Kbyte	Reserved	access[2]	access[1)2)]
	AFE1 4000$_H$ - AFF1 FFFF$_H$	1 Mbyte	Reserved	LMBBE & SPBBE	ignore
	AFF2 0000$_H$ - AFF5 FFFF$_H$	256 Kbyte	Reserved		
	AFF6 0000$_H$ - AFFF BFFF$_H$	624 Kbyte	Reserved		
	AFFF C000$_H$ - AFFF FFFF$_H$	16 Kbyte	Boot ROM (BROM)	access	
11	B000 0000$_H$ - BFFF FFFF$_H$	256 Mbyte	Reserved	SPBBE	SPBBE
12	C000 0000$_H$ - C000 0FFF$_H$	4 Kbyte	Overlay memory (OVRAM)	SPBBE	SPBBE
	C000 1000$_H$ - CFFF FFFF$_H$	≈ 256 Mbyte	Reserved	SPBBE	SPBBE

3.3.5 Address Map of the Local Memory Bus (LMB)

Table 3-5 shows the address map as seen from the LMB bus masters (PMI and DMI).

Table 3-5 LMB Address Map

Segment	Address Range	Size	Description	Action	
				Read	Write
0-7[1)]	$0000\ 0000_H$ - $0000\ 0007_H$	8 byte	Reserved (virtual address space)	MPN trap	MPN trap
	$0000\ 0008_H$ - $7FFF\ FFFF_H$	8 × 256 Mbyte		SPBBET	SPBBE
8[1)]	$8000\ 0000_H$ - $800F\ FFFF_H$	1 Mbyte	Program Flash (PFLASH)	access	access[2)]
	$8010\ 0000_H$ - $8017\ 7FFF_H$	≈ 0.5 Mbyte	Reserved	access[3)]	access[2)3)]
	$8017\ 8000_H$ - $807F\ FFFF_H$	6.5 Mbyte	Reserved	LMBBET	LMBBET
	$8080\ 0000_H$ - $8FDF\ FFFF_H$	246 Mbyte	Reserved	LMBBET	LMBBET
	$8FE0\ 0000_H$ - $8FE0\ 1FFF_H$	8 Kbyte	Data Flash (DFLASH) Bank 0	access	access[2)]
	$8FE0\ 2000_H$ - $8FE0\ 3FFF_H$	8 Kbyte	Reserved	access[3)]	access[2)3)]
	$8FE0\ 4000_H$ - $8FE0\ FFFF_H$	48 Kbyte	Reserved	LMBBET	LMBBET
	$8FE1\ 0000_H$ - $8FE1\ 1FFF_H$	8 Kbyte	Data Flash (DFLASH) Bank 1	access	access[2)]
	$8FE1\ 2000_H$ - $8FE1\ 3FFF_H$	8 Kbyte	Reserved	access[3)]	access[2)3)]
	$8FE1\ 4000_H$ - $8FF1\ FFFF_H$	1 Mbyte	Reserved	LMBBET	LMBBET
	$8FF2\ 0000_H$ - $8FF5\ FFFF_H$	256 Kbyte	Reserved		
	$8FF6\ 0000_H$ - $8FFF\ BFFF_H$	624 Kbyte	Reserved		
	$8FFF\ C000_H$ - $8FFF\ FFFF_H$	16 Kbyte	Boot ROM (BROM)	access	

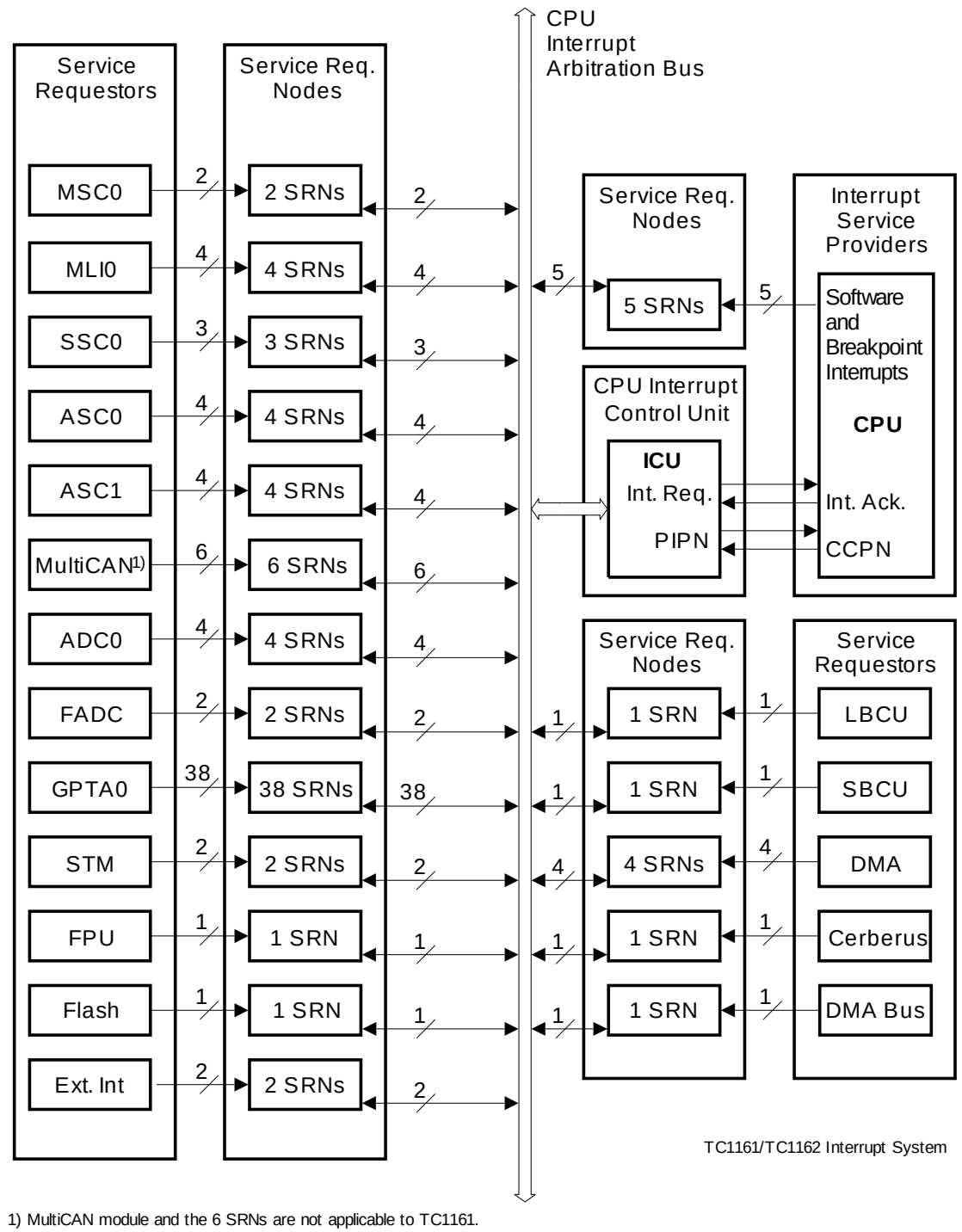


Figure 3-2 Block Diagram of the TC1161/TC1162 Interrupt System

3.12 General Purpose Timer Array

The GPTA provides a set of timer, compare, and capture functionalities that can be flexibly combined to form signal measurement and signal generation units. They are optimized for tasks typical of electrical motor control applications, but can also be used to generate simple and complex signal waveforms needed in other industrial applications.

The TC1161/TC1162 contains one General Purpose Timer Array (GPTA0). **Figure 3-9** shows a global view of the GPTA module.

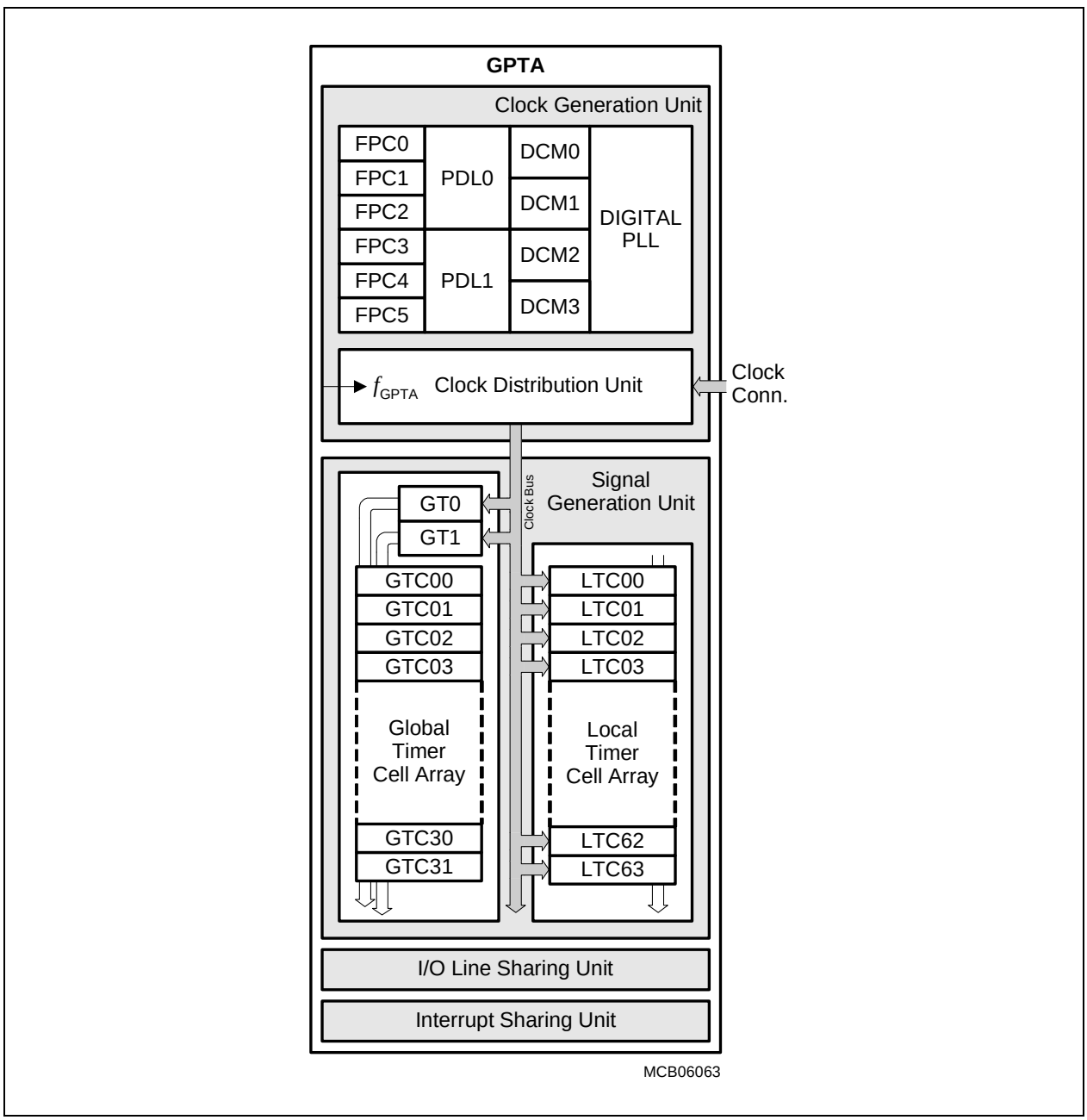


Figure 3-9 Block Diagram of the GPTA Module

- Duty Cycle Measurement (DCM)
  - Four independent units
  - 0 - 100% margin and time-out handling
  - f_{GPTA} maximum resolution
  - $f_{GPTA}/2$ maximum input signal frequency
- Digital Phase Locked Loop (PLL)
  - One unit
  - Arbitrary multiplication factor between 1 and 65535
  - f_{GPTA} maximum resolution
  - $f_{GPTA}/2$ maximum input signal frequency
- Clock Distribution Unit (CDU)
  - One unit
  - Provides nine clock output signals:
    f_{GPTA}, divided f_{GPTA} clocks, FPC1/FPC4 outputs, DCM clock, LTC prescaler clock

Signal Generation Unit

- Global Timers (GT)
  - Two independent units
  - Two operating modes (Free-Running Timer and Reload Timer)
  - 24-bit data width
  - f_{GPTA} maximum resolution
  - $f_{GPTA}/2$ maximum input signal frequency
- Global Timer Cell (GTC)
  - 32 units related to the Global Timers
  - Two operating modes (Capture, Compare and Capture after Compare)
  - 24-bit data width
  - f_{GPTA} maximum resolution
  - $f_{GPTA}/2$ maximum input signal frequency
- Local Timer Cell (LTC)
  - 64 independent units
  - Three basic operating modes (Timer, Capture and Compare) for 63 units
  - Special compare modes for one unit
  - 16-bit data width
  - f_{GPTA} maximum resolution
  - $f_{GPTA}/2$ maximum input signal frequency

Interrupt Control Unit

- 111 interrupt sources, generating up to 38 service requests

3.14 Fast Analog-to-Digital Converter Unit (FADC)

The on-chip FADC module of the TC1161/TC1162 basically is a 2-channel A/D converter with 10-bit resolution that operates by the method of the successive approximation.

As shown in **Figure 3-11**, the main FADC functional blocks are:

- The Input Stage — contains the differential inputs and the programmable amplifier
- The A/D Converter — is responsible for the analog-to-digital conversion
- The Data Reduction Unit — contains programmable antialiasing and data reduction filters
- The Channel Trigger Control block — determines the trigger and gating conditions for the two FADC channels
- The Channel Timers — can independently trigger the conversion of each FADC channel
- The A/D Control block is responsible for the overall FADC functionality

The FADC module is supplied by the following power supply and reference voltage lines:

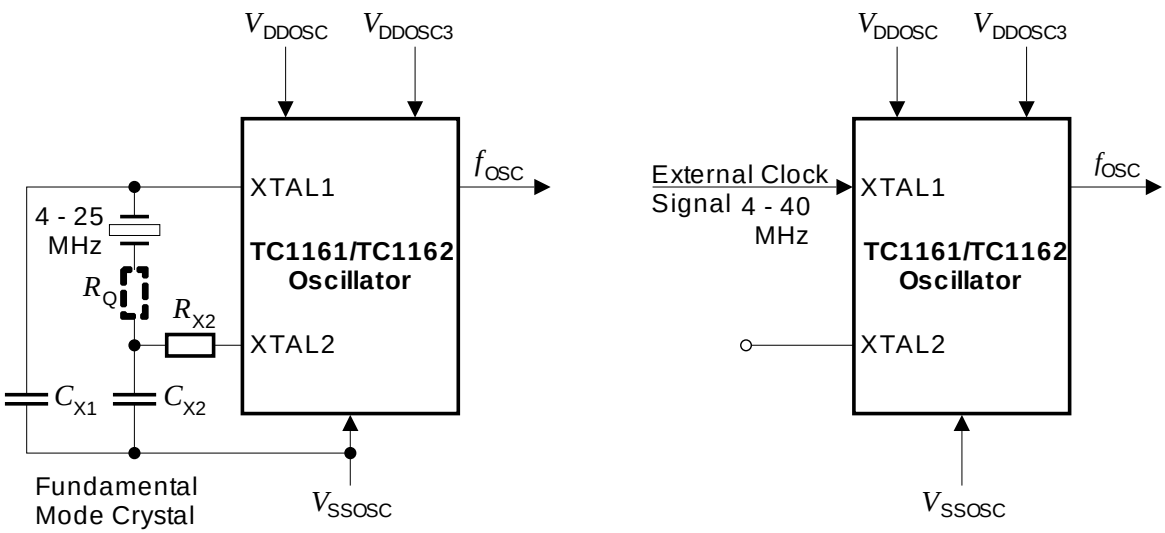
- V_{DDMF}/V_{DDMF}:FADC Analog Part Power Supply (3.3 V)
- V_{DDAF}/V_{DDAF}:FADC Analog Part Logic Power Supply (1.5 V)
- V_{FAREF}/V_{FAGND}:FADC Reference Voltage (3.3 V)/FADC Reference Ground

Oscillation measurement with the final target system is strongly recommended to verify the input amplitude at XTAL1 and to determine the actual oscillation allowance (margin negative resistance) for the oscillator-crystal system.

When using an external clock signal, the signal must be connected to XTAL1. XTAL2 is left open (unconnected). The external clock frequency can be in the range of 0 - 40 MHz if the PLL is bypassed, and 4 - 40 MHz if the PLL is used.

The oscillator can also be used in combination with a ceramic resonator. The final circuitry must also be verified by the resonator vendor.

Figure 3-15 shows the recommended external oscillator circuitries for both operating modes, external crystal mode and external input clock mode. A block capacitor is recommended to be placed between V_{DDOSC}/V_{DDOSC3} and V_{SSOSC}.



Crystal Frequency	C_{X1}, C_{X2} 1)	R_{X2} 1)
4 MHz	33 pF	0
8 MHz	18 pF	0
12 MHz	12 pF	0
16 - 25 MHz	10 pF	0

1) Note that these are evaluation start values!

TC1161/TC1162 Oscillator Circuitry

Figure 3-15 Oscillator Circuitries

Note: For crystal operation, it is strongly recommended to measure the negative resistance in the final target system (layout) to determine the optimum parameters for the oscillator operation. Please refer to the minimum and maximum values of the negative resistance specified by the crystal supplier.

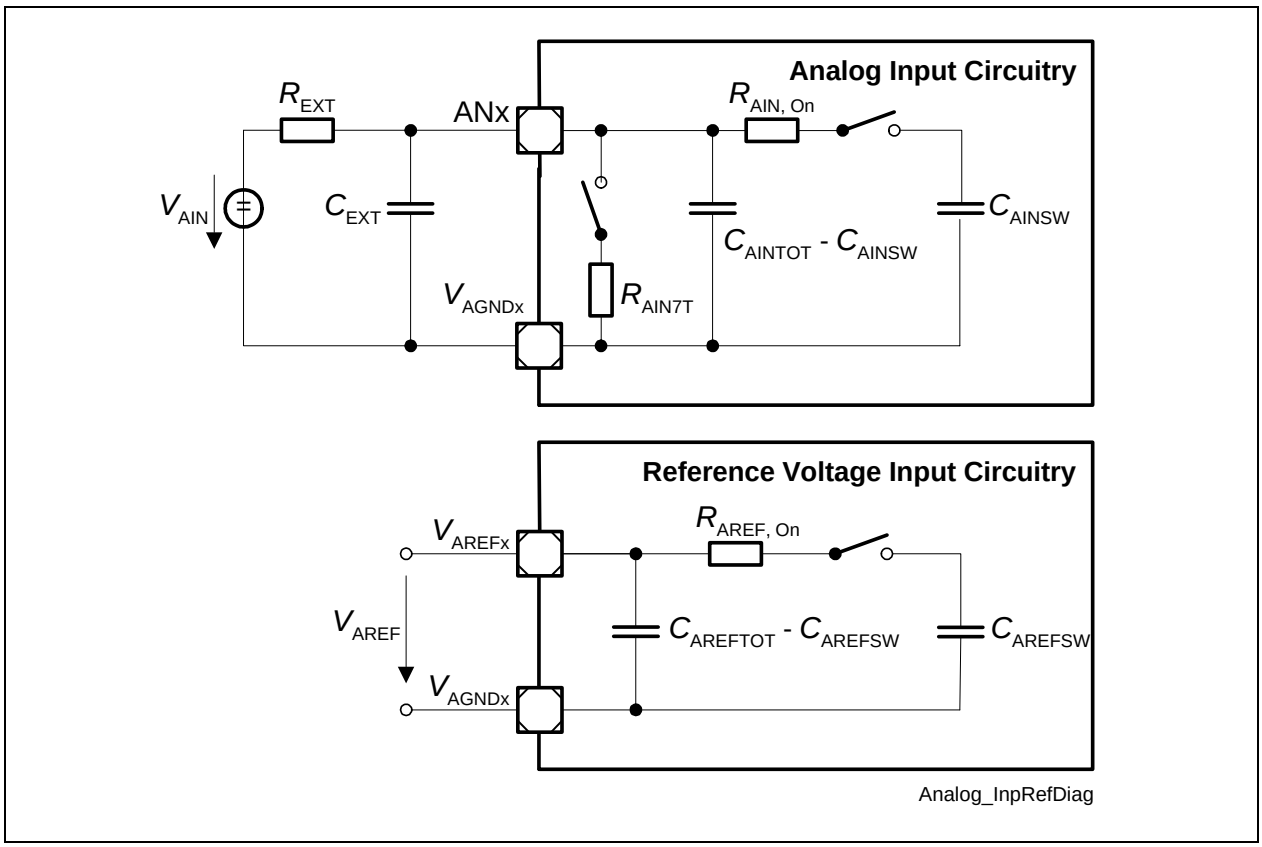


Figure 4-2 ADC0 Input Circuits

4.3.4 Power, Pad and Reset Timing

Figure 4-12 provides the characteristics of the power, pad and reset timing in the TC1161/TC1162.

Table 4-12 Power, Pad and Reset Timing Parameters

Parameter	Symbol		Limit Values		Unit
			Min.	Max.	
Min. V_{DDP} voltage to ensure defined pad states[1]	V_{DDPPA}	CC	0.6	–	V
Oscillator start-up time[2]	t_{OSCS}	CC	–	10	ms
Minimum $\overline{\text{PORST}}$ active time after power supplies are stable at operating levels	t_{POA}	SR	10	–	ms
$\overline{\text{HDRST}}$ pulse width	t_{HD}	CC	1024 clock cycles[3]	–	f_{SYS}
$\overline{\text{PORST}}$ rise time	t_{POR}	SR	–	50	ms
Setup time to $\overline{\text{PORST}}$ rising edge[4]	t_{POS}	SR	0	–	ns
Hold time from $\overline{\text{PORST}}$ rising edge[4]	t_{POH}	SR	100	–	ns
Setup time to $\overline{\text{HDRST}}$ rising edge[5]	t_{HDS}	SR	0	–	ns
Hold time from $\overline{\text{HDRST}}$ rising edge[5]	t_{HDH}	SR	100 + $(2 \times 1/f_{SYS})$	–	ns
Ports inactive after $\overline{\text{PORST}}$ reset active[6][7]	t_{PIP}	CC	–	150	ns
Ports inactive after $\overline{\text{HDRST}}$ reset active[8]	t_{PI}	CC	–	150 + $5 \times 1/f_{SYS}$	ns
Minimum V_{DDP} $\overline{\text{PORST}}$ activation threshold.[9]	$V_{PORST3.3}$	SR	–	2.9	V
Minimum V_{DD} $\overline{\text{PORST}}$ activation threshold. [9]	$V_{PORST1.5}$	SR	–	1.32	V
Power-on Reset Boot Time[10]	t_{BP}	CC	2.15	3.50	ms
Hardware/Software Reset Boot Time at f_{CPU}=66MHz[11]	t_B	CC	560	860	µs

1) This parameter is valid under assumption that $\overline{\text{PORST}}$ signal is constantly at low-level during the power-up/power-down of the V_{DDP}.

2) This parameter is verified by device characterization. The external oscillator circuitry must be optimized by the customer and checked for negative resistance as recommended and specified by crystal suppliers.

3) Any $\overline{\text{HDRST}}$ activation is internally prolonged to 1024 FPI bus clock (f_{SYS}) cycles.

4.3.6 Debug Trace Timing

V_{SS} = 0 V; V_{DDP} = 3.13 to 3.47 V (Class A); T_A = -40 °C to +85 °C;
C_L (TRCLK) = 25 pF; C_L (TR[15:0]) = 50 pF

Table 4-14 Debug Trace Timing Parameter[1)]

Parameter	Symbol		Limit Values		Unit
			Min.	Max.	
TR[15:0] new state from TRCLK	t_9	CC	-1	4	ns

1) Not subject to production test, verified by design/characterization.

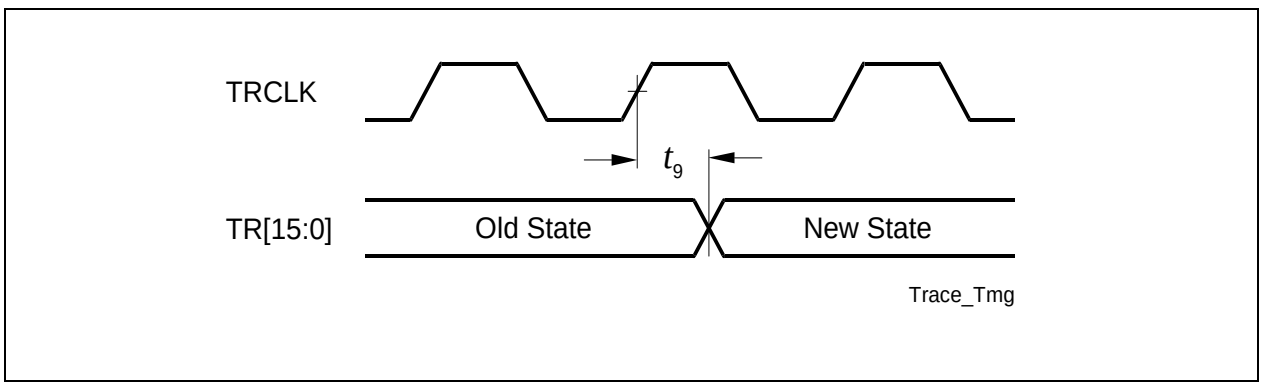


Figure 4-14 Debug Trace Timing

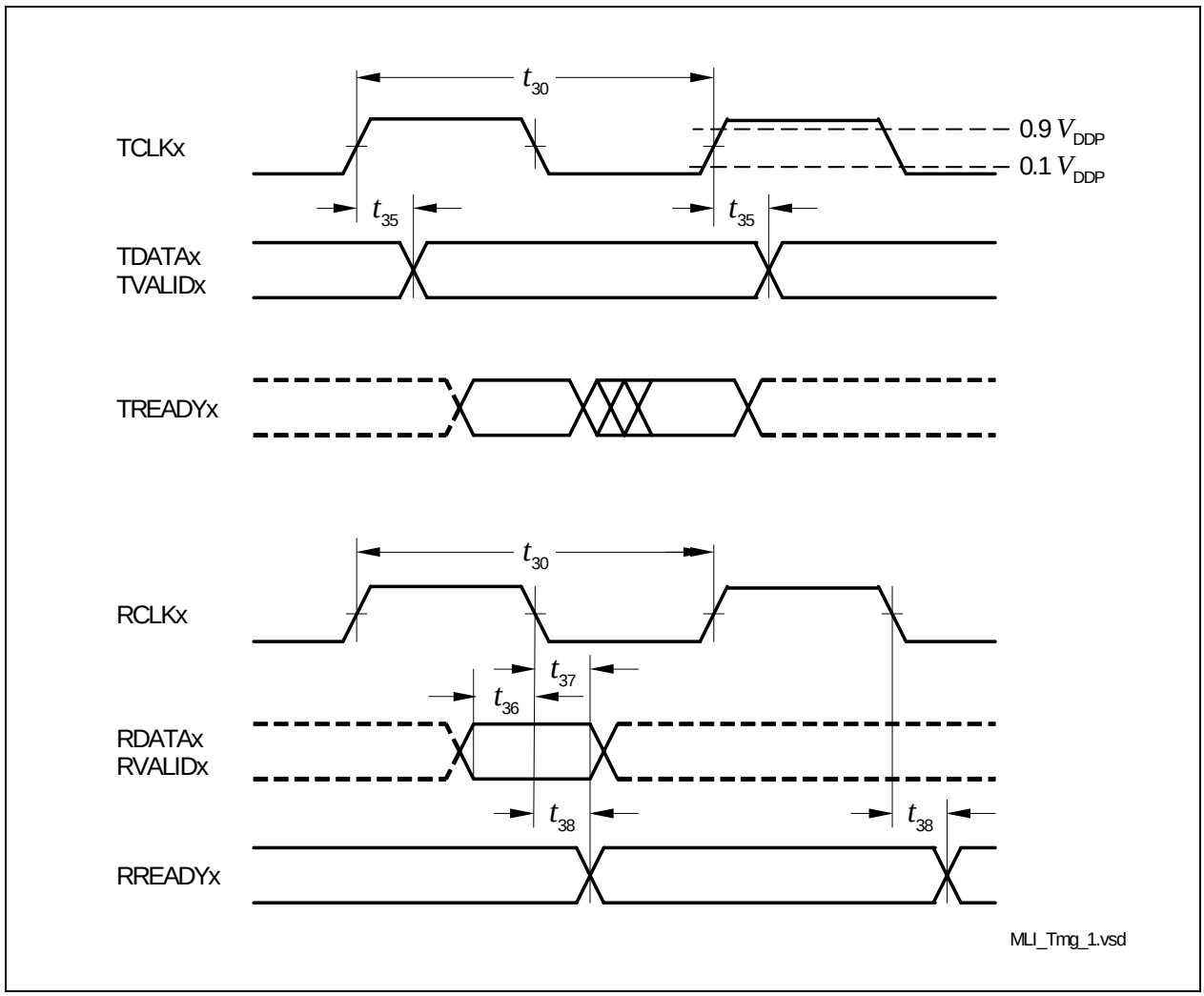


Figure 4-17 MLI Interface Timing

Note: The generation of RREADYx is in the input clock domain of the receiver. The reception of TREADYx is asynchronous to TCLKx.

5 Packaging and Reliability

Chapter 5 provides the information of the TC1161/TC1162 package and reliability section.

5.1 Package Parameters

Table 5-1 provides the thermal characteristics of the package.

Table 5-1 Package Parameters (PG-LQFP-176-2)

Parameter	Symbol		Limit Values		Unit	Notes
			Min.	Max.		
Thermal resistance junction case top[1)]	R_{TJCT}	CC	–	5.4	K/W	–
Thermal resistance junction leads	R_{TJL}	CC	–	21.5	K/W	–

1) The thermal resistances between the case top and the ambient (R_{TCAT}), the leads and the ambient (R_{TLA}) are to be combined with the thermal resistances between the junction and the case top (R_{TJCT}), the junction and the leads (R_{TJL}) given above, in order to calculate the total thermal resistance between the junction and the ambient (R_{TJA}). The thermal resistances between the case top and the ambient (R_{TCAT}), the leads and the ambient (R_{TLA}) depend on the external system (PCB, case) characteristics, and are under user responsibility. The junction temperature can be calculated using the following equation: $T_J=T_A+R_{TJA} \times P_D$, where the R_{TJA} is the total thermal resistance between the junction and the ambient. This total junction ambient resistance R_{TJA} can be obtained from the upper four partial thermal resistances.

5.2 Package Outline

Figure 5-1 shows the package outlines of the TC1161/TC1162.

PG-LQFP-176-2
Plastic Low Profile Quad Flat Package

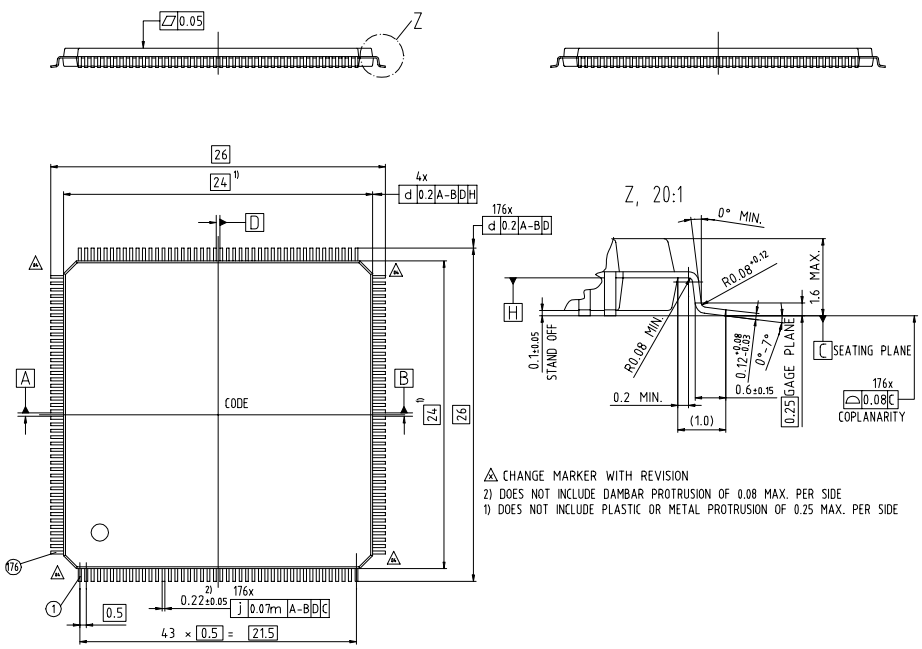


Figure 5-1 Package Outlines PG-LQFP-176-2

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: http://www.infineon.com/products.

SMD = Surface Mounted Device

Dimensions in mm