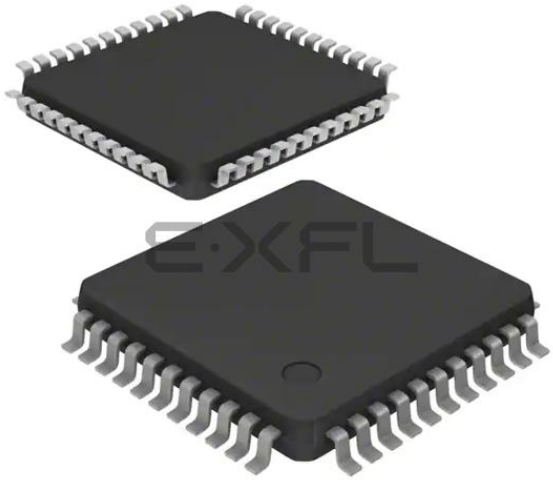

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	12MHz
Connectivity	EBI/EMI
Peripherals	POR, WDT
Number of I/O	32
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	4.75V ~ 5.25V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86c9012asg

Layout

Traces connecting crystal, caps, and the Z8® CPU oscillator pins should be as short and wide as possible. This reduces parasitic inductance and resistance. The components (caps, crystal, resistors) should be placed as close as possible to the oscillator pins of the Z8 CPU.

The traces from the oscillator pins of the IC and the ground side of the lead caps should be guarded from all other traces (clock, V_{CC}, address/data lines, system ground) to reduce cross talk and noise injection. This is usually accomplished by keeping other traces and system ground trace planes away from the oscillator circuit and by placing a Z8 CPU device V_{SS} ground ring around the traces/components. The ground side of the oscillator lead caps should be connected to a single trace to the Z8 CPU's V_{SS} (GND) pin. It should not be shared with any other system ground trace or components except at the Z8 CPU's V_{SS} pin. This is to prevent differential system ground noise injection into the oscillator (see Figure 17 on page 29).

Indications of an Unreliable Design

Start-up time and output level are two major indicators that are used in working designs to determine their reliability over full lot and temperature variations. These two indicators are described below.

Start-Up Time—If start-up time is excessive, or varies widely from unit to unit, there is probably a gain problem. C1/C2 must be reduced; the amplifier gain is not adequate at frequency, or crystal resistance is too large.

Output Level—The signal at the amplifier output should swing from ground to V_{CC}. This indicates there is adequate gain in the amplifier. As the oscillator starts up, the signal amplitude grows until clipping occurs, at which point the loop gain is effectively reduced to unity and constant oscillation is achieved. A signal of less than 2.5 V peak-to-peak is an indication that low gain may be a problem. Either C_1 or C_2 should be made smaller or a low-resistance crystal should be used.

Circuit Board Design Rules

The following circuit board design rules are suggested:

- To prevent induced noise the crystal and load capacitors should be physically located as close to the Z8 CPU as possible.
- Signal lines should not run parallel to the clock oscillator inputs. In particular, the crystal input circuitry and the internal system clock output should be separated as much as possible.
- V_{CC} power lines should be separated from the clock oscillator input circuitry.
- Resistivity between XTAL1 or XTAL2 and the other pins should be greater than 10 MT.

Table 12. Sample Control and Peripheral Register Reset Values (ERF Bank 0)

Register (Hex)	Register Name	Bits 7	6	5	4	3	2	1	0	Comments
F0	Serial I/O	U	U	U	U	U	U	U	U	
F1	Timer Mode	0	0	0	0	0	0	0	0	Counter/Timers stopped.
F2	Counter/Timer1	U	U	U	U	U	U	U	U	
F3	T1 Prescaler	U	U	U	U	U	U	0	0	Single-pass count mode, external clock source.
F4	Counter/Timer0	U	U	U	U	U	U	U	U	
F5	T0 Prescaler	U	U	U	U	U	U	U	0	Single-pass count mode.
F6	Port 2 Mode	1	1	1	1	1	1	1	1	All inputs.
F7	Port 3 Mode	0	0	0	0	0	0	0	0	Port 2 open-drain, P33–P30 Input, P37–P34 Output.
F8	Port 0–1 Mode	0	1	0	0	1	1	0	1	Internal Stack, Normal Memory Timing.
F9	Interrupt Priority	U	U	U	U	U	U	U	U	
FA	Interrupt Request	0	0	0	0	0	0	0	0	All Interrupts Cleared.
FB	Interrupt Mask	0	U	U	U	U	U	U	U	Interrupts Disabled.
FC	Flags	U	U	U	U	U	U	U	U	
FD	Register Pointer	0	0	0	0	0	0	0	0	
FE	Stack Pointer (High)	U	U	U	U	U	U	U	U	
FF	Stack Pointer (Low)	U	U	U	U	U	U	U	U	

Program execution starts 5 to 10 clock cycles after internal $\overline{\text{RESET}}$ has returned High. The initial instruction fetch is from location 000Ch. Figure 22 on page 35 displays reset timing.

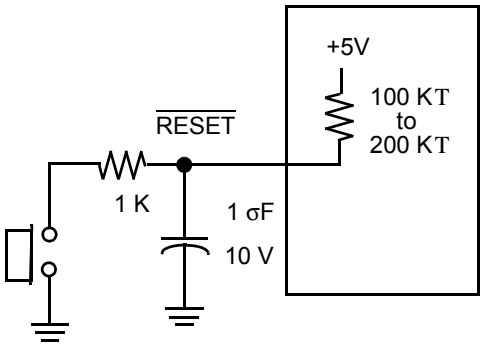


Figure 23. Example of External Power-On Reset Circuit

Table 13. ERF Bank 0 Reset Values at RESET

Register (Hex)	Register Name	Bits 7	6	5	4	3	2	1	0	Comments
00	Port 0	U	U	U	U	U	U	U	U	Input mode, output set to push–pull.
01	Port 1	U	U	U	U	U	U	U	U	Input mode, output set to push–pull.
02	Port 2	U	U	U	U	U	U	U	U	Input mode, output set to open drain.
03	Port 3	1	1	1	1	U	U	U	U	Standard digital input and output Z86L7X Family Device Port P34-P37 = 0 (Except Z86L70/71/75) All other Z8 = 1.
04–EF	General-Purpose Registers 04h–EFh	U	U	U	U	U	U	U	U	Undefined.

Table 14. Sample Expanded Register File Bank C Reset Values

Register (Hex)	Register Name	Bits 7	6	5	4	3	2	1	0	Comments
00	SPI Compare (SCOMP)	0	0	0	0	0	0	0	0	
01	Receive Buffer (RxBUF)	U	U	U	U	U	U	U	U	
02	SPI Control (SCON)	U	U	U	U	0	0	0	0	

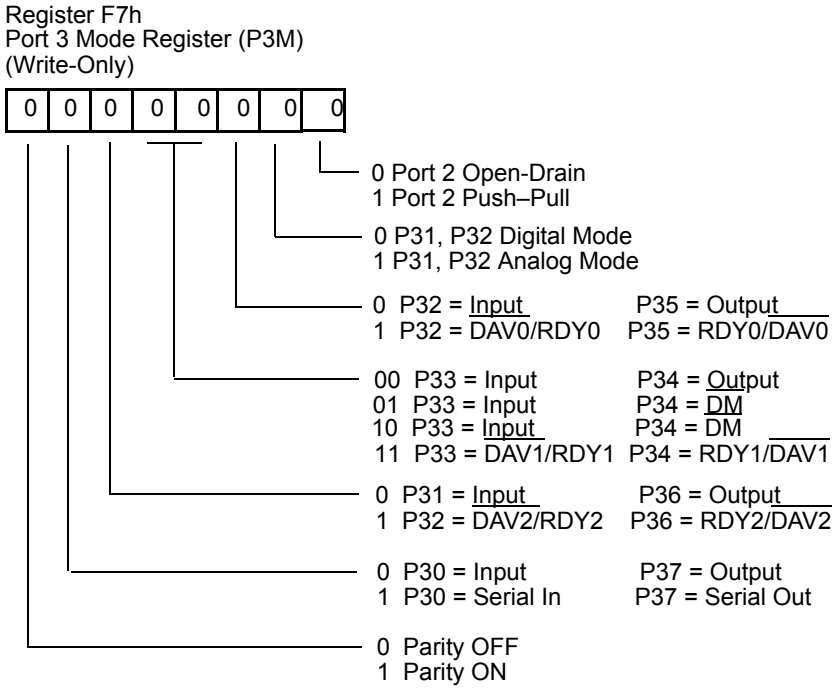


Figure 56. Port 3 Mode Reset

Analog Comparators

Select Z8 devices include two independent on-chip analog comparators. See the device product specification for feature availability and use. Port 3, Pins P31, and P32 each has a comparator front end. The comparator reference voltage, pin P33, is common to both comparators. In analog mode, the P31, and P32 are the positive inputs to the comparators and P33 is the reference voltage supplied to both comparators. In digital mode, pin P33 can be used as a P33 register input or IRQ1 source. P34, P35, or P37 may output the comparator outputs by software-programming the PCON Register bit D0 to 1.

Comparator Description

Two on-board comparators process analog signals on P31 and P32 with reference to the voltage on P33. The analog function is enabled by programming the Port 3 Mode Register (P3M bit 1). For interrupt functions during analog mode, P31 and P32 are programmable as rising, falling, or both edge triggered interrupts (IRQ register bits 6 and 7).

Note: P33 cannot generate an external interrupt while in this mode. P33 can only generate interrupts in DIGITAL mode.

second occurs when the input is connected to the output of a device with tri-state capability.

The autolatch also activates when the input voltage at the pin is not within 200 microvolts or so of either supply rail. In this case, the circuit draws current, which is not significant compared to the I_{CC} operating current of the device, but increases I_{CC2} STOP mode current of the device dramatically.

The fourth condition occurs when the I/O bit is configured as an output. As displayed in Figure 65 on page 77, there are two ways of tri-stating the port pin. The first is by configuring the port as an input, which disables the $\overline{OE}$ signal turning both transistors OFF. The second can be achieved in output mode by writing a 1 to the output port, then activating the open-drain mode. Both transistors are again OFF, and the port bit is in a high impedance state. The autolatches then pull the input section toward V_{DD}.

Autolatch Model

The autolatch's equivalent circuit is displayed in Figure 66. When the input is high, the circuit consists of a resistance Rp from V_{DD} (the P-channel transistor in its ON state) and a much greater resistance Rh to G_{ND}. Current I_{AO} flows from V_{DD} to the output. When the input is low, the circuit may be modeled as a resistance Rp from G_{ND} (the N-channel transistor in the ON state) and a much greater resistance Rh to V_{DD}. Current I_{AO} now flows from the input to ground. The autolatch is characterized with respect to I_{AO}, so the equivalent resistance Rp is calculated according to $R_P = (V_{DD}–V_{IN})/I_{AO}$. The worst case equivalent resistance Rp (min) may be calculated at the worst case input voltage, $V_I = V_{IH}$ (min).

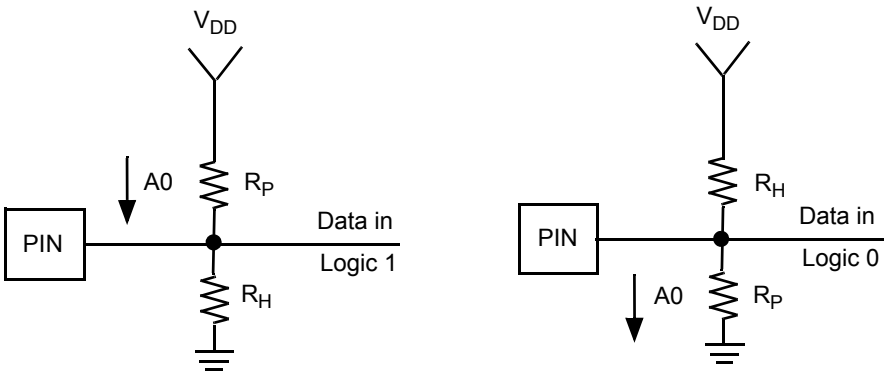


Figure 66. Autolatch Equivalent Circuit

Design Considerations

For circuits in which the autolatch is active, considerations should be given to the loading constraints of the autolatches. For example, with weak values of V_{IN}, close to Vih (min) or

Table 19. Interrupt Priority (Continued)

			Priority	
Group	**Bit**	**Value**	**Highest**	**Lowest**
B	Bit 2	0	IRQ2	IRQ0
		1	IRQ0	IRQ2
A	Bit 5	0	IRQ5	IRQ3
		1	IRQ3	IRQ5

Table 20. Interrupt Group Priority

Bit Pattern			Group Priority		
Bit 4	**Bit 3**	**Bit 0**	**High**	**Medium**	**Low**
0	0	0	Not Used		
0	0	1	C	A	B
0	1	0	A	B	C
0	1	1	A	C	B
1	0	0	B	C	A
1	0	1	C	B	A
1	1	0	B	A	C
1	1	1	Not Used		

Interrupt Mask Register Initialization

The Interrupt Mask Register individually or globally enables or disables the six interrupt requests (see Figure 97 on page 102). When bit 0 to bit 5 are set to 1, the corresponding interrupt requests are enabled. Bit 7 is the master enable and must be set before any of the individual interrupt requests can be recognized. Resetting bit 7 globally disables all of the interrupt requests. Bit 7 is set and reset by the EI and DI instructions. It is automatically reset during an interrupt service routine and set following the execution of an Interrupt Return (IRET) instruction.

Bit 7 must be reset by the DI instruction before the contents of the Interrupt Mask Register or the Interrupt Priority Register are changed except:

- Immediately after a hardware reset
- Immediately after executing an interrupt service routine and before IMR bit 7 has been set by any instruction

NOP instruction (opcode = FFh) immediately before the STOP instruction (opcode = 6Fh), that is,

```
FF NOP ;clear the instruction pipeline
6F STOP ;enter STOP mode
```

STOP mode is exited by any one of the following resets: POR activation, WDT time out (if available), or a Stop Mode Recovery source. Upon reset generation, the processor always restarts the application program at address 000Ch.

POR/RESET activation is present on all Z8 devices and is implemented as a reset pin and/or an on-chip power on reset circuit.

Some Z8 devices allow for the on-chip WDT to run in STOP mode. If so activated, the WDT time-out generates a reset some fixed time period after entering STOP mode.

Stop Mode Recovery by the WDT increases STOP mode standby current (I_{CC2}). This is due to the WDT clock and divider circuitry that is now enabled and running to support this recovery mode. See the product data sheet for actual I_{CC2} values.

All Z8 devices provide some form of dedicated Stop Mode Recovery circuitry. Two SMR methods are implemented—a single fixed input pin or a flexible, programmable set of inputs. The selected Z8 device product specification should be reviewed to determine the SMR options available for use.

For devices that support SPI, the slave mode compare feature also serves as a SMR source.

In the simple case, a low level applied to input pin P27 triggers a SMR. To use this mode, pin P27 (I/O Port 2, bit 7) must be configured as an input before STOP mode is entered. The low level on P27 must meet a minimum pulse width T_{WSM}. (See the product data sheet) to trigger the device reset mode). Some Z8 devices provide multiple SMR input sources. The appropriate SMR source is selected via the SMR Register.

Use of specialized SMR modes (P2.7 input or SMR register based) or the WDT time-out (only when in STOP mode) provide a unique reset operation. Some control registers are initialized differently for a SMR/WDT triggered POR than a standard reset operation. See the product specification (register file map) for exact details.

To determine the actual STOP mode current (I_{CC2}) value for the optional SMR modes available, see the selected Z8 device's product data sheet.

STOP mode current (I_{CC2}) is minimized when:

- V_{CC} is at the low end of the devices operating range
- WDT is off in STOP mode
- Output current sourcing is minimized
- All inputs (digital and analog) are at the low or high rail voltages

external clock frequency when this bit is set (D1 = 1). Using this bit together with D7 of PCON helps further lower EMI (D7 (PCON) = 0, D1 (SMR) = 1). The default setting is zero.

Stop Mode Recovery Source—The D2, D3, and D4 bits of the SMR specify the wake-up source of the stop-recovery and (Table 22 and Figure 104 on page 114).

Table 22. Stop Mode Recovery Source

SMR: 432			
D4	**D3**	**D2**	**Description of Operation**
0	0	0	POR and/or external reset recovery.
0	0	1	P30 transition.
0	1	0	P31 transition (not in Analog Mode).
0	1	1	P32 transition (not in Analog Mode).
1	0	0	P33 transition (not in Analog Mode).
1	0	1	P27 transition.
1	1	0	Logical NOR of P20 through P23.
1	1	1	Logical NOR of P20 through P27.

Stop Mode Recovery Delay Select—This D5 bit, if High, enables the T_{POR} $\overline{\text{RESET}}$ delay after Stop Mode Recovery. The default configuration of this bit is 1. If the fast wake up is selected, the Stop Mode Recovery source is kept active for at least 5 TpC.

Stop Mode Recovery Edge Select—A 1 in this D6 bit position indicates that a high level on any one of the recovery sources wakes the Z8® CPU from STOP mode. A 0 indicates low-level recovery. The default is 0 on POR (see Figure 104 on page 114).

Cold or Warm Start—This D7 bit is set by the device upon entering STOP mode. A 0 in this bit (cold) indicates that the device reset by POR/WDT RESET. A 1 in this bit (warm) indicates that the device awakens by a SMR source.

the current instruction, the opcode of the next instruction is fetched. Instruction pipelining is displayed in Figure 131.

Figure 131 and Figure 132 on page 139 display typical instruction cycle timing for instructions fetched from memory. For those instructions that require execution time longer than that of the overlapped fetch, or reference program or data memory as part of their execution, the pipe must be flushed.Figure 131 and Figure 132 on page 139 assume the XTAL ÷ 2 clock mode is selected.

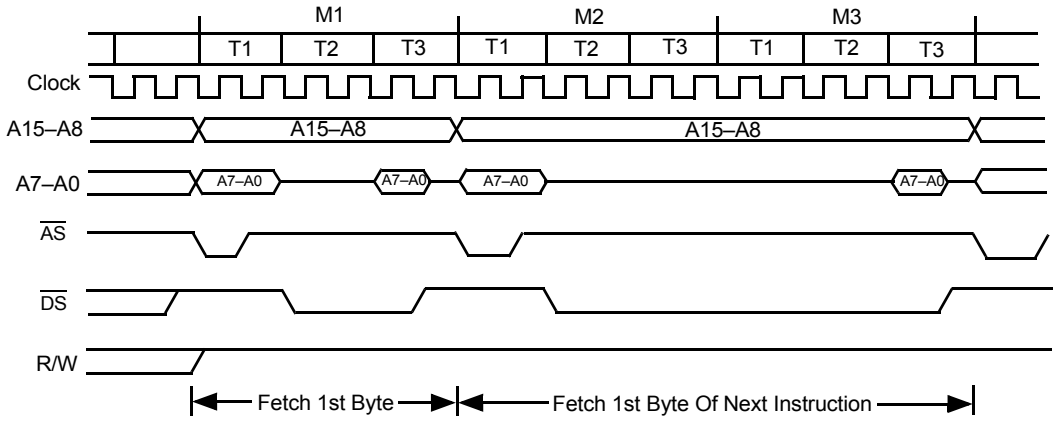


Figure 131. Instruction Cycle Timing (1-Byte Instructions)

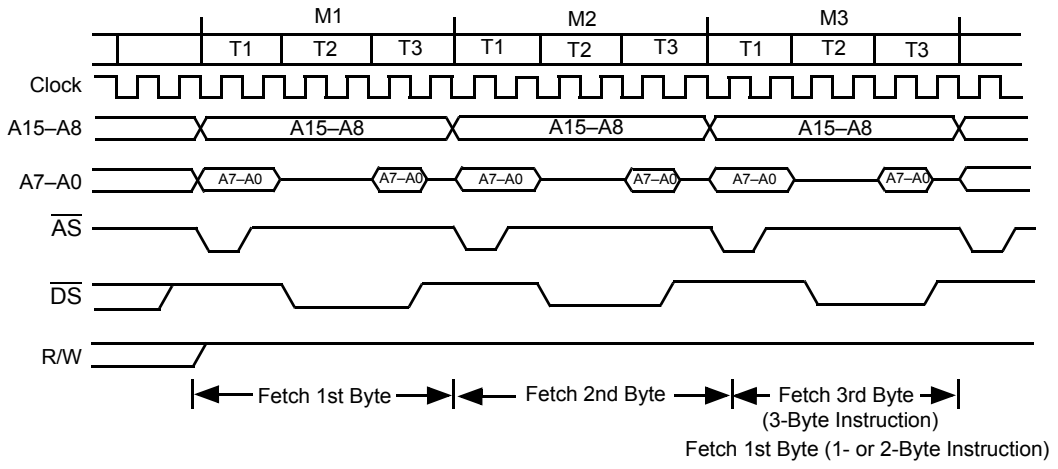


Figure 132. Instruction Cycle Timing (2- and 3-Byte Instructions)

Table 39. Summary of Z8 Instruction Set (Continued)

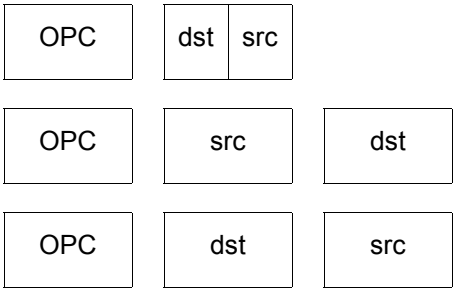
Instruction and Operation	Address Mode dst	Address Mode src	Op Code Byte (Hex)	Flags Affected C	Z	S	V	D	H
JP cc, dst	DA		cD	–	–	–	–	–	–
if cc is true,			c = 0–F						
then PC ⇑ dst	IRR		30						
JR cc, dst	RA		cB	–	–	–	–	–	–
if cc is true, PC ⇑ PC + dst Range: +127, –128			c = 0–F						
LD dst, src	r	Im	r C	–	–	–	–	–	–
dst ⇑ src	r	R	r 8						
	R	r	r 9						
			r = 0–F						
	r	X	C 7						
	X	r	D 7						
	r	Ir	E 3						
	Ir	r	F 3						
	R	R	E 4						
	R	IR	E 5						
	R	IM	E 6						
	IR	IM	E 7						
	IR	R	F 5						
LDC dst, src	r	Irr	C 2	–	–	–	–	–	–
dst ⇑ src	Irr	r	D 2						
LDCI dst, src	Ir	Irr	C 3	–	–	–	–	–	–
dst ⇑ src r ⇑ r + 1 or rr ⇑rr + 1	Irr	Ir	D 3						
LDE dst, src	r	Irr	82	–	–	–	–	–	–
dst ⇑ src	Irr	r	92						
LDEI dst, src	Ir	Irr	83	–	–	–	–	–	–

Add With Carry

Syntax

ADC dst, src

Instruction Format



Cycles	OPC (Hex)	Address Mode dst	Address Mode src
6	02	r	r
6	03	r	lr
10	04	R	R
10	05	R	IR
10	06	R	IM
10	07	IR	IM

Operation

dst ⇑ dst + src + C

The source operand, along with the setting of the Carry (C) Flag, is added to the destination operand. Two's complement addition is performed. The sum is stored in the destination operand. The contents of the source operand are not affected. In multiple precision arithmetic, this instruction permits the carry from the addition of low order operands to be carried into the addition of high order operands.

Flag	Description
C	Set if there is a carry from the most significant bit of the result; cleared otherwise.
Z	Set if the result is zero; cleared otherwise.
S	Set if the result is negative; cleared otherwise.
V	Set if an arithmetic overflow occurs, that is, if both operands are of the same sign and the result is of the opposite sign; cleared otherwise.
D	Always cleared.
H	Set if there is a carry from the most significant bit of the low order four bits of the result; cleared otherwise.

Note: Address modes R or IR can be used to specify 4-bit Working Register addresses. In this format, the source or destination Working Register operand is specified by adding 1110b (Eh) to the high nibble of the operand. For example, if Working Register R12 (CH) is the destination operand, then ECh is used as the destination operand in the Op Code.

- End the loop with DJNZ.
  The assembly listing required for this routine is as follows:

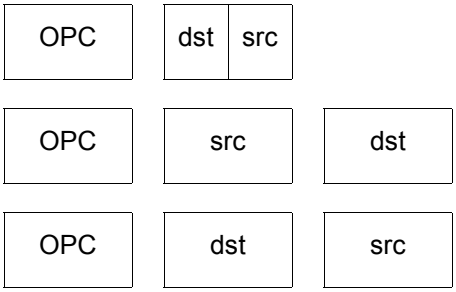
```
    LD R6, 12          ;Load Counter
LOOP: LD R9, @R6       ;Move one byte to
    LD @R6, R9         ;new location
    DJNZ R6, LOOP  ;Decrement and Loop until counter
                       ;= 0
```

Logical OR

Syntax

OR dst, src

Instruction Format



		Address Mode	
Cycles	OPC (Hex)	dst	src
6	02	r	r
6	03	r	Ir
10	04	R	R
10	05	R	IR
10	06	R	IM
10	07	IR	IM

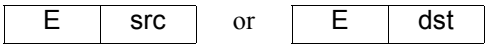
Operation

dst ⇑ dst OR src

The source operand is logically ORed with the destination operand and the result is stored in the destination operand. The contents of the source operand are not affected. The OR operation results in a one bit being stored whenever either of the corresponding bits in the two operands is a one. Otherwise, a zero bit is stored.

Flag	Description
C	Unaffected
Z	Set if the result is zero; cleared otherwise
S	Set if the result of bit 7 is set; cleared otherwise
V	Always reset to 0
D	Unaffected
H	Unaffected

Note: Address modes R or IR can be used to specify 4-bit Working Register addresses. In this format, the source or destination Working Register operand is specified by adding 1110b (Eh) to the high nibble of the operand. For example, if Working Register R12 is the destination operand, then ECh is used as the destination operand in the Op Code.



Logical Exclusive OR

Syntax

XOR dst, src

Instruction Format

			Cycles	OPC (Hex)	Address Mode dst	Address Mode src
OPC	dst | src		6	82	r	r
			6	83	r	lr
OPC	src	dst	10	84	R	R
			10	85	R	IR
OPC	dst	src	10	86	R	IM
			10	87	IR	IM

Operation

dst ⇑ dst XOR src

The source operand is logically EXCLUSIVE ORed with the destination operand. The XOR operation results in a 1 being stored in the destination operand whenever the corresponding bits in the two operands are different, otherwise a 0 is stored. The contents of the source operand are not affected.

C	Unaffected
Z	Set if the result is zero; cleared otherwise.
S	Set if the result of bit 7 is set; cleared otherwise.
V	Always reset to 0
D	Unaffected
H	Unaffected

Note: Address modes R or IR can be used to specify 4-bit Working Register addresses. In this format, the source or destination Working Register operand is specified by adding 1110b (Eh) to the high nibble of the operand. For example, if Working Register R12 (CH) is the destination operand, then ECh is used as the destination operand in the Op Code.

E	src	or	E	dst	

Example 6

If Working Register R3 contains the value 3Eh and Register 3Eh contains the value 6Ch (01101100b), the statement:

XOR @R3, #05h ♯
Op Code: B7 E3 05

leaves the value 69h (01101001b) in Register 3Eh. The Z, V, and S Flags are cleared.

Set Register Pointer

Syntax

SRP src

Instruction Format

		Cycles	OPC (Hex)	Address Mode dst
OPC	src	6	31	IM

Operation

RP ⇑ src

The specified value is loaded into the Register Pointer (RP) (Control Register FDh). Bits 7-4 determine the Working Register Group. Bits 3-0 selects the Expanded Register Bank. Addressing of un-implemented Working Register Group, while using Expanded Register Banks, points to Bank 0.

Example 1

SRP TD addresses Working Register Group 7 of Bank 0.

Register Pointer (FDh)	Working Register Group	Actual Registers
Contents (Bin)	(Hex)	(Hex)
1111 0000	F	F0–FF
1110 0000	E	E0–EF
1101 0000	D	D0–DF
1100 0000	C	C0–CF
1011 0000	B	B0–BF
1010 0000	A	A0–AF
1001 0000	9	90–9F
1000 0000	8	80–8F
0111 0000	7	70–7F
0110 0000	6	60–6F
0101 0000	5	50–5F
0100 0000	4	40–4F
0011 0000	3	30–3F
0010 0000	2	20–2F
0001 0000	1	10–1F
0000 0000	0	00–0F

Subtract

Syntax

SUB dst, src

Instruction Format

			Cycles	OPC (Hex)	Address Mode dst	Address Mode src
OPC	dst | src		6	22	r	r
			6	23	r	lr
OPC	src	dst	10	24	R	R
			10	25	R	IR
OPC	dst	src	10	26	R	IM
			10	27	IR	IM

Operation

dst ⇑ dst–src

The source operand is subtracted from the destination operand and the result is stored in the destination operand. The contents of the source operand are not affected. Subtraction is performed by adding the two's complement of the source operand to the destination operand.

Flag	Description
C	Cleared if there is a carry from the most significant bit of the result; set otherwise, indicating a *borrow*.
Z	Set if the result is 0; cleared otherwise.
V	Set if arithmetic overflow occurred (if the operands were of opposite sign and the sign of the result is the same as the sign of the source); reset otherwise.
S	Set if the result is negative; cleared otherwise.
H	Cleared if there is a carry from the most significant bit of the low order four bits of the result; set otherwise indicating a *borrow*.
D	Always set to 1.

Note: Address modes R or IR can be used to specify 4-bit Working Register addresses. In this format, the source or destination Working Register operand is specified by adding 1110b (Eh) to the high nibble of the operand. For example, if Working Register 12 (CH) is the destination operand, then ECh is used as the destination operand in the Op Code.

E	src	or	E	dst

Swap Nibbles

Syntax

SWAP dst

Instruction Format

		Cycles	OPC (Hex)	Address Mode dst
OPC	dst	6	F0	R
		6	F1	IR

Operation

dst(7-4) ⇐ dst(3-0)

The contents of the lower four bits and upper four bits of the destination operand are swapped.

Flag	Description
C	Unaffected
Z	Set if the result is zero; cleared otherwise.
S	Set if the result bit 7 is set; cleared otherwise.
V	Undefined
D	Unaffected
H	Unaffected

Note: Address modes R or IR can be used to specify a 4-bit Working Register. In this format, destination Working Register operand is specified by adding 1110b (Eh) to the high nibble of the operand. For example, if Working Register R12 (CH) is the destination operand, then ECh is used as the destination operand in the Op Code.

E	dst

Example 1

If Register BCh contains B3h (10110011B), the statement:

SWAP B3h
Op Code: F0 B3

leaves the value 3Bh (00111011B) in Register BCh. The Z and S Flags are cleared.

tests bit 1 of the destination operand for 0. The Z Flag is set indicating bit 1 in the destination operand was 0. The S and V Flags are cleared.

Example 6

If Register 5Dh contains A0h, and Register A0h contains 0Fh (00001111b), the statement:

```
TM @5D, #10h
Op Code: 77 5D 10
```

tests bit 4 of the Register A0h for 0. The Z Flag is set indicating bit 4 in the destination operand was 0. The S and V Flags are cleared.