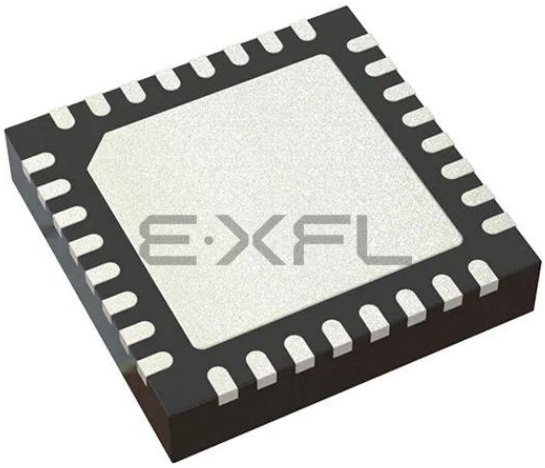

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Details	
Product Status	Discontinued at Digi-Key
Core Processor	80C52
Core Size	8-Bit
Speed	48MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART, USB
Peripherals	LED, POR, PWM, WDT
Number of I/O	18
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-VQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at83c5134-pntul

Figure 4-2. AT83C5134/35/36 48-pin MLF Pinout

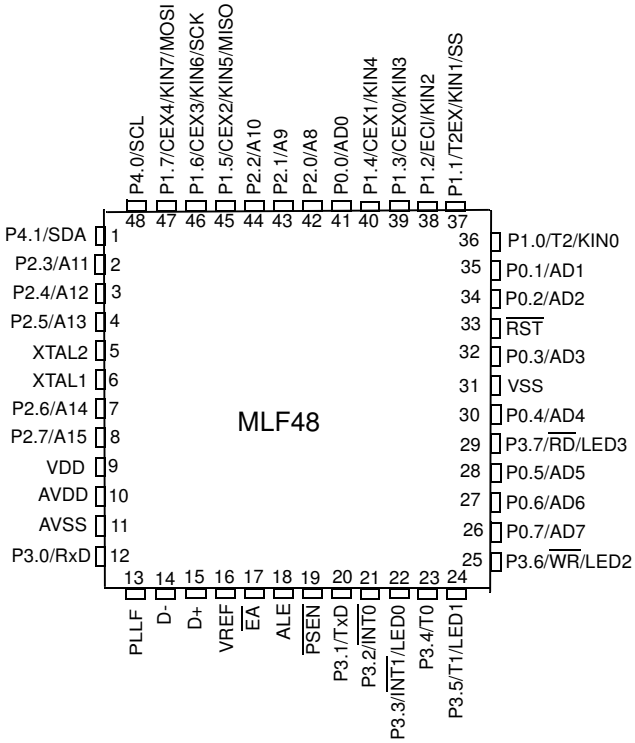


Figure 4-3. AT83C5134/35/36 28-pin SO Pinout

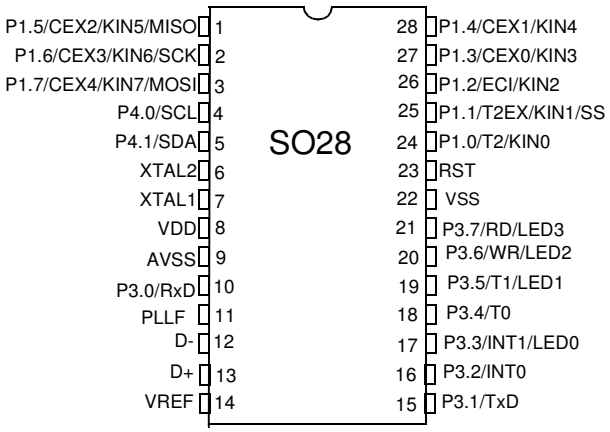
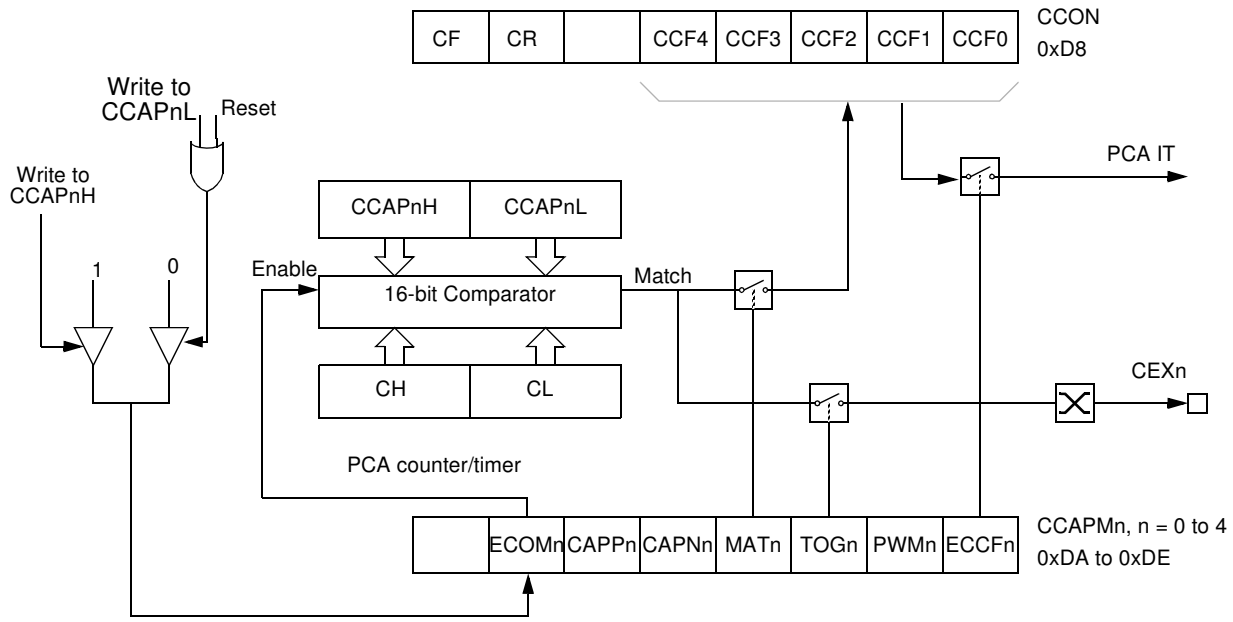


Figure 13-5. PCA High-speed Output Mode



Before enabling ECOM bit, CCAPnL and CCAPnH should be set with a non zero value, otherwise an unwanted match could happen.

Once ECOM set, writing CCAPnL will clear ECOM so that an unwanted match doesn't occur while modifying the compare value. Writing to CCAPnH will set ECOM. For this reason, user software should write CCAPnL first, and then CCAPnH. Of course, the ECOM bit can still be controlled by accessing to CCAPMn register.

13.4 Pulse Width Modulator Mode

All of the PCA modules can be used as PWM outputs. Figure 13-6 shows the PWM function. The frequency of the output depends on the source for the PCA timer. All of the modules will have the same frequency of output because they all share the PCA timer. The duty cycle of each module is independently variable using the module's capture register CCAPLn. When the value of the PCA CL SFR is less than the value in the module's CCAPLn SFR the output will be low, when it is equal to or greater than the output will be high. When CL overflows from FF to 00, CCAPLn is reloaded with the value in CCAPHn. This allows updating the PWM without glitches. The PWM and ECOM bits in the module's CCAPMn register must be set to enable the PWM mode.

Example of computed value when X2 = 1, SMOD1 = 1, SPD = 1

Baud Rates	F_{osc} = 16.384 MHz		F_{osc} = 24 MHz	
	BRL	Error (%)	BRL	Error (%)
115200	247	1.23	243	0.16
57600	238	1.23	230	0.16
38400	229	1.23	217	0.16
28800	220	1.23	204	0.16
19200	203	0.63	178	0.16
9600	149	0.31	100	0.16
4800	43	1.23	-	-

Example of computed value when X2 = 0, SMOD1 = 0, SPD = 0

Baud Rates	F_{osc} = 16.384 MHz		F_{osc} = 24 MHz	
	BRL	Error (%)	BRL	Error (%)
4800	247	1.23	243	0.16
2400	238	1.23	230	0.16
1200	220	1.23	202	3.55
600	185	0.16	152	0.16

The baud rate generator can be used for mode 1 or 3 (refer to Figure 14-4.), but also for mode 0 for UART, thanks to the bit SRC located in BDRCON register (Table 14-4.)

14.4 UART Registers

SADEN - Slave Address Mask Register for UART (B9h)

7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	–

Reset Value = 0000 0000b

SADDR - Slave Address Register for UART (A9h)

7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	–

Reset Value = 0000 0000b

SBUF - Serial Buffer Register for UART (99h)

7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	–

Reset Value = XXXX XXXXb

BRL - Baud Rate Reload Register for the internal baud rate generator, UART (9Ah)

7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	–

Reset Value = 0000 0000b

Table 14-2. T2CON Register

T2CON - Timer 2 Control Register (C8h)

7	6	5	4	3	2	1	0
TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2#	CP/RL2#

Bit Number	Bit Mnemonic	Description
7	TF2	**Timer 2 overflow Flag** Must be cleared by software. Set by hardware on Timer 2 overflow, if RCLK = 0 and TCLK = 0.
6	EXF2	**Timer 2 External Flag** Set when a capture or a reload is caused by a negative transition on T2EX pin if EXEN2 = 1. When set, causes the CPU to vector to Timer 2 interrupt routine when Timer 2 interrupt is enabled. Must be cleared by software. EXF2 doesn't cause an interrupt in Up/down counter mode (DCEN = 1)
5	RCLK	**Receive Clock bit for UART** Cleared to use Timer 1 overflow as receive clock for serial port in mode 1 or 3. Set to use Timer 2 overflow as receive clock for serial port in mode 1 or 3.
4	TCLK	**Transmit Clock bit for UART** Cleared to use Timer 1 overflow as transmit clock for serial port in mode 1 or 3. Set to use Timer 2 overflow as transmit clock for serial port in mode 1 or 3.
3	EXEN2	**Timer 2 External Enable bit** Cleared to ignore events on T2EX pin for Timer 2 operation. Set to cause a capture or reload when a negative transition on T2EX pin is detected, if Timer 2 is not used to clock the serial port.
2	TR2	**Timer 2 Run control bit** Cleared to turn off Timer 2. Set to turn on Timer 2.
1	C/T2#	**Timer/Counter 2 select bit** Cleared for timer operation (input from internal clock system: $F_{CLK\ PERIPH}$). Set for counter operation (input from T2 input pin, falling edge trigger). Must be 0 for clock out mode.
0	CP/RL2#	**Timer 2 Capture/Reload bit** If RCLK = 1 or TCLK = 1, CP/RL2# is ignored and timer is forced to Auto-reload on Timer 2 overflow. Cleared to Auto-reload on Timer 2 overflows or negative transitions on T2EX pin if EXEN2 = 1. Set to capture on negative transitions on T2EX pin if EXEN2 = 1.

Reset Value = 0000 0000b

Bit addressable

Table 16-3. IPL0 Register

IPL0 - Interrupt Priority Register (B8h)

7	6	5	4	3	2	1	0
-	PPCL	PT2L	PSL	PT1L	PX1L	PT0L	PX0L

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	PPCL	**PCA interrupt Priority bit** Refer to PPCH for priority level.
5	PT2L	**Timer 2 overflow interrupt Priority bit** Refer to PT2H for priority level.
4	PSL	**Serial port Priority bit** Refer to PSH for priority level.
3	PT1L	**Timer 1 overflow interrupt Priority bit** Refer to PT1H for priority level.
2	PX1L	**External interrupt 1 Priority bit** Refer to PX1H for priority level.
1	PT0L	**Timer 0 overflow interrupt Priority bit** Refer to PT0H for priority level.
0	PX0L	**External interrupt 0 Priority bit** Refer to PX0H for priority level.

Reset Value = x000 0000b

Bit addressable

Table 16-6. IPL1 Register

IPL1 - Interrupt Priority Register (B2h)

7	6	5	4	3	2	1	0
-	PUSBL	-	-	-	PSPIL	PTWIL	PKBDL

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	PUSBL	**USB Interrupt Priority bit** Refer to PUSBH for priority level.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	PSPIL	**SPI Interrupt Priority bit** Refer to PSPIH for priority level.
1	PTWIL	**TWI Interrupt Priority bit** Refer to PTWIH for priority level.
0	PKBL	**Keyboard Interrupt Priority bit** Refer to PKBH for priority level.

Reset Value = X0XX X000b

Not bit addressable

17.2.2 Power Reduction Mode

P1 inputs allow exit from idle and power down modes as detailed in section “Power-down Mode”.

17.3 Registers

Table 17-1. KBF Register

KBF - Keyboard Flag Register (9Eh)

7	6	5	4	3	2	1	0
KBF7	KBF6	KBF5	KBF4	KBF3	KBF2	KBF1	KBF0

Bit Number	Bit Mnemonic	Description
7	KBF7	**Keyboard line 7 flag** Set by hardware when the Port line 7 detects a programmed level. It generates a Keyboard interrupt request if the KBKBIE.7 bit in KBIE register is set. Cleared by hardware when reading KBF SFR by software.
6	KBF6	**Keyboard line 6 flag** Set by hardware when the Port line 6 detects a programmed level. It generates a Keyboard interrupt request if the KBIE.6 bit in KBIE register is set. Cleared by hardware when reading KBF SFR by software.
5	KBF5	**Keyboard line 5 flag** Set by hardware when the Port line 5 detects a programmed level. It generates a Keyboard interrupt request if the KBIE.5 bit in KBIE register is set. Cleared by hardware when reading KBF SFR by software.
4	KBF4	**Keyboard line 4 flag** Set by hardware when the Port line 4 detects a programmed level. It generates a Keyboard interrupt request if the KBIE.4 bit in KBIE register is set. Cleared by hardware when reading KBF SFR by software.
3	KBF3	**Keyboard line 3 flag** Set by hardware when the Port line 3 detects a programmed level. It generates a Keyboard interrupt request if the KBIE.3 bit in KBIE register is set. Cleared by hardware when reading KBF SFR by software.
2	KBF2	**Keyboard line 2 flag** Set by hardware when the Port line 2 detects a programmed level. It generates a Keyboard interrupt request if the KBIE.2 bit in KBIE register is set. Must be cleared by software.
1	KBF1	**Keyboard line 1 flag** Set by hardware when the Port line 1 detects a programmed level. It generates a Keyboard interrupt request if the KBIE.1 bit in KBIE register is set. Cleared by hardware when reading KBF SFR by software.
0	KBF0	**Keyboard line 0 flag** Set by hardware when the Port line 0 detects a programmed level. It generates a Keyboard interrupt request if the KBIE.0 bit in KBIE register is set. Cleared by hardware when reading KBF SFR by software.

Reset Value = 0000 0000b

18. Programmable LED

AT83C5134/35/36 have up to 4 programmable LED current sources, configured by the register LEDCON.

Table 18-1. LEDCON Register

LEDCON (S:F1h) LED Control Register

7	6	5	4	3	2	1	0
LED3		LED2		LED1		LED0	

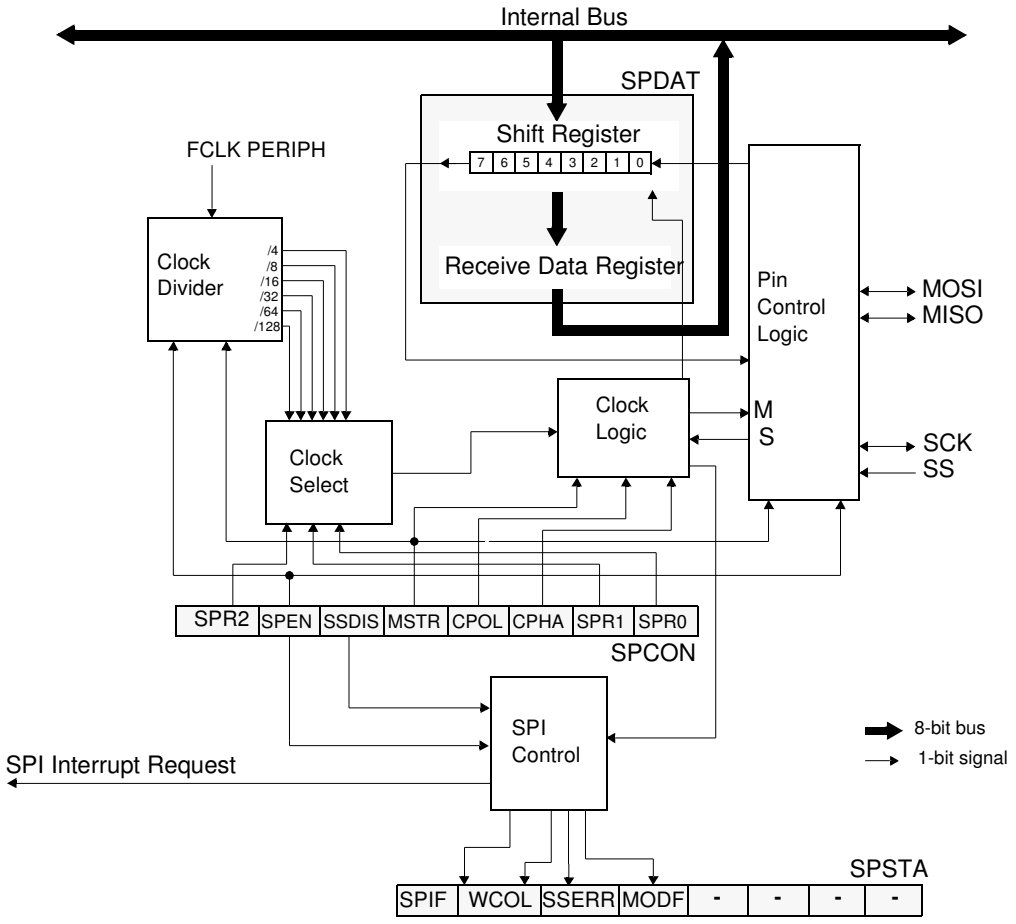
Bit Number	Bit Mnemonic	Description
7:6	LED3	**Port LED3 Configuration** 0 0 Standard C51 Port 0 1 2 mA current source when P3.7 is low 1 0 4 mA current source when P3.7 is low 1 1 10 mA current source when P3.7 is low
5:4	LED2	**Port /LED2 Configuration** 0 0 Standard C51 Port 0 1 2 mA current source when P3.6 is low 1 0 4 mA current source when P3.6 is low 1 1 10 mA current source when P3.6 is low
3:2	LED1	**Port/ LED1 Configuration** 0 0 Standard C51 Port 0 1 2 mA current source when P3.5 is low 1 0 4 mA current source when P3.5 is low 1 1 10 mA current source when P3.5 is low
1:0	LED0	**Port/ LED0 Configuration** 0 0 Standard C51 Port 0 1 2 mA current source when P3.3 is low 1 0 4 mA current source when P3.3 is low 1 1 10 mA current source when P3.3 is low

Reset Value = 00h

19.3 Functional Description

Figure 19-2 shows a detailed structure of the SPI module.

Figure 19-2. SPI Module Block Diagram



19.3.1 Operating Modes

The Serial Peripheral Interface can be configured as one of the two modes: Master mode or Slave mode. The configuration and initialization of the SPI module is made through one register:

- The Serial Peripheral CONtrol register (SPCON)

Once the SPI is configured, the data exchange is made using:

- SPCON
- The Serial Peripheral STAtus register (SPSTA)
- The Serial Peripheral DATa register (SPDAT)

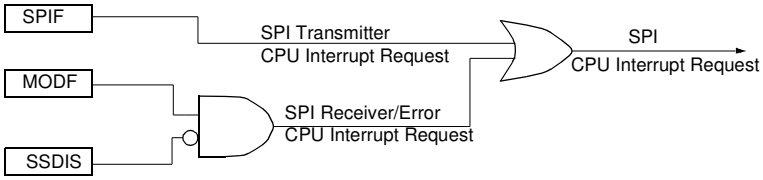
During an SPI transmission, data is simultaneously transmitted (shifted out serially) and received (shifted in serially). A serial clock line (SCK) synchronizes shifting and sampling on the two serial data lines (MOSI and MISO). A Slave Select line ($\overline{SS}$) allows individual selection of a Slave SPI device; Slave devices that are not selected do not interfere with SPI bus activities.

When the Master device transmits data to the Slave device via the MOSI line, the Slave device responds by sending data to the Master device via the MISO line. This implies full-duplex transmission with both data out and data in synchronized with the same clock (Figure 19-3).

Mode Fault flag, MODF: This bit becomes set to indicate that the level on the SS is inconsistent with the mode of the SPI. MODF with SSDIS reset, generates receiver/error CPU interrupt requests.

Figure 19-7 gives a logical view of the above statements.

Figure 19-7. SPI Interrupt Requests Generation



19.3.5 Registers

There are three registers in the module that provide control, status and data storage functions. These registers are describes in the following paragraphs.

19.3.5.1 Serial Peripheral Control Register (SPCON)

- The Serial Peripheral Control Register does the following:
  - Selects one of the Master clock rates
  - Configure the SPI module as Master or Slave
  - Selects serial clock polarity and phase
  - Enables the SPI module
  - Frees the SS pin for a general-purpose

Table 19-3 describes this register and explains the use of each bit.

Table 19-3. SPCON Register

7	6	5	4	3	2	1	0
SPR2	**SPEN**	**SSDIS**	**MSTR**	**CPOL**	**CPHA**	**SPR1**	**SPR0**

Bit Number	Bit Mnemonic	Description
7	SPR2	**Serial Peripheral Rate 2** Bit with SPR1 and SPR0 define the clock rate.
6	SPEN	**Serial Peripheral Enable** Cleared to disable the SPI interface. Set to enable the SPI interface.
5	SSDIS	**$\overline{SS}$ Disable** Cleared to enable $\overline{SS}$ in both Master and Slave modes. Set to disable $\overline{SS}$ in both Master and Slave modes. In Slave mode, this bit has no effect if CPHA = “0”.
5	MSTR	**Serial Peripheral Master** Cleared to configure the SPI as a Slave. Set to configure the SPI as a Master.
4	CPOL	**Clock Polarity** Cleared to have the SCK set to “0” in idle state. Set to have the SCK set to “1” in idle state.

20. Two Wire Interface (TWI)

This section describes the 2-wire interface. The 2-wire bus is a bi-directional 2-wire serial communication standard. It is designed primarily for simple but efficient integrated circuit (IC) control. The system is comprised of two lines, SCL (Serial Clock) and SDA (Serial Data) that carry information between the ICs connected to them. The serial data transfer is limited to 100 Kbit/s in standard mode. Various communication configuration can be designed using this bus. Figure 20-1 shows a typical 2-wire bus configuration. All the devices connected to the bus can be master and slave.

Figure 20-1. 2-wire Bus Configuration

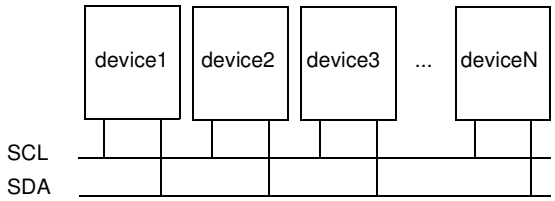
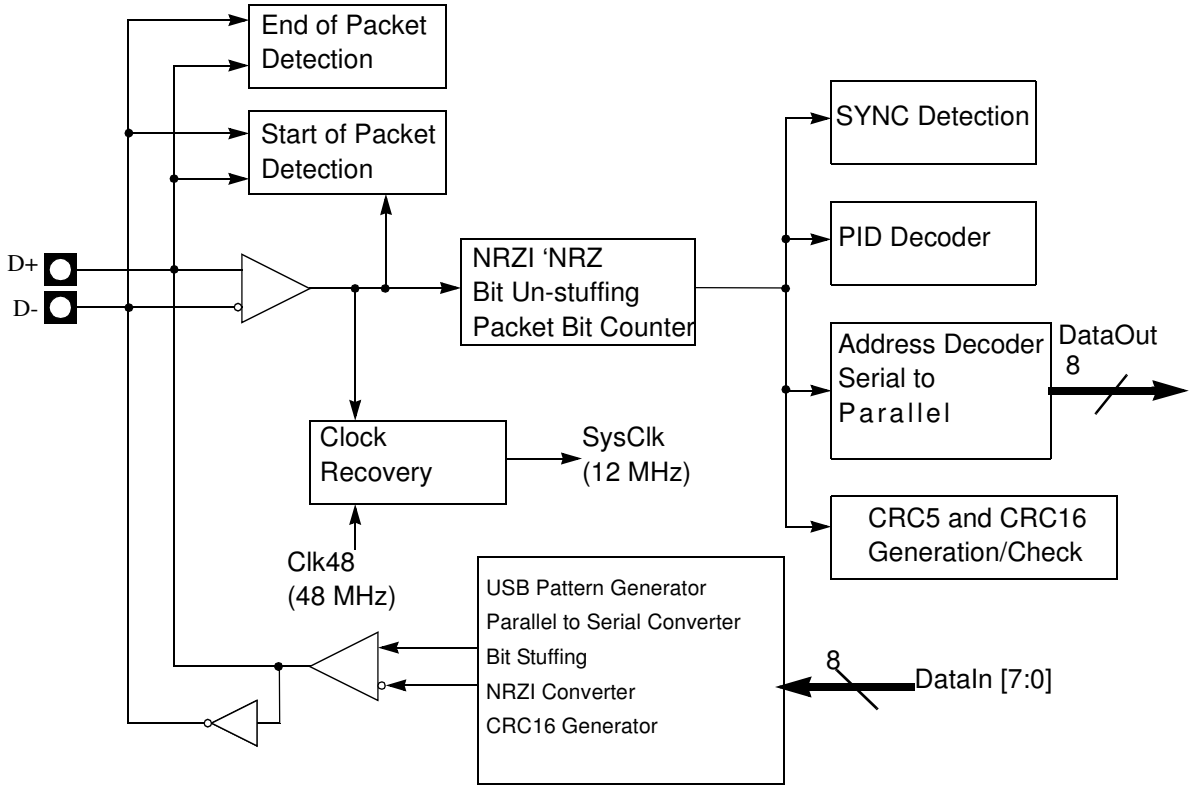


Table 20-6. Status in Master Receiver Mode

Status Code SSSTA	Status of the Two-wire Bus and Two-wire Hardware	Application software response					Next Action Taken by Two-wire Hardware
		To/From SSDAT	To SSCON				
			SSSTA	SSSTO	SSI	SSAA	
08h	A START condition has been transmitted	Write SLA+R	X	0	0	X	SLA+R will be transmitted.
10h	A repeated START condition has been transmitted	Write SLA+R	X	0	0	X	SLA+R will be transmitted.
		Write SLA+W	X	0	0	X	SLA+W will be transmitted. Logic will switch to master transmitter mode.
38h	Arbitration lost in SLA+R or NOT ACK bit	No SSDAT action	0	0	0	X	Two-wire bus will be released and not addressed slave mode will be entered.
		No SSDAT action	1	0	0	X	A START condition will be transmitted when the bus becomes free.
40h	SLA+R has been transmitted; ACK has been received	No SSDAT action	0	0	0	0	Data byte will be received and NOT ACK will be returned.
		No SSDAT action	0	0	0	1	Data byte will be received and ACK will be returned.
48h	SLA+R has been transmitted; NOT ACK has been received	No SSDAT action	1	0	0	X	Repeated START will be transmitted.
		No SSDAT action	0	1	0	X	STOP condition will be transmitted and SSSTO flag will be reset.
		No SSDAT action	1	1	0	X	STOP condition followed by a START condition will be transmitted and SSSTO flag will be reset.
50h	Data byte has been received; ACK has been returned	Read data byte	0	0	0	0	Data byte will be received and NOT ACK will be returned.
		Read data byte	0	0	0	1	Data byte will be received and ACK will be returned.
58h	Data byte has been received; NOT ACK has been returned	Read data byte	1	0	0	X	Repeated START will be transmitted.
		Read data byte	0	1	0	X	STOP condition will be transmitted and SSSTO flag will be reset.
		Read data byte	1	1	0	X	STOP condition followed by a START condition will be transmitted and SSSTO flag will be reset.

- Address checking.
- Clock generation (via DPLL).

Figure 21-2. SIE Block Diagram

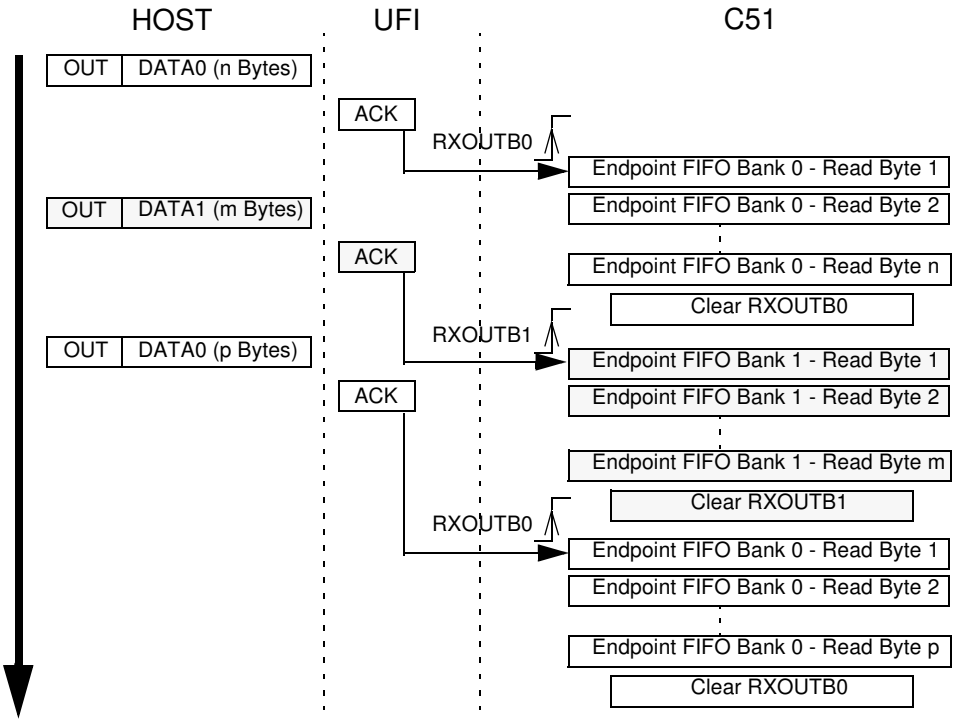


21.1.2 Function Interface Unit (FIU)

The Function Interface Unit provides the interface between the AT89C5131 and the SIE. It manages transactions at the packet level with minimal intervention from the device firmware, which reads and writes the endpoint FIFOs.

21.4.2 Bulk/Interrupt OUT Transactions in Ping-pong Mode

Figure 21-8. Bulk/Interrupt OUT Transactions in Ping-pong Mode



An endpoint will be first enabled and configured before being able to receive Bulk or Interrupt packets.

When a valid OUT packet is received on the endpoint bank 0, the RXOUTB0 bit is set by the USB controller. This triggers an interrupt if enabled. The firmware has to select the corresponding endpoint, store the number of data bytes by reading the UBYCTLX and UBYCTHX registers. If the received packet is a ZLP (Zero Length Packet), the UBYCTLX and UBYCTHX register values are equal to 0 and no data has to be read.

When all the endpoint FIFO bytes have been read, the firmware will clear the RXOUB0 bit to allow the USB controller to accept the next OUT packet on the endpoint bank 0. This action switches the endpoint bank 0 and 1. Until the RXOUTB0 bit has been cleared by the firmware, the USB controller will answer a NAK handshake for each OUT requests on the bank 0 endpoint FIFO.

When a new valid OUT packet is received on the endpoint bank 1, the RXOUTB1 bit is set by the USB controller. This triggers an interrupt if enabled. The firmware empties the bank 1 endpoint FIFO before clearing the RXOUTB1 bit. Until the RXOUTB1 bit has been cleared by the firmware, the USB controller will answer a NAK handshake for each OUT requests on the bank 1 endpoint FIFO.

The RXOUTB0 and RXOUTB1 bits are alternatively set by the USB controller at each new valid packet receipt.
The firmware has to clear one of these two bits after having read all the data FIFO to allow a new valid packet to be stored in the corresponding bank.

Table 21-2. Priority Levels

IPHUSB	IPLUSB	USB Priority Level
0	0	0 Lowest
0	1	1
1	0	2
1	1	3 Highest

21.10.2 USB Interrupt Control System

As shown in Figure 21-16, many events can produce a USB interrupt:

- TXCMPL: Transmitted In Data (see Table 21-9 on page 125). This bit is set by hardware when the Host accept a In packet.
- RXOUTB0: Received Out Data Bank 0 (see Table 21-9 on page 125). This bit is set by hardware when an Out packet is accepted by the endpoint and stored in bank 0.
- RXOUTB1: Received Out Data Bank 1 (only for Ping-pong endpoints) (see Table 21-9 on page 125). This bit is set by hardware when an Out packet is accepted by the endpoint and stored in bank 1.
- RXSETUP: Received Setup (see Table 21-9 on page 125). This bit is set by hardware when an SETUP packet is accepted by the endpoint.
- STLCRC: STALLED (only for Control, Bulk and Interrupt endpoints) (see Table 21-9 on page 125). This bit is set by hardware when a STALL handshake has been sent as requested by STALLRQ, and is reset by hardware when a SETUP packet is received.
- SOFINT: Start of Frame Interrupt (See “USBIEN Register USBIEN (S:BEh) USB Global Interrupt Enable Register” on page 122.). This bit is set by hardware when a USB Start of Frame packet has been received.
- WUPCPU: Wake-Up CPU Interrupt (See “USBIEN Register USBIEN (S:BEh) USB Global Interrupt Enable Register” on page 122.). This bit is set by hardware when a USB resume is detected on the USB bus, after a SUSPEND state.
- SPINT: Suspend Interrupt (See “USBIEN Register USBIEN (S:BEh) USB Global Interrupt Enable Register” on page 122.). This bit is set by hardware when a USB suspend is detected on the USB bus.

Table 21-10. UEPDATX Register
UEPDATX (S:CFh)
USB FIFO Data Endpoint X (X = EPNUM set in UEPNUM Register UEPNUM (S:C7h) USB Endpoint Number)

7	6	5	4	3	2	1	0
FDAT7	FDAT6	FDAT5	FDAT4	FDAT3	FDAT2	FDAT1	FDAT0

Bit Number	Bit Mnemonic	Description
7 - 0	FDAT[7:0]	**Endpoint X FIFO data** Data byte to be written to FIFO or data byte to be read from the FIFO, for the Endpoint X (see EPNUM).

Reset Value = XXh

Table 21-11. UBYCTLX Register
UBYCTLX (S:E2h)
USB Byte Count Low Register X (X = EPNUM set in UEPNUM Register UEPNUM (S:C7h) USB Endpoint Number)

7	6	5	4	3	2	1	0
BYCT7	BYCT6	BYCT5	BYCT4	BYCT3	BYCT2	BYCT1	BYCT0

Bit Number	Bit Mnemonic	Description
7 - 0	BYCT[7:0]	**Byte Count LSB** Least Significant Byte of the byte count of a received data packet. The most significant part is provided by the UBYCTHX Register UBYCTHX (S:E3h) USB Byte Count High Register X (X = EPNUM set in UEPNUM Register UEPNUM (S:C7h) USB Endpoint Number) (see Figure 21-11 on page 126). This byte count is equal to the number of data bytes received after the Data PID.

Reset Value = 00h

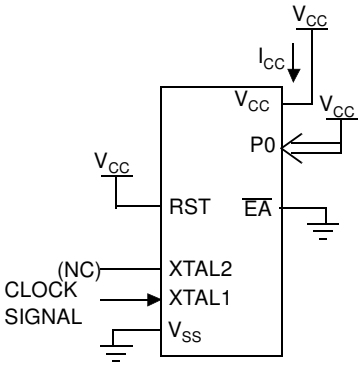
Table 21-12. UBYCTHX Register
UBYCTHX (S:E3h)
USB Byte Count High Register X (X = EPNUM set in UEPNUM Register UEPNUM (S:C7h) USB Endpoint Number)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	BYCT9	BYCT8

Bit Number	Bit Mnemonic	Description
7-2	-	**Reserved** The value read from these bits is always 0. Do not set these bits.
2-0	BYCT[10:8]	**Byte Count MSB** Most Significant Byte of the byte count of a received data packet. The Least significant part is provided by UBYCTLX Register UBYCTLX (S:E2h) USB Byte Count Low Register X (X = EPNUM set in UEPNUM Register UEPNUM (S:C7h) USB Endpoint Number) (see Figure 21-11 on page 126).

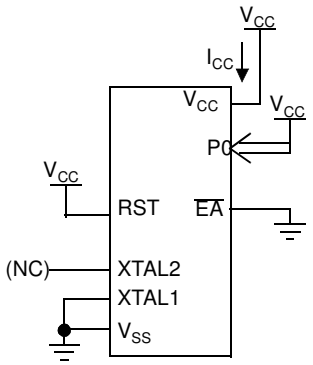
Reset Value = 00h

Figure 27-2. I_{CC} Test Condition, Idle Mode



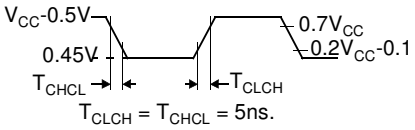
All other pins are disconnected.

Figure 27-3. I_{CC} Test Condition, Power-down Mode



All other pins are disconnected.

Figure 27-4. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes



27.2.1 LED's

Table 27-1. LED Outputs DC Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{OL}	Output Low Current, P3.6 and P3.7 LED modes	1	2	4	mA	2 mA configuration
		2	4	8	mA	4 mA configuration
		5	10	20	mA	10 mA configuration

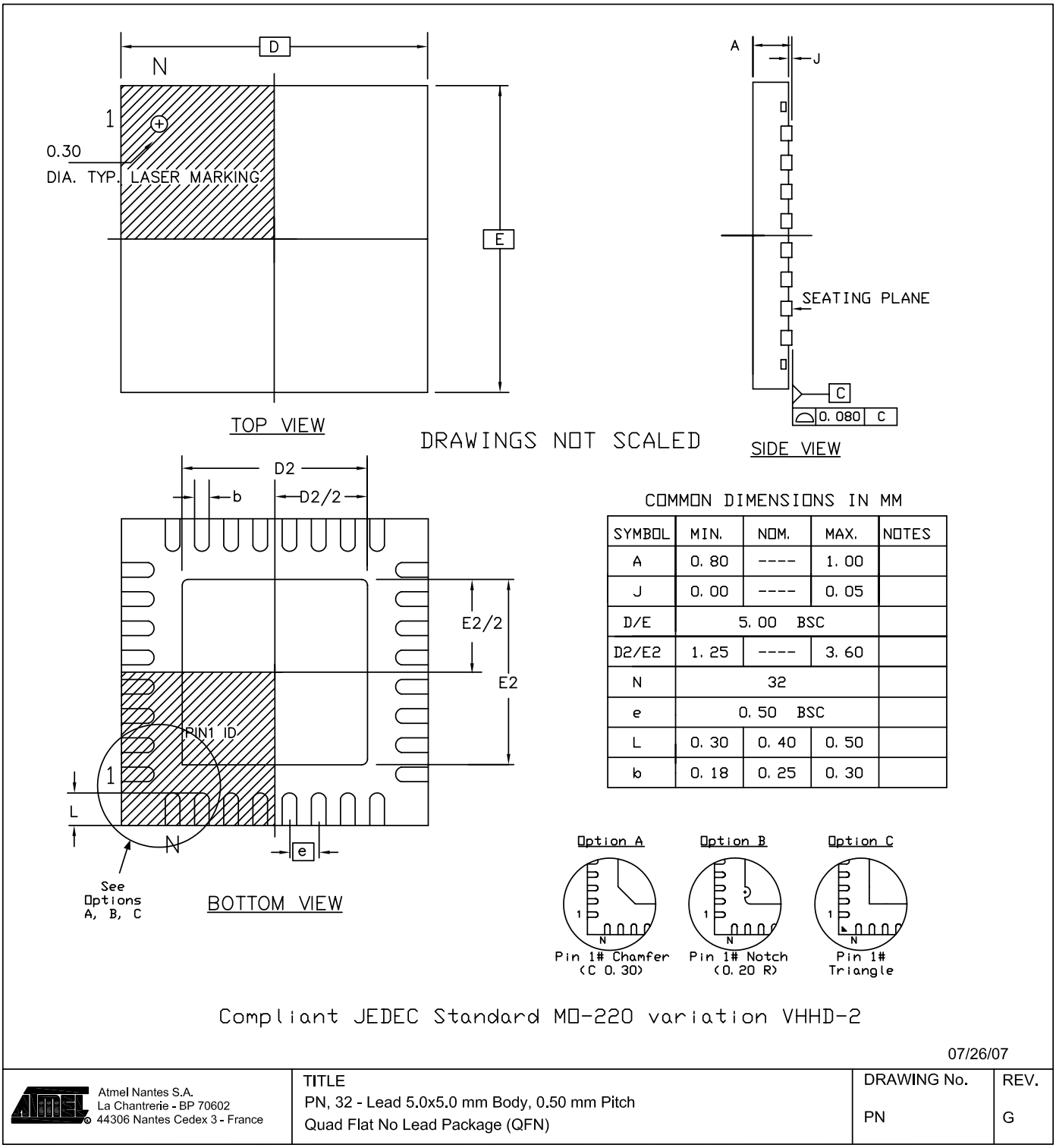
Note: 1. (T_A = -20°C to +50°C, V_{CC} - V_{OL} = 2 V ± 20%)

28. Ordering Information

Table Possible Order Entries

Part Number	Memory Size	Supply Voltage	Temperature Range	Package	Packing
AT83C5134xxx-PNTUL	8KB	2.7 to 3.6V	Industrial & Green	QFN32	Tray
AT83C5135xxx-PNTUL	16KB	2.7 to 3.6V	Industrial & Green	QFN32	Tray
AT83C5136xxx-PNTUL	32KB	2.7 to 3.6V	Industrial & Green	QFN32	Tray
AT83C5136xxx-PLTUL	32KB	2.7 to 3.6V	Industrial & Green	QFN/MLF48	Tray
AT83C5136xxx-TISUL	32KB	2.7 to 3.6V	Industrial & Green	SO28	Stick
AT83C5136-RDTUL	32	2.7 to 3.6V	Industrial & Green	VQFP64	Tray
AT83C5136xxx-DDW	32KB	2.7 to 3.6V	Industrial & Green	Die	Inked Wafer
AT83EC5136xxx-PNTUL	32KB with 512-byte of EEPROM	2.7 to 3.6V	Industrial & Green	QFN/MLF48	Tray
AT83EI5136xxx-PNTUL	32KB with 32-kbyte of EEPROM	2.7 to 3.6V	Industrial & Green	QFN/MLF48	Tray

29.4 QFN32



SYMBOL	MIN.	NOM.	MAX.	NOTES
A	0.80	----	1.00	
J	0.00	----	0.05	
D/E		5.00 BSC		
D2/E2	1.25	----	3.60	
N		32		
e		0.50 BSC		
L	0.30	0.40	0.50	
b	0.18	0.25	0.30	

Atmel Nantes S.A. La Chantrerie - BP 70602 44306 Nantes Cedex 3 - France	TITLE PN, 32 - Lead 5.0x5.0 mm Body, 0.50 mm Pitch Quad Flat No Lead Package (QFN)	DRAWING No. PN	REV. G