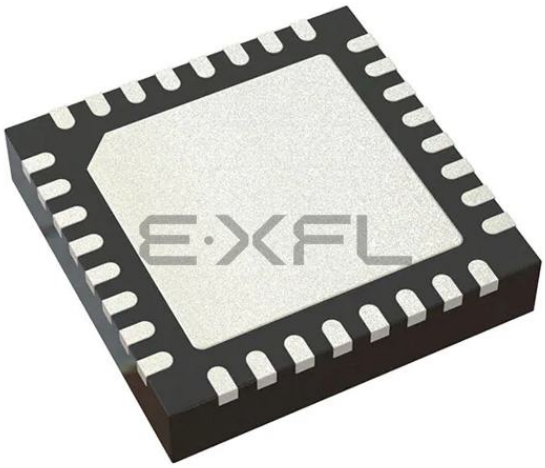

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	80C52
Core Size	8-Bit
Speed	48MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART, USB
Peripherals	LED, POR, PWM, WDT
Number of I/O	18
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-VQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at83c5135-pntul

Oscillator Frequency	R+1	N+1	PLLDIV
32 MHz	3	2	21h
40 MHz	12	10	B9h

6.4 Registers

Table 6-2. CKCON0 (S:8Fh)
Clock Control Register 0

7	6	5	4	3	2	1	0
TWIX2	WDX2	PCAX2	SIX2	T2X2	T1X2	T0X2	X2

Bit Number	Bit Mnemonic	Description
7	TWIX2	TWI Clock This control bit is validated when the CPU clock X2 is set. When X2 is low, this bit has no effect. Clear to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
6	WDX2	Watchdog Clock This control bit is validated when the CPU clock X2 is set. When X2 is low, this bit has no effect. Clear to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
5	PCAX2	Programmable Counter Array Clock This control bit is validated when the CPU clock X2 is set. When X2 is low, this bit has no effect. Clear to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
4	SIX2	Enhanced UART Clock (Mode 0 and 2) This control bit is validated when the CPU clock X2 is set. When X2 is low, this bit has no effect. Clear to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
3	T2X2	Timer2 Clock This control bit is validated when the CPU clock X2 is set. When X2 is low, this bit has no effect. Clear to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
2	T1X2	Timer1 Clock This control bit is validated when the CPU clock X2 is set. When X2 is low, this bit has no effect. Clear to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
1	T0X2	Timer0 Clock This control bit is validated when the CPU clock X2 is set. When X2 is low, this bit has no effect. Clear to select 6 clock periods per peripheral clock cycle. Set to select 12 clock periods per peripheral clock cycle.
0	X2	System Clock Control bit Clear to select 12 clock periods per machine cycle (STD mode, $F_{CPU} = F_{PER} = F_{OSC}/2$). Set to select 6 clock periods per machine cycle (X2 mode, $F_{CPU} = F_{PER} = F_{OSC}$).

Reset Value = 0000 0000b

Table 7-4. Timer SFR s (Continued)

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
RCAP2H	CBh	Timer/Counter 2 Reload/Capture High byte								
RCAP2L	CAh	Timer/Counter 2 Reload/Capture Low byte								
WDTRST	A6h	WatchDog Timer Reset								
WDTPRG	A7h	WatchDog Timer Program						S2	S1	S0

Table 7-5. Serial I/O Port SFR s

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
SCON	98h	Serial Control	FE/SM0	SM1	SM2	REN	TB8	RB8	TI	RI
SBUF	99h	Serial Data Buffer								
SADEN	B9h	Slave Address Mask								
SADDR	A9h	Slave Address								

Table 7-6. Baud Rate Generator SFR s

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
BRL	9Ah	Baud Rate Reload								
BDRCON	9Bh	Baud Rate Control				BRR	TBCK	RBCK	SPD	SRC

Table 7-7. PCA SFR s

Mnemo-nic	Add	Name	7	6	5	4	3	2	1	0
CCON	D8h	PCA Timer/Counter Control	CF	CR		CCF4	CCF3	CCF2	CCF1	CCF0
CMOD	D9h	PCA Timer/Counter Mode	CIDL	WDTE				CPS1	CPS0	ECF
CL	E9h	PCA Timer/Counter Low byte								
CH	F9h	PCA Timer/Counter High byte								
CCAPM0	DAh	PCA Timer/Counter Mode 0		ECOM0	CAPP0	CAPN0	MAT0	TOG0	PWM0	ECCF0
CCAPM1	DBh	PCA Timer/Counter Mode 1		ECOM1	CAPP1	CAPN1	MAT1	TOG1	PWM1	ECCF1
CCAPM2	DCh	PCA Timer/Counter Mode 2		ECOM2	CAPP2	CAPN2	MAT2	TOG2	PWM2	ECCF2
CCAPM3	DDh	PCA Timer/Counter Mode 3		ECOM3	CAPP3	CAPN3	MAT3	TOG3	PWM3	ECCF3
CCAPM4	DEh	PCA Timer/Counter Mode 4		ECOM4	CAPP4	CAPN4	MAT4	TOG4	PWM4	ECCF4

Table 7-7. PCA SFR s

Mnemo-nic	Add	Name	7	6	5	4	3	2	1	0
CCAP0H CCAP1H CCAP2H CCAP3H CCAP4H	 FAh FBh FCh FDh FEh	PCA Compare Capture Module 0 H PCA Compare Capture Module 1 H PCA Compare Capture Module 2 H PCA Compare Capture Module 3 H PCA Compare Capture Module 4 H	 CCAP0H7 CCAP1H7 CCAP2H7 CCAP3H7 CCAP4H7	 CCAP0H6 CCAP1H6 CCAP2H6 CCAP3H6 CCAP4H6	 CCAP0H5 CCAP1H5 CCAP2H5 CCAP3H5 CCAP4H5	 CCAP0H4 CCAP1H4 CCAP2H4 CCAP3H4 CCAP4H4	 CCAP0H3 CCAP1H3 CCAP2H3 CCAP3H3 CCAP4H3	 CCAP0H2 CCAP1H2 CCAP2H2 CCAP3H2 CCAP4H2	 CCAP0H1 CCAP1H1 CCAP2H1 CCAP3H1 CCAP4H1	 CCAP0H0 CCAP1H0 CCAP2H0 CCAP3H0 CCAP4H0
CCAP0L CCAP1L CCAP2L CCAP3L CCAP4L	 EAh EBh ECh EDh EEh	PCA Compare Capture Module 0 L PCA Compare Capture Module 1 L PCA Compare Capture Module 2 L PCA Compare Capture Module 3 L PCA Compare Capture Module 4 L	 CCAP0L7 CCAP1L7 CCAP2L7 CCAP3L7 CCAP4L7	 CCAP0L6 CCAP1L6 CCAP2L6 CCAP3L6 CCAP4L6	 CCAP0L5 CCAP1L5 CCAP2L5 CCAP3L5 CCAP4L5	 CCAP0L4 CCAP1L4 CCAP2L4 CCAP3L4 CCAP4L4	 CCAP0L3 CCAP1L3 CCAP2L3 CCAP3L3 CCAP4L3	 CCAP0L2 CCAP1L2 CCAP2L2 CCAP3L2 CCAP4L2	 CCAP0L1 CCAP1L1 CCAP2L1 CCAP3L1 CCAP4L1	 CCAP0L0 CCAP1L0 CCAP2L0 CCAP3L0 CCAP4L0

Table 7-8. Interrupt SFR s

Mnemo-nic	Add	Name	7	6	5	4	3	2	1	0
IEN0	A8h	Interrupt Enable Control 0	EA	EC	ET2	ES	ET1	EX1	ET0	EX0
IEN1	B1h	Interrupt Enable Control 1		EUSB				ESPI	ETWI	EKB
IPL0	B8h	Interrupt Priority Control Low 0		PPCL	PT2L	PSL	PT1L	PX1L	PT0L	PX0L
IPH0	B7h	Interrupt Priority Control High 0		PPCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H
IPL1	B2h	Interrupt Priority Control Low 1		PUSBL				PSPIL	PTWIL	PKBL
IPH1	B3h	Interrupt Priority Control High 1		PUSBH				PSPIH	PTWIH	PKBH

Table 7-9. PLL SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
PLLCON	A3h	PLL Control						EXT48	PLLEN	PLOCK
PLLDIV	A4h	PLL Divider	R3	R2	R1	R0	N3	N2	N1	N0

Table 7-10. Keyboard SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
KBF	9Eh	Keyboard Flag Register	KBF7	KBF6	KBF5	KBF4	KBF3	KBF2	KBF1	KBF0
KBE	9Dh	Keyboard Input Enable Register	KBE7	KBE6	KBE5	KBE4	KBE3	KBE2	KBE1	KBE0

12. Timer 2

The Timer 2 in the AT83C5134/35/36 is the standard C52 Timer 2. It is a 16-bit timer/counter: the count is maintained by two cascaded eight-bit timer registers, TH2 and TL2. It is controlled by T2CON (Table 12-1) and T2MOD (Table 12-2) registers. Timer 2 operation is similar to Timer 0 and Timer 1. C/$\overline{T2}$ selects $F_{OSC}/12$ (timer operation) or external pin T2 (counter operation) as the timer clock input. Setting TR2 allows TL2 to be incremented by the selected input.

Timer 2 has 3 operating modes: capture, auto reload and Baud Rate Generator. These modes are selected by the combination of RCLK, TCLK and CP/$\overline{RL2}$ (T2CON).

Refer to the Atmel 8-bit microcontroller hardware documentation for the description of Capture and Baud Rate Generator Modes.

Timer 2 includes the following enhancements:

- Auto-reload mode with up or down counter
- Programmable Clock-output

12.1 Auto-reload Mode

The Auto-reload mode configures Timer 2 as a 16-bit timer or event counter with automatic reload. If DCEN bit in T2MOD is cleared, Timer 2 behaves as in 80C52 (refer to the Atmel 8-bit microcontroller hardware description). If DCEN bit is set, Timer 2 acts as an Up/down timer/counter as shown in Figure 12-1. In this mode the T2EX pin controls the direction of count.

When T2EX is high, Timer 2 counts up. Timer overflow occurs at FFFFh which sets the TF2 flag and generates an interrupt request. The overflow also causes the 16-bit value in RCAP2H and RCAP2L registers to be loaded into the timer registers TH2 and TL2.

When T2EX is low, Timer 2 counts down. Timer underflow occurs when the count in the timer registers TH2 and TL2 equals the value stored in RCAP2H and RCAP2L registers. The underflow sets TF2 flag and reloads FFFFh into the timer registers.

The EXF2 bit toggles when Timer 2 overflows or underflows according to the direction of the count. EXF2 does not generate any interrupt. This bit can be used to provide 17-bit resolution.

13. Programmable Counter Array (PCA)

The PCA provides more timing capabilities with less CPU intervention than the standard timer/counters. Its advantages include reduced software overhead and improved accuracy. The PCA consists of a dedicated timer/counter which serves as the time base for an array of five compare/capture modules. Its clock input can be programmed to count any one of the following signals:

Peripheral clock frequency ($F_{CLK\ PERIPH}$) , 6

Peripheral clock frequency ($F_{CLK\ PERIPH}$) , 2

Timer 0 overflow

External input on ECI (P1.2)

Each compare/capture modules can be programmed in any one of the following modes:

rising and/or falling edge capture,

software timer

high-speed output, or

pulse width modulator

Module 4 can also be programmed as a watchdog timer (see Section "PCA Watchdog Timer", page 48).

When the compare/capture modules are programmed in the capture mode, software timer, or high speed output mode, an interrupt can be generated when the module executes its function. All five modules plus the PCA timer overflow share one interrupt vector.

The PCA timer/counter and compare/capture modules share Port 1 for external I/O. These pins are listed below. If the port pin is not used for the PCA, it can still be used for standard I/O.

PCA Component	External I/O Pin
16-bit Counter	P1.2/ECI
16-bit Module 0	P1.3/CEX0
16-bit Module 1	P1.4/CEX1
16-bit Module 2	P1.5/CEX2
16-bit Module 3	P1.6/CEX3
16-bit Module 4	P1.7/CEX4

The PCA timer is a common time base for all five modules (see Figure 13-1). The timer count source is determined from the CPS1 and CPS0 bits in the CMOD register (Table 13-1) and can be programmed to run at:

1/6 the peripheral clock frequency ($F_{CLK\ PERIPH}$).

1/2 the peripheral clock frequency ($F_{CLK\ PERIPH}$).

The Timer 0 overflow

The input on the ECI pin (P1.2)

Reset Value = 00XX X000b
Not bit addressable

The CMOD register includes three additional bits associated with the PCA (See Figure 13-1 and Table 13-1).

The CIDL bit allows the PCA to stop during idle mode.

The WDTE bit enables or disables the watchdog function on module 4.

The ECF bit when set causes an interrupt and the PCA overflow flag CF (in the CCON SFR) to be set when the PCA timer overflows.

The CCON register contains the run control bit for the PCA and the flags for the PCA timer (CF) and each module (see Table 13-2).

Bit CR (CCON.6) must be set by software to run the PCA. The PCA is shut off by clearing this bit.

Bit CF: The CF bit (CCON.7) is set when the PCA counter overflows and an interrupt will be generated if the ECF bit in the CMOD register is set. The CF bit can only be cleared by software.

Bits 0 through 4 are the flags for the modules (bit 0 for module 0, bit 1 for module 1, etc.) and are set by hardware when either a match or a capture occurs. These flags can only be cleared by software.

Table 13-2. CCON Register

CCON - PCA Counter Control Register (D8h)

7	6	5	4	3	2	1	0
CF	CR		CCF4	CCF3	CCF2	CCF1	CCF0

Bit Number	Bit Mnemonic	Description
7	CF	PCA Counter Overflow flag Set by hardware when the counter rolls over. CF flags an interrupt if bit ECF in CMOD is set. CF may be set by either hardware or software but can only be cleared by software.
6	CR	PCA Counter Run control bit Must be cleared by software to turn the PCA counter off. Set by software to turn the PCA counter on.
5		Reserved The value read from this bit is indeterminate. Do not set this bit.
4	CCF4	PCA Module 4 interrupt flag Must be cleared by software. Set by hardware when a match or capture occurs.
3	CCF3	PCA Module 3 interrupt flag Must be cleared by software. Set by hardware when a match or capture occurs.
2	CCF2	PCA Module 2 interrupt flag Must be cleared by software. Set by hardware when a match or capture occurs.

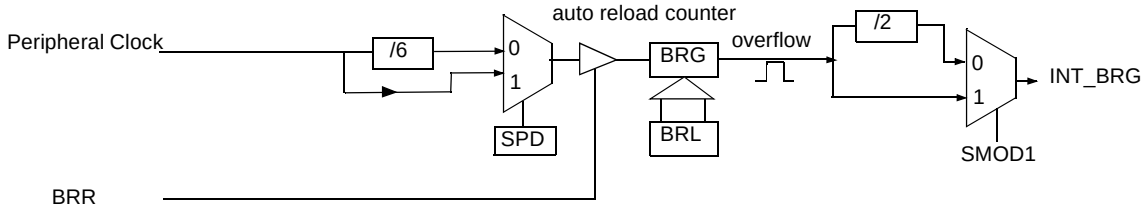
14.3.1 Baud Rate Selection Table for UART

TCLK (T2CON)	RCLK (T2CON)	TBCK (BDRCON)	RBCK (BDRCON)	Clock Source UART Tx	Clock Source UART Rx
0	0	0	0	Timer 1	Timer 1
1	0	0	0	Timer 2	Timer 1
0	1	0	0	Timer 1	Timer 2
1	1	0	0	Timer 2	Timer 2
X	0	1	0	INT_BRG	Timer 1
X	1	1	0	INT_BRG	Timer 2
0	X	0	1	Timer 1	INT_BRG
1	X	0	1	Timer 2	INT_BRG
X	X	1	1	INT_BRG	INT_BRG

14.3.2 Internal Baud Rate Generator (BRG)

When the internal Baud Rate Generator is used, the Baud Rates are determined by the BRG overflow depending on the BRL reload value, the value of SPD bit (Speed Mode) in BDRCON register and the value of the SMOD1 bit in PCON register.

Figure 14-5. Internal Baud Rate



The baud rate for UART is token by formula:

$$Baud\_Rate = \frac{2^{SMOD1} \times F_{CLK\ PERIPH}}{2 \times 6^{(1-SPD)} \times 16 \times [256 - (BRL)]}$$

$$(BRL) = 256 - \frac{2^{SMOD1} \times F_{CLK\ PERIPH}}{2 \times 6^{(1-SPD)} \times 16 \times Baud\_Rate}$$

Table 14-1. SCON Register SCON Serial Control Register (98h)

7	6	5	4	3	2	1	0
FE/SM0	SM1	SM2	REN	TB8	RB8	TI	RI

Table 16-4. IPH0 Register

IPH0 - Interrupt Priority High Register (B7h)

7	6	5	4	3	2	1	0
-	PPCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H

Bit Number	Bit Mnemonic	Description
7	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
6	PPCH	PCA interrupt Priority high bit. PPCH PPCL Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
5	PT2H	Timer 2 overflow interrupt Priority High bit PT2H PT2L Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
4	PSH	Serial port Priority High bit PSH PSL Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
3	PT1H	Timer 1 overflow interrupt Priority High bit PT1H PT1L Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
2	PX1H	External interrupt 1 Priority High bit PX1H PX1L Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
1	PT0H	Timer 0 overflow interrupt Priority High bit PT0H PT0L Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
0	PX0H	External interrupt 0 Priority High bit PX0H PX0L Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest

Reset Value = x000 0000b

Not bit addressable

16.3 Interrupt Sources and Vector Addresses

Table 16-8. Vector Table

Number	Polling Priority	Interrupt Source	Interrupt Request	Vector Address
0	0	Reset		0000h
1	1	INT0	IE0	0003h
2	2	Timer 0	TF0	000Bh
3	3	INT1	IE1	0013h
4	4	Timer 1	IF1	001Bh
5	6	UART	RI+TI	0023h
6	7	Timer 2	TF2+EXF2	002Bh
7	5	PCA	CF + CCFn (n = 0-4)	0033h
8	8	Keyboard	KBDIT	003Bh
9	9	TWI	TWIIT	0043h
10	10	SPI	SPIIT	004Bh
11	11			0053h
12	12			005Bh
13	13			0063h
14	14	USB	UEPINT + USBINT	006Bh
15	15			0073h