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Details	
Product Status	Discontinued at Digi-Key
Core Processor	80C52
Core Size	8-Bit
Speed	48MHz
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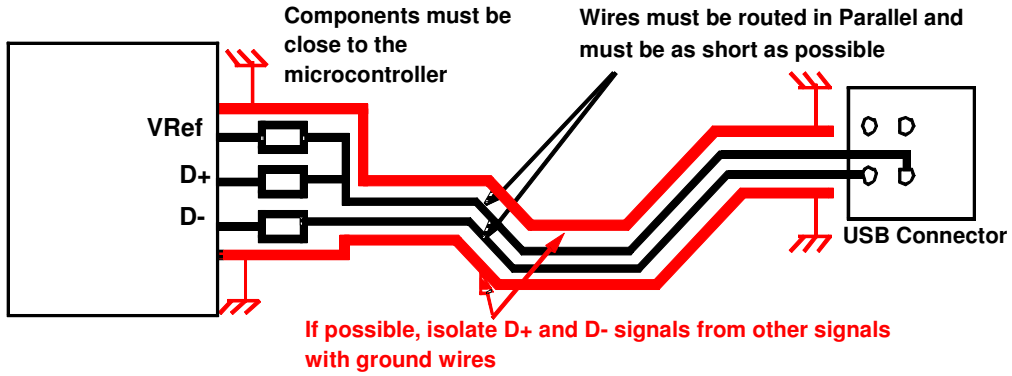
Peripherals	LED, POR, PWM, WDT
Number of I/O	18
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	-
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at83c5136-pntul

5.2 PCB Recommandations

Figure 5-2. USB Pads



Note: No sharp angle in above drawing.

Figure 5-3. USB PLL

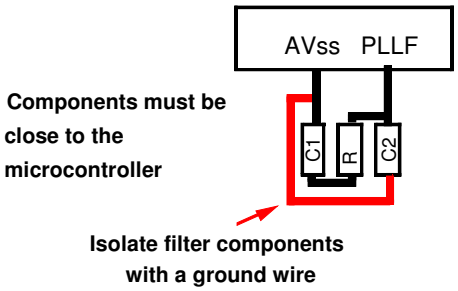


Table 7-7. PCA SFR's

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
CCAP0H CCAP1H CCAP2H CCAP3H CCAP4H	 FAh FBh FCh FDh FEh	PCA Compare Capture Module 0 H PCA Compare Capture Module 1 H PCA Compare Capture Module 2 H PCA Compare Capture Module 3 H PCA Compare Capture Module 4 H	 CCAP0H7 CCAP1H7 CCAP2H7 CCAP3H7 CCAP4H7	 CCAP0H6 CCAP1H6 CCAP2H6 CCAP3H6 CCAP4H6	 CCAP0H5 CCAP1H5 CCAP2H5 CCAP3H5 CCAP4H5	 CCAP0H4 CCAP1H4 CCAP2H4 CCAP3H4 CCAP4H4	 CCAP0H3 CCAP1H3 CCAP2H3 CCAP3H3 CCAP4H3	 CCAP0H2 CCAP1H2 CCAP2H2 CCAP3H2 CCAP4H2	 CCAP0H1 CCAP1H1 CCAP2H1 CCAP3H1 CCAP4H1	 CCAP0H0 CCAP1H0 CCAP2H0 CCAP3H0 CCAP4H0
CCAP0L CCAP1L CCAP2L CCAP3L CCAP4L	 EAh EBh ECh EDh EEh	PCA Compare Capture Module 0 L PCA Compare Capture Module 1 L PCA Compare Capture Module 2 L PCA Compare Capture Module 3 L PCA Compare Capture Module 4 L	 CCAP0L7 CCAP1L7 CCAP2L7 CCAP3L7 CCAP4L7	 CCAP0L6 CCAP1L6 CCAP2L6 CCAP3L6 CCAP4L6	 CCAP0L5 CCAP1L5 CCAP2L5 CCAP3L5 CCAP4L5	 CCAP0L4 CCAP1L4 CCAP2L4 CCAP3L4 CCAP4L4	 CCAP0L3 CCAP1L3 CCAP2L3 CCAP3L3 CCAP4L3	 CCAP0L2 CCAP1L2 CCAP2L2 CCAP3L2 CCAP4L2	 CCAP0L1 CCAP1L1 CCAP2L1 CCAP3L1 CCAP4L1	 CCAP0L0 CCAP1L0 CCAP2L0 CCAP3L0 CCAP4L0

Table 7-8. Interrupt SFR's

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
IEN0	A8h	Interrupt Enable Control 0	EA	EC	ET2	ES	ET1	EX1	ET0	EX0
IEN1	B1h	Interrupt Enable Control 1		EUSB				ESPI	ETWI	EKB
IPL0	B8h	Interrupt Priority Control Low 0		PPCL	PT2L	PSL	PT1L	PX1L	PT0L	PX0L
IPH0	B7h	Interrupt Priority Control High 0		PPCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H
IPL1	B2h	Interrupt Priority Control Low 1		PUSBL				PSPIL	PTWIL	PKBL
IPH1	B3h	Interrupt Priority Control High 1		PUSBH				PSPIH	PTWIH	PKBH

Table 7-9. PLL SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
PLLCON	A3h	PLL Control						EXT48	PLLEN	PLOCK
PLLDIV	A4h	PLL Divider	R3	R2	R1	R0	N3	N2	N1	N0

Table 7-10. Keyboard SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
KBF	9Eh	Keyboard Flag Register	KBF7	KBF6	KBF5	KBF4	KBF3	KBF2	KBF1	KBF0
KBE	9Dh	Keyboard Input Enable Register	KBE7	KBE6	KBE5	KBE4	KBE3	KBE2	KBE1	KBE0

9.2.1 Program ROM lock Bits

The lock bits when programmed according to Table 9-2 will provide different level of protection for the on-chip code and data.

Table 9-2. Program Lock bits

Program Lock Bits			Protection Description
Security level	**LB1**	**LB0**	
1	U	U	No program lock feature enabled.
3	P	U	Reading ROM data from programmer is disabled.

U: unprogrammed
P: programmed

Bit Number	Bit Mnemonic	Description
4	-	Reserved The value read from this bit is indeterminate. Do not set this bit
3	XRS1	ERAM Size **XRS1 XRS0 — ERAM size** 0 0 — 256 bytes 0 1 — 512 bytes 1 0 — 768 bytes 1 1 — 1024 bytes (default)
2	XRS0	
1	EXTRAM	**EXTRAM bit** Cleared to access internal ERAM using MOVX at $\overline{Ri}$ at DPTR. Set to access external memory.
0	AO	**ALE Output bit** Cleared, ALE is emitted at a constant rate of 1/6 the oscillator frequency (or 1/3 if X2 mode is used) (default). Set, ALE is active only when a MOVX or MOVC instruction is used.

Reset Value = 0X0X 1100b
Not bit addressable

Table 14-3. PCON Register

PCON - Power Control Register (87h)

7	6	5	4	3	2	1	0
SMOD1	**SMOD0**	**-**	**POF**	**GF1**	**GF0**	**PD**	**IDL**

Bit Number	Bit Mnemonic	Description
7	SMOD1	**Serial port Mode bit 1 for UART** Set to select double baud rate in mode 1, 2 or 3.
6	SMOD0	Serial port Mode bit 0 for UART Cleared to select SM0 bit in SCON register. Set to select FE bit in SCON register.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	POF	**Power-Off Flag** Cleared to recognize next reset type. Set by hardware when V_{CC} rises from 0 to its nominal voltage. Can also be set by software.
3	GF1	**General-purpose Flag** Cleared by user for general-purpose usage. Set by user for general-purpose usage.
2	GF0	**General-purpose Flag** Cleared by user for general-purpose usage. Set by user for general-purpose usage.
1	PD	**Power-down Mode Bit** Cleared by hardware when reset occurs. Set to enter power-down mode.
0	IDL	**Idle Mode Bit** Cleared by hardware when interrupt or reset occurs. Set to enter idle mode.

Reset Value = 00x1 0000b

Not bit addressable

Power-off flag reset value will be 1 only after a power on (cold reset). A warm reset doesn't affect the value of this bit.

Table 16-4. IPH0 Register

IPH0 - Interrupt Priority High Register (B7h)

7	6	5	4	3	2	1	0
-	PPCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	PPCH	**PCA interrupt Priority high bit.** PPCH PPCL Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
5	PT2H	**Timer 2 overflow interrupt Priority High bit** PT2H PT2L Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
4	PSH	**Serial port Priority High bit** PSH PSL Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
3	PT1H	**Timer 1 overflow interrupt Priority High bit** PT1H PT1L Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
2	PX1H	**External interrupt 1 Priority High bit** PX1H PX1L Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
1	PT0H	**Timer 0 overflow interrupt Priority High bit** PT0H PT0L Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
0	PX0H	**External interrupt 0 Priority High bit** PX0H PX0L Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest

Reset Value = x000 0000b

Not bit addressable

Table 16-5. IEN1 Register

IEN1 - Interrupt Enable Register (B1h)

7	6	5	4	3	2	1	0
-	EUSB	-	-	-	ESPI	ETWI	EKB

Bit Number	Bit Mnemonic	Description
7	-	Reserved
6	EUSB	USB Interrupt Enable bit Cleared to disable USB interrupt. Set to enable USB interrupt.
5	-	Reserved
4	-	Reserved
3	-	Reserved
2	ESPI	**SPI interrupt Enable bit** Cleared to disable SPI interrupt. Set to enable SPI interrupt.
1	ETWI	**TWI interrupt Enable bit** Cleared to disable TWI interrupt. Set to enable TWI interrupt.
0	EKB	**Keyboard interrupt Enable bit** Cleared to disable keyboard interrupt. Set to enable keyboard interrupt.

Reset Value = x0xx x000b

Not bit addressable

Table 16-7. IPH1 Register

IPH1 - Interrupt Priority High Register (B3h)

7	6	5	4	3	2	1	0
-	PUSBH	-	-	-	PSPIH	PTWIH	PKBH

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	PUSBH	**USB Interrupt Priority High bit** PUSBH PUSBL Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	PSPIH	**SPI Interrupt Priority High bit** PSPIH PSPIL Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
1	PTWIH	**TWI Interrupt Priority High bit** PTWIH PTWIL Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
0	PKBH	**Keyboard Interrupt Priority High bit** PKBH PKBL Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest

Reset Value = X0XX X000b

Not bit addressable

16.3 Interrupt Sources and Vector Addresses

Table 16-8. Vector Table

Number	Polling Priority	Interrupt Source	Interrupt Request	Vector Address
0	0	Reset		0000h
1	1	INT0	IE0	0003h
2	2	Timer 0	TF0	000Bh
3	3	INT1	IE1	0013h
4	4	Timer 1	IF1	001Bh
5	6	UART	RI+TI	0023h
6	7	Timer 2	TF2+EXF2	002Bh
7	5	PCA	CF + CCFn (n = 0-4)	0033h
8	8	Keyboard	KBDIT	003Bh
9	9	TWI	TWIIT	0043h
10	10	SPI	SPIIT	004Bh
11	11			0053h
12	12			005Bh
13	13			0063h
14	14	USB	UEPINT + USBINT	006Bh
15	15			0073h

Table 17-2. KBE Register

KBE - Keyboard Input Enable Register (9Dh)

7	6	5	4	3	2	1	0
KBE7	KBE6	KBE5	KBE4	KBE3	KBE2	KBE1	KBE0

Bit Number	Bit Mnemonic	Description
7	KBE7	**Keyboard line 7 Enable bit** Cleared to enable standard I/O pin. Set to enable KBF.7 bit in KBF register to generate an interrupt request.
6	KBE6	**Keyboard line 6 Enable bit** Cleared to enable standard I/O pin. Set to enable KBF.6 bit in KBF register to generate an interrupt request.
5	KBE5	**Keyboard line 5 Enable bit** Cleared to enable standard I/O pin. Set to enable KBF.5 bit in KBF register to generate an interrupt request.
4	KBE4	**Keyboard line 4 Enable bit** Cleared to enable standard I/O pin. Set to enable KBF.4 bit in KBF register to generate an interrupt request.
3	KBE3	**Keyboard line 3 Enable bit** Cleared to enable standard I/O pin. Set to enable KBF.3 bit in KBF register to generate an interrupt request.
2	KBE2	**Keyboard line 2 Enable bit** Cleared to enable standard I/O pin. Set to enable KBF.2 bit in KBF register to generate an interrupt request.
1	KBE1	**Keyboard line 1 Enable bit** Cleared to enable standard I/O pin. Set to enable KBF.1 bit in KBF register to generate an interrupt request.
0	KBE0	**Keyboard line 0 Enable bit** Cleared to enable standard I/O pin. Set to enable KBF.0 bit in KBF register to generate an interrupt request.

Reset Value = 0000 0000b

Table 17-3. KBLS Register

KBLS-Keyboard Level Selector Register (9Ch)

7	6	5	4	3	2	1	0
KBLS7	**KBLS6**	**KBLS5**	**KBLS4**	**KBLS3**	**KBLS2**	**KBLS1**	**KBLS0**

Bit Number	Bit Mnemonic	Description
7	KBLS7	**Keyboard line 7 Level Selection bit** Cleared to enable a low level detection on Port line 7. Set to enable a high level detection on Port line 7.
6	KBLS6	**Keyboard line 6 Level Selection bit** Cleared to enable a low level detection on Port line 6. Set to enable a high level detection on Port line 6.
5	KBLS5	**Keyboard line 5 Level Selection bit** Cleared to enable a low level detection on Port line 5. Set to enable a high level detection on Port line 5.
4	KBLS4	**Keyboard line 4 Level Selection bit** Cleared to enable a low level detection on Port line 4. Set to enable a high level detection on Port line 4.
3	KBLS3	**Keyboard line 3 Level Selection bit** Cleared to enable a low level detection on Port line 3. Set to enable a high level detection on Port line 3.
2	KBLS2	**Keyboard line 2 Level Selection bit** Cleared to enable a low level detection on Port line 2. Set to enable a high level detection on Port line 2.
1	KBLS1	**Keyboard line 1 Level Selection bit** Cleared to enable a low level detection on Port line 1. Set to enable a high level detection on Port line 1.
0	KBLS0	**Keyboard line 0 Level Selection bit** Cleared to enable a low level detection on Port line 0. Set to enable a high level detection on Port line 0.

Reset Value = 0000 0000b

20.1 Description

The CPU interfaces to the 2-wire logic via the following four 8-bit special function registers: the Synchronous Serial Control register (SSCON; Table 20-10), the Synchronous Serial Data register (SSDAT; Table 20-11), the Synchronous Serial Control and Status register (SSCS; Table 20-12) and the Synchronous Serial Address register (SSADR Table 20-13).

SSCON is used to enable the TWI interface, to program the bit rate (see Table 20-3), to enable slave modes, to acknowledge or not a received data, to send a START or a STOP condition on the 2-wire bus, and to acknowledge a serial interrupt. A hardware reset disables the TWI module.

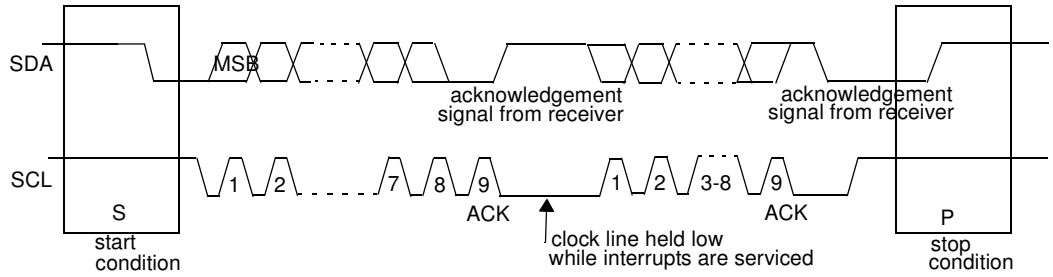
SSCS contains a status code which reflects the status of the 2-wire logic and the 2-wire bus. The three least significant bits are always zero. The five most significant bits contains the status code. There are 26 possible status codes. When SSCS contains F8h, no relevant state information is available and no serial interrupt is requested. A valid status code is available in SSCS one machine cycle after SI is set by hardware and is still present one machine cycle after SI has been reset by software. to Table 20-9. give the status for the master modes and miscellaneous states.

SSDAT contains a byte of serial data to be transmitted or a byte which has just been received. It is addressable while it is not in process of shifting a byte. This occurs when 2-wire logic is in a defined state and the serial interrupt flag is set. Data in SSDAT remains stable as long as SI is set. While data is being shifted out, data on the bus is simultaneously shifted in; SSDAT always contains the last byte present on the bus.

SSADR may be loaded with the 7-bit slave address (7 most significant bits) to which the TWI module will respond when programmed as a slave transmitter or receiver. The LSB is used to enable general call address (00h) recognition.

Figure 20-3 shows how a data transfer is accomplished on the 2-wire bus.

Figure 20-3. Complete Data Transfer on 2-wire Bus



The four operating modes are:

- Master Transmitter
- Master Receiver
- Slave transmitter
- Slave receiver

Data transfer in each mode of operation is shown in Table to Table 20-9 and Figure 20-4. to Figure 20-7.. These figures contain the following abbreviations:

S : START condition

address and the data direction bit (SLA+R). The serial interrupt flag SI must then be cleared before the serial transfer can continue.

When the slave address and the direction bit have been transmitted and an acknowledgement bit has been received, the serial interrupt flag is set again and a number of status code in SSCS are possible. There are 40h, 48h or 38h for the master mode and also 68h, 78h or B0h if the slave mode was enabled (AA=logic 1). The appropriate action to be taken for each of these status code is detailed in Table . This scheme is repeated until a STOP condition is transmitted.

SSIE, CR2, CR1 and CR0 are not affected by the serial transfer and are referred to Table 7 to Table 11. After a repeated START condition (state 10h) the TWI module may switch to the master transmitter mode by loading SSDAT with SLA+W.

20.1.3 Slave Receiver Mode

In the slave receiver mode, a number of data bytes are received from a master transmitter (Figure 20-6). To initiate the slave receiver mode, SSADR and SSCON must be loaded as follows:

Table 20-2. SSADR: Slave Receiver Mode Initialization

A6	A5	A4	A3	A2	A1	A0	GC
own slave address							

The upper 7 bits are the address to which the TWI module will respond when addressed by a master. If the LSB (GC) is set the TWI module will respond to the general call address (00h); otherwise it ignores the general call address.

Table 20-3. SSCON: Slave Receiver Mode Initialization

CR2	SSIE	STA	STO	SI	AA	CR1	CR0
bit rate	1	0	0	0	1	bit rate	bit rate

CR0, CR1 and CR2 have no effect in the slave mode. SSIE must be set to enable the TWI. The AA bit must be set to enable the own slave address or the general call address acknowledgement. STA, STO and SI must be cleared.

When SSADR and SSCON have been initialised, the TWI module waits until it is addressed by its own slave address followed by the data direction bit which must be at logic 0 (W) for the TWI to operate in the slave receiver mode. After its own slave address and the W bit have been received, the serial interrupt flag is set and a valid status code can be read from SSCS. This status code is used to vector to an interrupt service routine.The appropriate action to be taken for each of these status code is detailed in Table . The slave receiver mode may also be entered if arbitration is lost while TWI is in the master mode (states 68h and 78h).

If the AA bit is reset during a transfer, TWI module will return a not acknowledge (logic 1) to SDA after the next received data byte. While AA is reset, the TWI module does not respond to its own slave address. However, the 2-wire bus is still monitored and address recognition may be resume at any time by setting AA. This means that the AA bit may be used to temporarily isolate the module from the 2-wire bus.

Table 20-5. Status in Master Transmitter Mode

Status Code SSSTA	Status of the Two-wire Bus and Two-wire Hardware	Application software response					Next Action Taken by Two-wire Hardware
		To/From SSDAT	To SSCON				
			SSSTA	SSSTO	SSI	SSAA	
08h	A START condition has been transmitted	Write SLA+W	X	0	0	X	SLA+W will be transmitted.
10h	A repeated START condition has been transmitted	Write SLA+W	X	0	0	X	SLA+W will be transmitted.
		Write SLA+R	X	0	0	X	SLA+R will be transmitted. Logic will switch to master receiver mode
18h	SLA+W has been transmitted; ACK has been received	Write data byte	0	0	0	X	Data byte will be transmitted.
		No SSDAT action	1	0	0	X	Repeated START will be transmitted.
		No SSDAT action	0	1	0	X	STOP condition will be transmitted and SSSTO flag will be reset.
		No SSDAT action	1	1	0	X	STOP condition followed by a START condition will be transmitted and SSSTO flag will be reset.
20h	SLA+W has been transmitted; NOT ACK has been received	Write data byte	0	0	0	X	Data byte will be transmitted.
		No SSDAT action	1	0	0	X	Repeated START will be transmitted.
		No SSDAT action	0	1	0	X	STOP condition will be transmitted and SSSTO flag will be reset.
		No SSDAT action	1	1	0	X	STOP condition followed by a START condition will be transmitted and SSSTO flag will be reset.
28h	Data byte has been transmitted; ACK has been received	Write data byte	0	0	0	X	Data byte will be transmitted.
		No SSDAT action	1	0	0	X	Repeated START will be transmitted.
		No SSDAT action	0	1	0	X	STOP condition will be transmitted and SSSTO flag will be reset.
		No SSDAT action	1	1	0	X	STOP condition followed by a START condition will be transmitted and SSSTO flag will be reset.
30h	Data byte has been transmitted; NOT ACK has been received	Write data byte	0	0	0	X	Data byte will be transmitted.
		No SSDAT action	1	0	0	X	Repeated START will be transmitted.
		No SSDAT action	0	1	0	X	STOP condition will be transmitted and SSSTO flag will be reset.
		No SSDAT action	1	1	0	X	STOP condition followed by a START condition will be transmitted and SSSTO flag will be reset.
38h	Arbitration lost in SLA+W or data bytes	No SSDAT action	0	0	0	X	Two-wire bus will be released and not addressed slave mode will be entered.
		No SSDAT action	1	0	0	X	A START condition will be transmitted when the bus becomes free.

Table 20-8. Status in Slave Transmitter Mode (Continued)

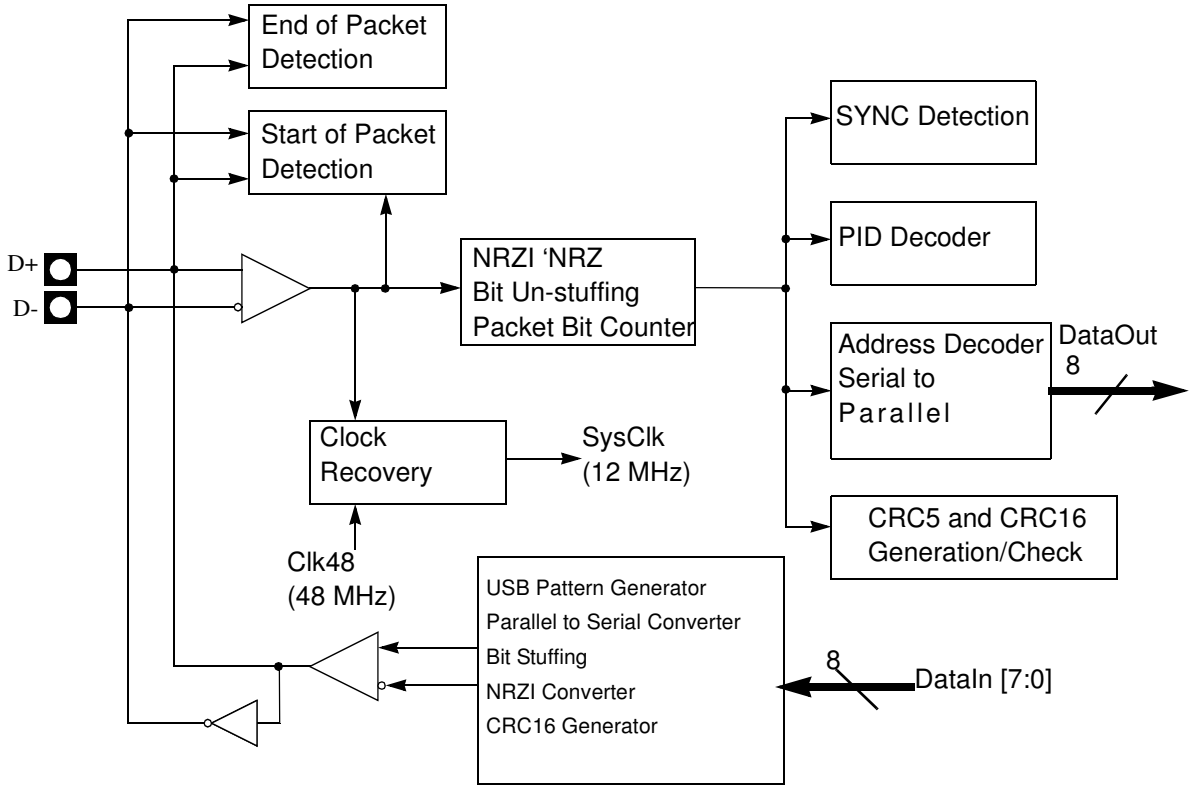
Status Code (SSCS)	Status of the 2-wire bus and 2-wire hardware	Application Software Response					Next Action Taken By 2-wire Software
		To/from SSDAT	To SSCON				
			STA	STO	SI	AA	
C0h	Data byte in SSDAT has been transmitted; NOT ACK has been received	No SSDAT action or	0	0	0	0	Switched to the not addressed slave mode; no recognition of own SLA or GCA
		No SSDAT action or	0	0	0	1	Switched to the not addressed slave mode; own SLA will be recognised; GCA will be recognised if GC=logic 1
		No SSDAT action or	1	0	0	0	Switched to the not addressed slave mode; no recognition of own SLA or GCA. A START condition will be transmitted when the bus becomes free
		No SSDAT action	1	0	0	1	Switched to the not addressed slave mode; own SLA will be recognised; GCA will be recognised if GC=logic 1. A START condition will be transmitted when the bus becomes free
C8h	Last data byte in SSDAT has been transmitted (AA=0); ACK has been received	No SSDAT action or	0	0	0	0	Switched to the not addressed slave mode; no recognition of own SLA or GCA
		No SSDAT action or	0	0	0	1	Switched to the not addressed slave mode; own SLA will be recognised; GCA will be recognised if GC=logic 1
		No SSDAT action or	1	0	0	0	Switched to the not addressed slave mode; no recognition of own SLA or GCA. A START condition will be transmitted when the bus becomes free
		No SSDAT action	1	0	0	1	Switched to the not addressed slave mode; own SLA will be recognised; GCA will be recognised if GC=logic 1. A START condition will be transmitted when the bus becomes free

Table 20-9. Miscellaneous Status

Status Code (SSCS)	Status of the 2-wire bus and 2-wire hardware	Application Software Response					Next Action Taken By 2-wire Software
		To/from SSDAT	To SSCON				
			STA	STO	SI	AA	
F8h	No relevant state information available; SI= 0	No SSDAT action	No SSCON action				Wait or proceed current transfer
00h	Bus error due to an illegal START or STOP condition	No SSDAT action	0	1	0	X	Only the internal hardware is affected, no STOP condition is sent on the bus. In all cases, the bus is released and STO is reset.

- Address checking.
- Clock generation (via DPLL).

Figure 21-2. SIE Block Diagram



21.1.2 Function Interface Unit (FIU)

The Function Interface Unit provides the interface between the AT89C5131 and the SIE. It manages transactions at the packet level with minimal intervention from the device firmware, which reads and writes the endpoint FIFOs.

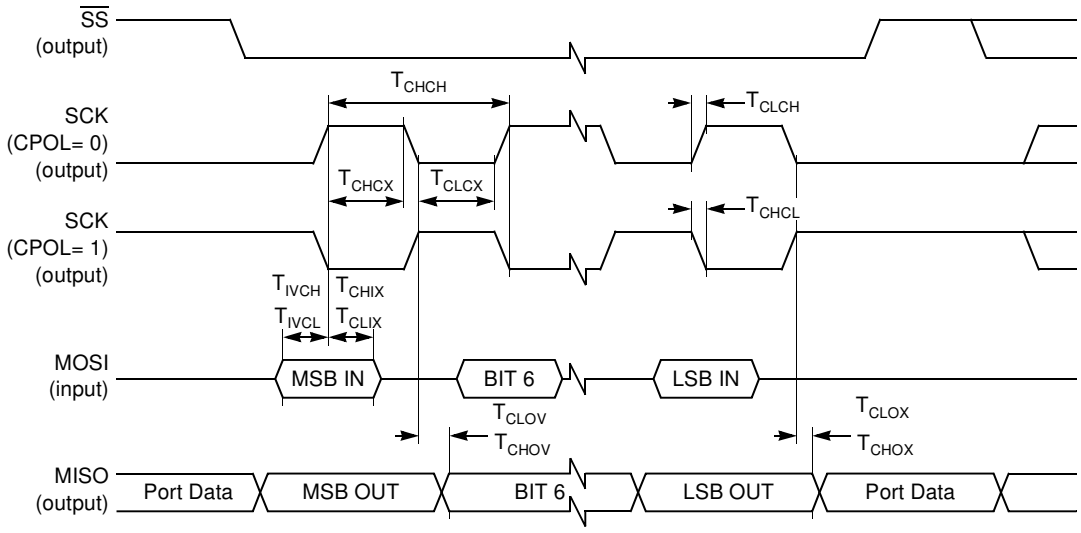
Table 21-14. UEPINT Register
UEPINT (S:F8h read-only)
USB Endpoint Interrupt Register

7	6	5	4	3	2	1	0
-	-	EP5INT	EP4INT	EP3INT	EP2INT	EP1INT	EP0INT

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is always 0. Do not set this bit.
6	-	**Reserved** The value read from this bit is always 0. Do not set this bit.
5	EP5INT	Endpoint 5 Interrupt This bit is set by hardware when an endpoint interrupt source has been detected on the endpoint 5. The endpoint interrupt sources are in the UEPSTAX register and can be: TXCMP, RXOUTB0, RXOUTB1, RXSETUP or STLCRC. A USB interrupt is triggered when the EP5IE bit in the UEPIEN register is set. This bit is cleared by hardware when all the endpoint interrupt sources are cleared
4	EP4INT	Endpoint 4 Interrupt This bit is set by hardware when an endpoint interrupt source has been detected on the endpoint 4. The endpoint interrupt sources are in the UEPSTAX register and can be: TXCMP, RXOUTB0, RXOUTB1, RXSETUP or STLCRC. A USB interrupt is triggered when the EP4IE bit in the UEPIEN register is set. This bit is cleared by hardware when all the endpoint interrupt sources are cleared
3	EP3INT	Endpoint 3 Interrupt This bit is set by hardware when an endpoint interrupt source has been detected on the endpoint 3. The endpoint interrupt sources are in the UEPSTAX register and can be: TXCMP, RXOUTB0, RXOUTB1, RXSETUP or STLCRC. A USB interrupt is triggered when the EP3IE bit in the UEPIEN register is set. This bit is cleared by hardware when all the endpoint interrupt sources are cleared
2	EP2INT	Endpoint 2 Interrupt This bit is set by hardware when an endpoint interrupt source has been detected on the endpoint 2. The endpoint interrupt sources are in the UEPSTAX register and can be: TXCMP, RXOUTB0, RXOUTB1, RXSETUP or STLCRC. A USB interrupt is triggered when the EP2IE bit in the UEPIEN register is set. This bit is cleared by hardware when all the endpoint interrupt sources are cleared
1	EP1INT	Endpoint 1 Interrupt This bit is set by hardware when an endpoint interrupt source has been detected on the endpoint 1. The endpoint interrupt sources are in the UEPSTAX register and can be: TXCMP, RXOUTB0, RXOUTB1, RXSETUP or STLCRC. A USB interrupt is triggered when the EP1IE bit in the UEPIEN register is set. This bit is cleared by hardware when all the endpoint interrupt sources are cleared
0	EP0INT	Endpoint 0 Interrupt This bit is set by hardware when an endpoint interrupt source has been detected on the endpoint 0. The endpoint interrupt sources are in the UEPSTAX register and can be: TXCMP, RXOUTB0, RXOUTB1, RXSETUP or STLCRC. A USB interrupt is triggered when the EP0IE bit in the UEPIEN register is set. This bit is cleared by hardware when all the endpoint interrupt sources are cleared

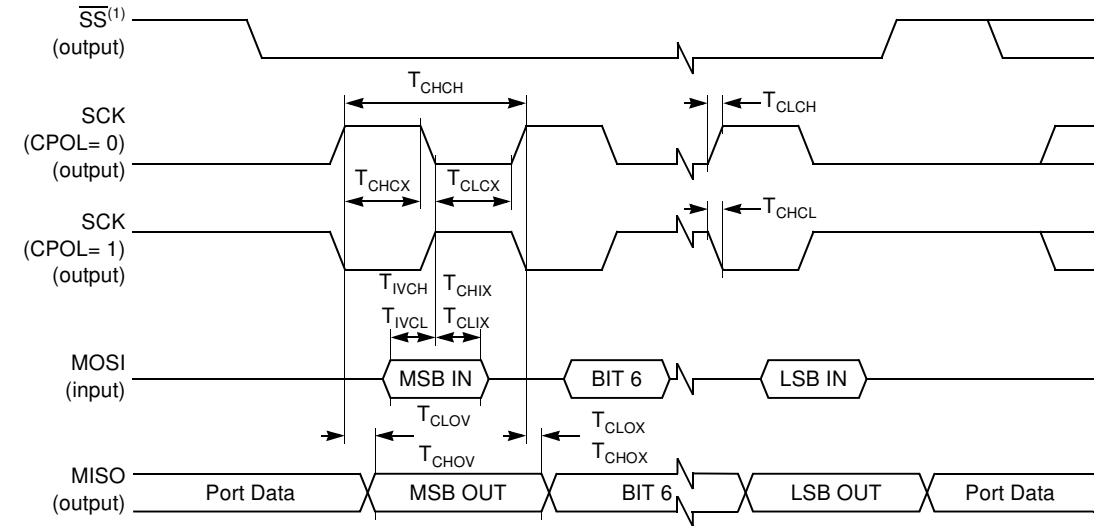
Reset Value = 00h

Figure 27-7. SPI Master Waveforms (SSCPHA= 0)



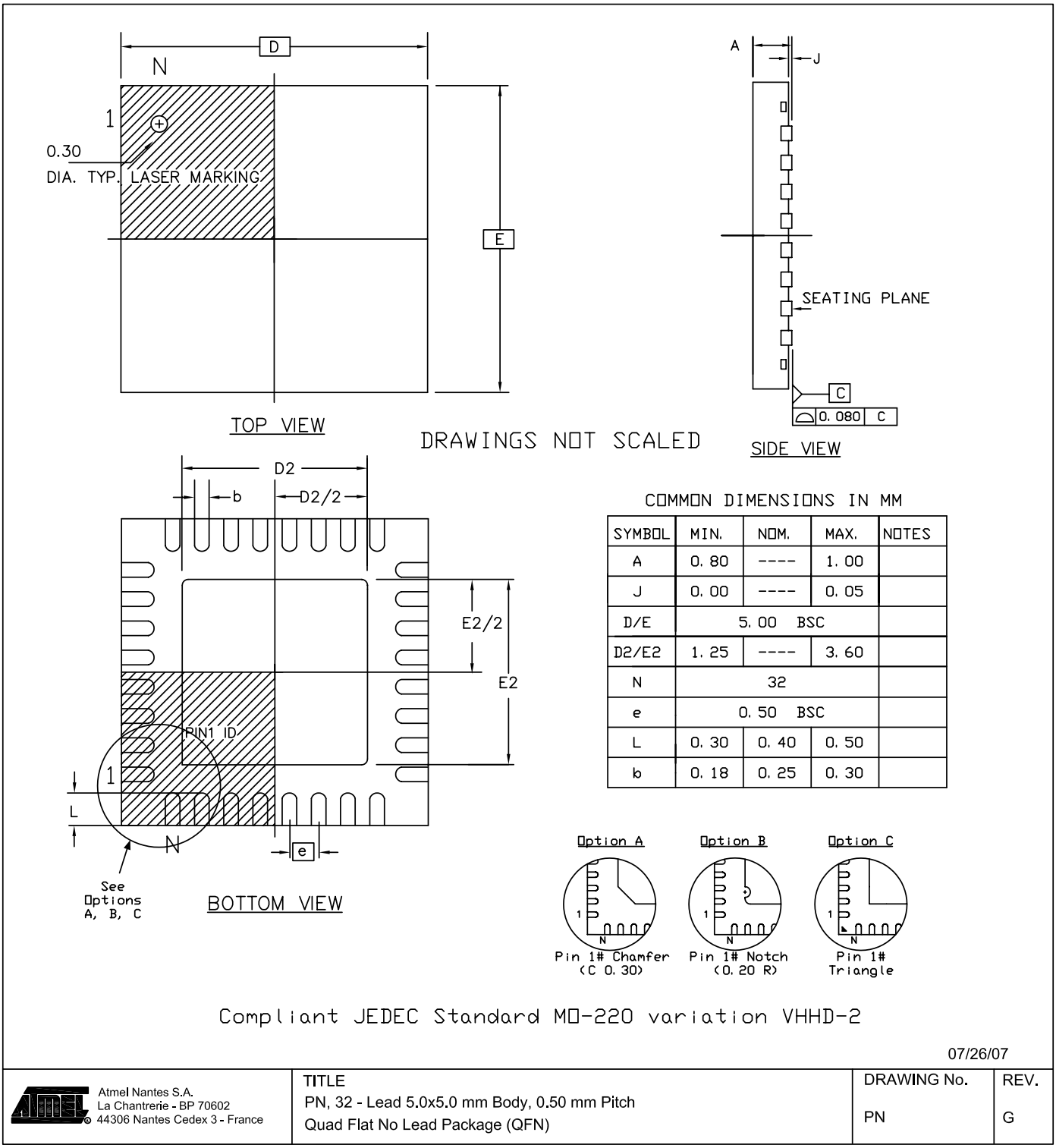
Note: 1. $\overline{SS}$ handled by software using general purpose port pin.

Figure 27-8. SPI Master Waveforms (SSCPHA= 1)



$\overline{SS}$ handled by software using general purpose port pin.

29.4 QFN32



SYMBOL	MIN.	NOM.	MAX.	NOTES
A	0.80	----	1.00	
J	0.00	----	0.05	
D/E		5.00 BSC		
D2/E2	1.25	----	3.60	
N		32		
e		0.50 BSC		
L	0.30	0.40	0.50	
b	0.18	0.25	0.30	

Atmel Nantes S.A. La Chantrerie - BP 70602 44306 Nantes Cedex 3 - France	TITLE PN, 32 - Lead 5.0x5.0 mm Body, 0.50 mm Pitch Quad Flat No Lead Package (QFN)	DRAWING No. PN	REV. G

30. Document Revision History

30.1 Changes from Rev A. to Rev. B

1. Added QFN32 package.

30.2 Changes from Rev B. to Rev. C

1. Updated package drawings.