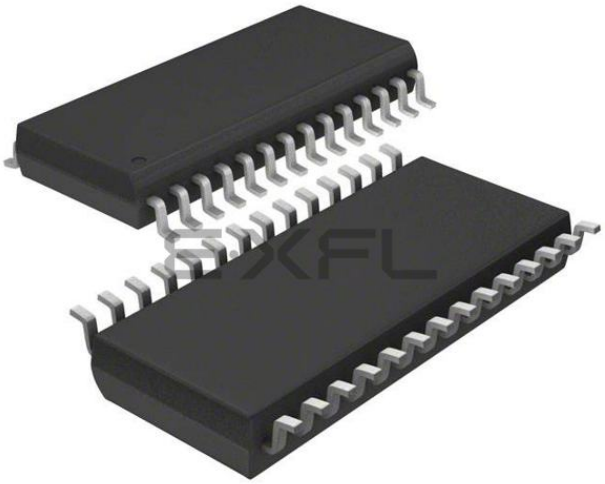

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	26
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 8x14b; D/A 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c23433-24pvxi

PSoC Functional Overview

The PSoC family consists of many programmable system-on-chips with on-chip controller devices. These devices are designed to replace multiple traditional MCU-based system components with a low-cost single-chip programmable device. PSoC devices include configurable blocks of analog and digital logic, and programmable interconnects. This architecture make it possible for you to create customized peripheral configurations that match the requirements of each individual application. additionally, a fast central processing unit (CPU), flash memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts and packages.

The PSoC architecture, as shown in the Logic Block Diagram on page 1, consists of four main areas: PSoC core, digital system, analog system, and system resources. Configurable global busing allows combining all of the device resources into a complete custom system. The PSoC CY8C23x33 family can have up to three I/O ports that connect to the global digital and analog interconnects, providing access to four digital blocks and four analog blocks.

PSoC Core

The PSoC core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable general Purpose I/O (GPIO)

The M8C CPU core is a powerful processor with speeds up to 24 MHz, providing a four million instructions per second MIPS 8-bit Harvard-architecture microprocessor. The CPU uses an interrupt controller with 11 vectors, to simplify programming of real time embedded events. program execution is timed and protected using the included sleep and watch dog timers (WDT).

Memory encompasses 8 KB of flash for program storage, 256 bytes of SRAM for data storage, and up to 2 KB of EEPROM emulated using the flash. Program flash uses four protection levels on blocks of 64 bytes, allowing customized software IP protection.

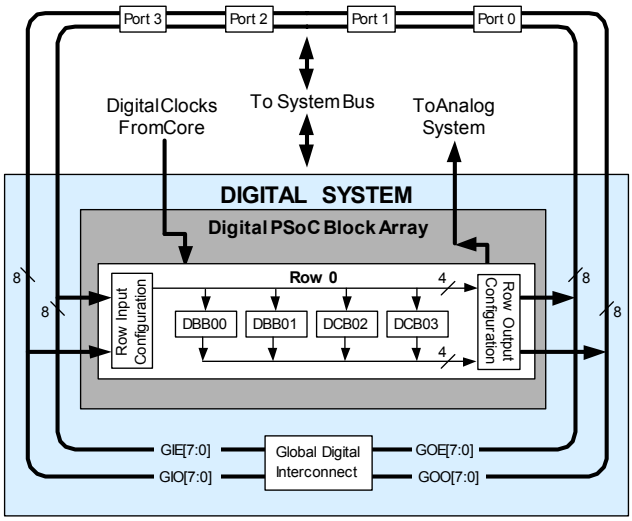
The PSoC device incorporates flexible internal clock generators, including a 24 MHz internal main oscillator (IMO) accurate to ±5% [2] over temperature and voltage. The 24 MHz IMO can also be doubled to 48 MHz for use by the digital system. A low power 32 kHz internal low speed oscillator (ILO) is provided for the sleep timer and WDT. If crystal accuracy is desired, the ECO (32.768 kHz external crystal oscillator) is available for use as a real time clock (RTC) and can optionally generate a crystal-accurate 24 MHz system clock using a PLL. The clocks, together with programmable clock dividers (as a system resource), provide the flexibility to integrate almost any timing requirement into the PSoC device.

PSoC GPIOs provide connection to the CPU, digital and analog resources of the device. Each pin's drive mode may be selected from eight options, allowing great flexibility in external interfacing. Every pin also has the capability to generate a system interrupt on high level, low level, and change from last read.

Digital System

The Digital system consists of 4 digital PSoC blocks. Each block is an 8-bit resource that is used alone or combined with other blocks to form 8, 16, 24, and 32-bit peripherals, which are called user module references.

Figure 1. Digital System Block Diagram



Digital peripheral configurations are:

- PWMs (8-and 16-bit)
- PWMs with Dead band (8- and 16-bit)
- Counters (8- to 32- bit)
- Timers (8- to 32- bit)
- UART 8 bit with selectable parity (up to 1)
- Serial peripheral interface (SPI) master and slave (up to 1)
- I^2C slave and multi master (1 available as a system resource)
- Cyclical redundancy checker (CRC)/Generator (8 to 32 bit)
- IrDA (up to 1)
- Pseudo Random Sequence Generators (8- to 32- bit)

The digital blocks can be connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also allow for signal multiplexing and for performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Digital blocks are provided in rows of four, where the number of blocks varies by PSoC device family. This allows the optimum choice of system resources for your application. Family resources are shown in the table titled PSoC Device Characteristics on page 5.

Note
2. Errata: When the device is operated within 0 °C to 70 °C, the frequency tolerance is reduced to ±2.5%, but if operated at extreme temperature (below 0 °C or above 70 °C), frequency tolerance deviates from ±2.5% to ±5%. For more information, see Errata on page 50.

Analog System

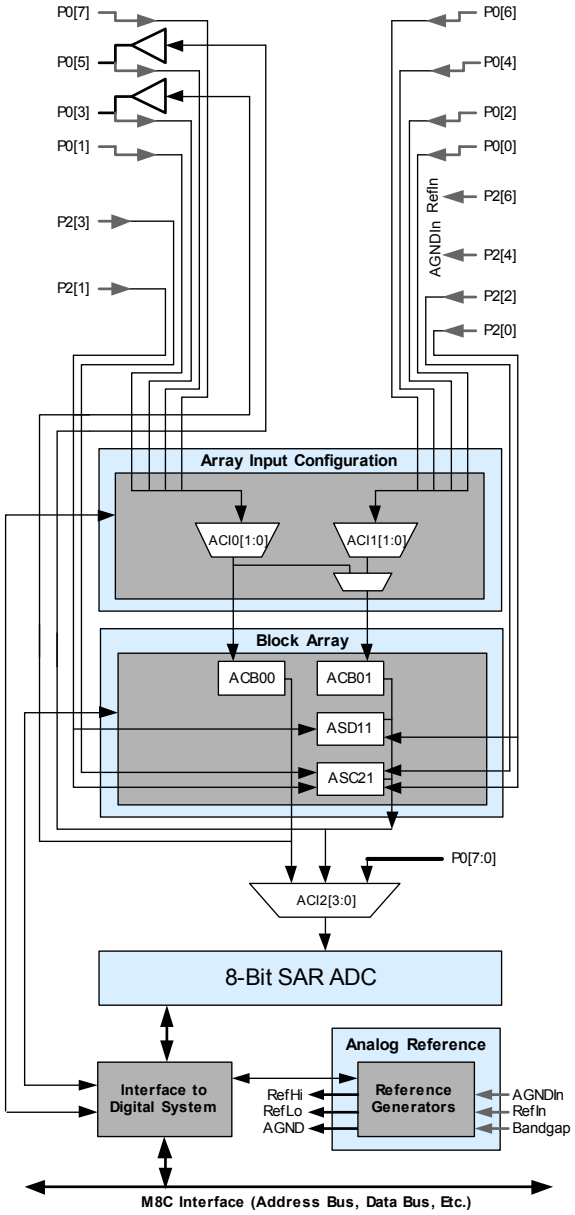
The analog system consists of an 8-bit SAR ADC and four configurable blocks. The programmable 8-bit SAR ADC is an optimized ADC that runs up to 300 Ksps, with monotonic guarantee. It also has the features to support a motor control application.

Each analog block consists of an opamp circuit allowing the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the more common PSoC analog functions (most available as user modules) are:

- Filters (2 band pass, low-pass)
- Amplifiers (up to 2, with selectable gain to 48x)
- Instrumentation amplifiers (1 with selectable gain to 93x)
- Comparators (1, with 16 selectable thresholds)
- DAC (6 or 9-bit DAC)
- Multiplying DAC (6 or 9-bit DAC)
- High current output drivers (two with 30 mA drive)
- 1.3-V reference (as a system resource)
- DTMF dialer
- Modulators
- Correlators
- Peak detectors
- Many other topologies possible

Analog blocks are arranged in a column of three, which includes one continuous time (CT) and two switched capacitor (SC) blocks. The Analog column 0 contains the SAR8 ADC block rather than the standard SC blocks.

Figure 2. Analog System Block Diagram



Additional System Resources

System resources, some of which are listed in the previous sections, provide additional capability useful to complete systems. Additional resources include a multiplier, decimator, low voltage detection, and power-on-reset. Brief statements describing the merits of each system resource follow:

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks may be routed to both the digital and analog systems. Additional clocks can be generated using digital PSoC blocks as clock dividers.
- A multiply accumulate (MAC) provides a fast 8-bit multiplier with 32-bit accumulate, to assist in both general math and digital filters.
- The decimator provides a custom hardware filter for digital signal processing applications including the creation of delta sigma ADCs.
- The I^2C module provides 100- and 400-kHz communication over two wires. Slave, master, and multi-master modes are all supported.
- Low-Voltage detection interrupts can signal the application of falling voltage levels, while the advanced POR circuit eliminates the need for a system supervisor.
- An internal 1.3-V reference provides an absolute reference for the analog system, including ADCs and DACs.

PSoC Device Characteristics

Depending on the PSoC device characteristics, the digital and analog systems can have 16, 8, or 4 digital blocks and 12, 6, or 3 analog blocks. Table 1 lists the resources available for specific PSoC device groups.

Table 1. PSoC Device Characteristics

PSoC Part Number	Digital I/O	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size	SAR ADC
CY8C29x66	up to 64	4	16	up to 12	4	4	12	2 K	32 K	No
CY8C28xxx	up to 44	up to 3	up to 12	up to 44	up to 4	up to 6	up to 12 + 4[3]	1 K	16 K	Yes
CY8C27x43	up to 44	2	8	up to 12	4	4	12	256	16 K	No
CY8C24x94	up to 56	1	4	up to 48	2	2	6	1 K	16 K	No
CY8C24x23A	up to 24	1	4	up to 12	2	2	6	256	4 K	No
CY8C23x33	up to 26	1	4	up to 12	2	2	4	256	8 K	Yes
CY8C24x33	up to 26	1	4	up to 12	2	2	4	256	8 K	Yes
CY8C22x45	up to 38	2	8	up to 38	0	4	6[3]	1 K	16 K	No
CY8C21x45	up to 24	1	4	up to 24	0	4	6[3]	512	8 K	Yes
CY8C21x34	up to 28	1	4	up to 28	0	2	4[3]	512	8 K	No
CY8C21x23	up to 16	1	4	up to 8	0	2	4[3]	256	4 K	No
CY8C20x34	up to 28	0	0	up to 28	0	0	3[3,4]	512	8 K	No
CY8C20xx6	up to 36	0	0	up to 36	0	0	3[3,4]	up to 2 K	up to 32 K	No

Notes
3. Limited analog functionality.
4. Two analog blocks and one CapSense®.

Getting Started

The quickest way to understand PSoC silicon is to read this data sheet and then use the PSoC Designer integrated development environment (IDE). This data sheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications.

For in-depth information, along with detailed programming details, see the PSoC® Technical Reference Manual.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device data sheets on the web at http://www.cypress.com.

Application Notes

Cypress application notes are an excellent introduction to the wide variety of possible PSoC designs and can be found at http://www.cypress.com

Development Kits

PSoC Development Kits are available online from cypress at http://www.cypress.com and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops), which is available online at http://www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

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Technical Support

For assistance with technical issues, search KnowledgeBase articles and forums at http://www.cypress.com. If you cannot find an answer to your question, call technical support at 1-800-541-4736.

Register Reference

This section lists the registers of the CY8C23433 PSoC device by using mapping tables, in offset order.

Register Conventions

The register conventions specific to this section are listed in Table 4.

Table 4. Register Conventions

Convention	Description
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

Register Mapping Tables

The PSoC device has a total register address space of 512 bytes. The register space is referred to as I/O space and is divided into two banks Bank 0 and Bank 1. The XIO bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XIO bit is set to 1 the user is in Bank 1.

Note In the following register mapping tables, blank fields are reserved and must not be accessed.

Table 6. Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW		40			80			C0	
PRT0DM1	01	RW		41			81			C1	
PRT0IC0	02	RW		42			82			C2	
PRT0IC1	03	RW		43			83			C3	
PRT1DM0	04	RW		44		ASD11CR0	84	RW		C4	
PRT1DM1	05	RW		45		ASD11CR1	85	RW		C5	
PRT1IC0	06	RW		46		ASD11CR2	86	RW		C6	
PRT1IC1	07	RW		47		ASD11CR3	87	RW		C7	
PRT2DM0	08	RW		48			88			C8	
PRT2DM1	09	RW		49			89			C9	
PRT2IC0	0A	RW		4A			8A			CA	
PRT2IC1	0B	RW		4B			8B			CB	
PRT3DM0	0C	RW		4C			8C			CC	
PRT3DM1	0D	RW		4D			8D			CD	
PRT3IC0	0E	RW		4E			8E			CE	
PRT3IC1	0F	RW		4F			8F			CF	
	10			50			90		GDI_O_IN	D0	RW
	11			51			91		GDI_E_IN	D1	RW
	12			52			92		GDI_O_OU	D2	RW
	13			53			93		GDI_E_OU	D3	RW
	14			54		ASC21CR0	94	RW		D4	
	15			55		ASC21CR1	95	RW		D5	
	16			56		ASC21CR2	96	RW		D6	
	17			57		ASC21CR3	97	RW		D7	
	18			58			98			D8	
	19			59			99			D9	
	1A			5A			9A			DA	
	1B			5B			9B			DB	
	1C			5C			9C			DC	
	1D			5D			9D		OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBB00FN	20	RW	CLK_CR0	60	RW		A0		OSC_CR0	E0	RW
DBB00IN	21	RW	CLK_CR1	61	RW		A1		OSC_CR1	E1	RW
DBB00OU	22	RW	ABF_CR0	62	RW		A2		OSC_CR2	E2	RW
	23		AMD_CR0	63	RW		A3		VLT_CR	E3	RW
DBB01FN	24	RW		64			A4		VLT_CMP	E4	R
DBB01IN	25	RW		65			A5			E5	
DBB01OU	26	RW	AMD_CR1	66	RW		A6			E6	
	27		ALT_CR0	67	RW		A7			E7	
DCB02FN	28	RW		68		SARADC_TRS	A8	RW	IMO_TR	E8	W
DCB02IN	29	RW		69		SARADC_TRCL	A9	RW	ILO_TR	E9	W
DCB02OU	2A	RW		6A		SARADC_TRCH	AA	RW	BDG_TR	EA	RW
	2B			6B		SARADC_CR2	AB	#	ECO_TR	EB	W
DCB03FN	2C	RW	TMP_DR0	6C	RW	SARADC_LCR	AC	RW		EC	
DCB03IN	2D	RW	TMP_DR1	6D	RW		AD			ED	
DCB03OU	2E	RW	TMP_DR2	6E	RW		AE			EE	
	2F		TMP_DR3	6F	RW		AF			EF	
	30		ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
	31		ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
	32		ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34		ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
	35		ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
	36		ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACB01CR2 *	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA		FLS_PR1	FA	RW
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD			FD	
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Gray fields are reserved. # Access is bit specific.

DC Operational Amplifier Specifications

The following table lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40°C ≤ T_A ≤ 85°C, or 3.0 V to 3.6 V and –40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5 V and 3.3 V at 25°C and are for design guidance only.

The Operational amplifier is a component of both the analog continuous time PSoC blocks and the analog switched cap PSoC blocks. The guaranteed specifications are measured in the analog continuous time PSoC block. Typical parameters apply to 5 V at 25°C and are for design guidance only.

Table 11. 5-V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input offset voltage (absolute value) Power = low, Opamp bias = high Power = medium, Opamp bias = high Power = high, Opamp bias = high	 – – –	 1.6 1.3 1.2	 10 8 7.5	 mV mV mV	
TCV_{OSOA}	Average input offset voltage drift	–	7.0	35.0	µV/°C	
I_{EBOA}	Input leakage current (Port 0 analog pins)	–	20	–	pA	Gross tested to 1 µA
C_{INOA}	Input capacitance (Port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25°C
V_{CMOA}	Common mode voltage range Common mode voltage range (high power or high opamp bias)	0.0 0.5	– –	V_{DD} V_{DD} – 0.5	V V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
G_{OLOA}	Open loop gain Power = low, Opamp bias = high Power = medium, Opamp bias = high Power = high, Opamp bias = high	 60 60 80	 – – –	 – – –	 dB – –	Specification is applicable at high power. For all other bias modes (except high power, high opamp bias), minimum is 60 dB.
$V_{OHIGHOA}$	High output voltage swing (internal signals) Power = low, Opamp bias = high Power = medium, Opamp bias = high Power = high, Opamp bias = high	 V_{DD} – 0.2 V_{DD} – 0.2 V_{DD} – 0.5	 – – –	 – – –	 V V V	
V_{OLOWOA}	Low output voltage swing (internal signals) Power = low, Opamp bias = high Power = medium, Opamp bias = high Power = high, Opamp bias = high	 – – –	 – – –	 0.2 0.2 0.5	 V V V	
I_{SOA}	Supply current (including associated AGND buffer) Power = low, Opamp bias = high Power = medium, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = low Power = high, Opamp bias = high	 – – – – –	 300 600 1200 2400 4600	 400 800 1600 3200 6400	 µA µA µA µA µA	
$PSRR_{OA}$	Supply voltage rejection ratio	52	80	–	dB	V_{ss} ≤ VIN ≤ (V_{DD} - 2.25) or (V_{DD} - 1.25V) ≤ VIN ≤ V_{DD}

Table 12. 3.3-V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input offset voltage (absolute value) Power = low, Opamp bias = high Power = medium, Opamp bias = high Power = high, Opamp bias = high	 – – –	 1.65 1.32 –	 10 8 –	 mV mV mV	Power = high, Opamp bias = high setting is not allowed for 3.3 V V_{DD} operation.
TCV_{OSOA}	Average input offset voltage drift	–	7.0	35.0	µV/°C	
I_{EBOA}	Input leakage current (port 0 analog pins)	–	20	–	pA	Gross tested to 1 µA
C_{INOA}	Input capacitance (port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C
V_{CMOA}	Common mode voltage range	0.2	–	V_{DD} – 0.2	V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
G_{OLOA}	Open loop gain Power = low, ppamp Opamp bias = low Power = medium, Opamp bias = low Power = high, Opamp bias = low	 60 60 80	 – – –	 – – –	 dB dB dB	Specification is applicable at low Opamp bias. For high Opamp bias mode (except high power, high Opamp bias), minimum is 60 dB.
$V_{OHIGHOA}$	High output voltage swing (internal signals) Power = low, Opamp bias = low Power = medium, Opamp bias = low Power = high, Opamp bias = low	 V_{DD} – 0.2 V_{DD} – 0.2 V_{DD} – 0.2	 – – –	 – – –	 V V V	Power = high, Opamp bias = high setting is not allowed for 3.3 V V_{DD} operation.
V_{OLOWOA}	Low output voltage swing (internal signals) Power = low, ppamp Opamp bias = low Power = medium, Opamp bias = low Power = high, Opamp bias = low	 – – –	 – – –	 0.2 0.2 0.2	 V V V	Power = high, Opamp bias = high setting is not allowed for 3.3 V V_{DD} operation.
I_{SOA}	Supply current (including associated AGND buffer) Power = low, Opamp bias = low Power = low, Opamp bias = high Power = medium, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = low Power = high, Opamp bias = high	 – – – – – –	 150 300 600 1200 2400 –	 200 400 800 1600 3200 –	 mA mA mA mA mA mA	Power = high, Opamp bias = high setting is not allowed for 3.3 V V_{DD} operation.
$PSRR_{OA}$	Supply voltage rejection ratio	64	80	–	dB	V_{SS} £ V_{IN} £ (V_{DD} – 2.25) or (V_{DD} – 1.25 V) £ V_{IN} £ V_{DD}

DC Low-Power Comparator Specifications

The following table lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 13. DC Low-Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units
V_{REFLPC}	Low power comparator (LPC) reference voltage range	0.2	–	V_{DD} – 1.0	V
I_{SLPC}	LPC supply current	–	10	40	µA
V_{OSLPC}	LPC voltage offset	–	2.5	30	mV

Table 16. 5-V DC Analog Reference Specifications (continued)

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b110	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	2 × Bandgap	2.512	2.594	2.654	V
		V_{AGND}	AGND	Bandgap	1.250	1.303	1.346	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.011	V_{SS} + 0.027	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	2 × Bandgap	2.515	2.592	2.654	V
		V_{AGND}	AGND	Bandgap	1.253	1.301	1.340	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.006	V_{SS} + 0.02	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	2 × Bandgap	2.518	2.593	2.651	V
		V_{AGND}	AGND	Bandgap	1.254	1.301	1.338	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.004	V_{SS} + 0.017	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	2 × Bandgap	2.517	2.594	2.650	V
		V_{AGND}	AGND	Bandgap	1.255	1.300	1.337	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.003	V_{SS} + 0.015	V
0b111	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	3.2 × Bandgap	4.011	4.143	4.203	V
		V_{AGND}	AGND	1.6 × Bandgap	2.020	2.075	2.118	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.011	V_{SS} + 0.026	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	3.2 × Bandgap	4.022	4.138	4.203	V
		V_{AGND}	AGND	1.6 × Bandgap	2.023	2.075	2.114	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.006	V_{SS} + 0.017	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	3.2 × Bandgap	4.026	4.141	4.207	V
		V_{AGND}	AGND	1.6 × Bandgap	2.024	2.075	2.114	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.004	V_{SS} + 0.015	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	3.2 × Bandgap	4.030	4.143	4.206	V
		V_{AGND}	AGND	1.6 × Bandgap	2.024	2.076	2.112	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.003	V_{SS} + 0.013	V

Table 17. 3.3-V DC Analog Reference Specifications

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b000	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.170	$V_{DD}/2$ + 1.288	$V_{DD}/2$ + 1.376	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.098	$V_{DD}/2$ + 0.003	$V_{DD}/2$ + 0.097	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.386	$V_{DD}/2$ – 1.287	$V_{DD}/2$ – 1.169	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.210	$V_{DD}/2$ + 1.290	$V_{DD}/2$ + 1.355	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.055	$V_{DD}/2$ + 0.001	$V_{DD}/2$ + 0.054	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.359	$V_{DD}/2$ – 1.292	$V_{DD}/2$ – 1.214	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.198	$V_{DD}/2$ + 1.292	$V_{DD}/2$ + 1.368	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.041	$V_{DD}/2$	$V_{DD}/2$ + 0.04	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.362	$V_{DD}/2$ – 1.295	$V_{DD}/2$ – 1.220	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.202	$V_{DD}/2$ + 1.292	$V_{DD}/2$ + 1.364	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.033	$V_{DD}/2$	$V_{DD}/2$ + 0.030	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.364	$V_{DD}/2$ – 1.297	$V_{DD}/2$ – 1.222	V
0b001	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.072	P2[4] + P2[6] – 0.017	P2[4] + P2[6] + 0.041	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.029	P2[4] – P2[6] + 0.010	P2[4] – P2[6] + 0.048	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.066	P2[4] + P2[6] – 0.010	P2[4] + P2[6] + 0.043	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.024	P2[4] – P2[6] + 0.004	P2[4] – P2[6] + 0.034	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.073	P2[4] + P2[6] – 0.007	P2[4] + P2[6] + 0.053	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.028	P2[4] – P2[6] + 0.002	P2[4] – P2[6] + 0.033	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.073	P2[4] + P2[6] – 0.006	P2[4] + P2[6] + 0.056	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.030	P2[4] – P2[6]	P2[4] – P2[6] + 0.032	V

Table 17. 3.3-V DC Analog Reference Specifications (continued)

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b110	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	2 × Bandgap	2.460	2.594	2.695	V
		V_{AGND}	AGND	Bandgap	1.257	1.302	1.335	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.01	V_{SS} + 0.029	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	2 × Bandgap	2.462	2.592	2.692	V
		V_{AGND}	AGND	Bandgap	1.256	1.301	1.332	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.005	V_{SS} + 0.017	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	2 × Bandgap	2.473	2.593	2.682	V
		V_{AGND}	AGND	Bandgap	1.257	1.301	1.330	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.003	V_{SS} + 0.014	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	2 × Bandgap	2.470	2.594	2.685	V
		V_{AGND}	AGND	Bandgap	1.256	1.300	1.332	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.002	V_{SS} + 0.012	V
0b111	All power settings Not allowed at 3.3 V	–	–	–	–	–	–	–

DC Analog PSoC Block Specifications

The following table lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and–40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 18. DC Analog PSoC Block Specifications

Symbol	Description	Min	Typ	Max	Units
R_{CT}	Resistor unit value (continuous time)	–	12.2	–	kΩ
C_{SC}	Capacitor unit value (switch cap)	–	80[9]	–	fF

DC POR and LVD Specifications

The following table lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Note The bits PORLEV and VM in the following table refer to bits in the VLT_CR register. See the *PSoC Mixed-Signal Array Technical Reference Manual* for more information on the VLT_CR register.

Table 19. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{PPOR1} V_{PPOR2}	V_{DD} value for PPOR trip PORLEV[1:0] = 01b PORLEV[1:0] = 10b	–	2.82 4.55	2.95 4.70	V V	V_{DD} must be greater than or equal to 2.5 V during startup or reset from watchdog.
V_{LVD1} V_{LVD2} V_{LVD3} V_{LVD4} V_{LVD5} V_{LVD6} V_{LVD7}	Vdd value for LVD trip VM[2:0] = 001b VM[2:0] = 010b VM[2:0] = 011b VM[2:0] = 100b VM[2:0] = 101b VM[2:0] = 110b VM[2:0] = 111b	2.85 2.95 3.06 4.37 4.50 4.62 4.71	2.92 3.02 3.13 4.48 4.64 4.73 4.81	2.99[10] 3.09 3.20 4.55 4.75 4.83 4.95	V V V V V V V	

Notes
9. C_{SC} is a design guarantee parameter, not tested value
10. Always greater than 50 mV above V_{PPOR} (PORLEV=01) for falling supply.

DC Programming Specifications

The following table lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40°C ≤ T_A ≤ 85°C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25°C and are for design guidance only.

Table 20. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DDP}	V_{DD} for programming and erase	4.5	5	5.5	V	This specification applies to the functional requirements of external programmer tools
V_{DDLV}	Low V_{DD} for verify	3.0	3.1	3.2	V	This specification applies to the functional requirements of external programmer tools
V_{DDHV}	High V_{DD} for verify	5.1	5.2	5.3	V	This specification applies to the functional requirements of external programmer tools
$V_{DDIWRITE}$	Supply voltage for flash write operation	3.0	–	5.25	V	This specification applies to this device when it is executing internal flash writes
I_{DDP}	Supply current during programming or verify	–	5	25	mA	
V_{ILP}	Input low voltage during programming or verify	–	–	0.8	V	
V_{IHP}	Input high voltage during programming or verify	2.1	–	–	V	
I_{ILP}	Input current when applying vilp to P1[0] or P1[1] during programming or verify	–	–	0.2	mA	Driving internal pull down resistor
I_{IHP}	Input current when applying vihp to P1[0] or P1[1] during programming or verify	–	–	1.5	mA	Driving internal pull down resistor
V_{OLV}	Output low voltage during programming or verify	–	–	V_{SS} + 0.75	V	
V_{OHV}	Output high voltage during programming or verify	V_{DD} - 1.0	–	V_{DD}	V	
$Flash_{ENPB}$	Flash endurance (per block)	50,000	–	–	–	Erase/write cycles per block
$Flash_{ENT}$	Flash endurance (total)[11]	1,800,000	–	–	–	Erase/write cycles
$Flash_{DR}$	Flash data retention	10	–	–	Years	

DC I^2C Specifications

The following table lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85°C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25°C and are for design guidance only.

Table 21. DC I^2C Specifications[12]

Symbol	Description	Min	Typ	Max	Units	Notes
V_{ILI2C}	Input low level	–	–	0.3 × V_{DD}	V	3.0 V ≤ V_{DD} ≤ 3.6 V
		–	–	0.25 × V_{DD}	V	4.75 V ≤ V_{DD} ≤ 5.25 V
V_{IHI2C}	Input high level	0.7 × V_{DD}	–	–	V	3.0 V ≤ V_{DD} ≤ 5.25 V

Notes

11. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles). For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to 0xthe Flash APIs Application Note AN2015 at http://www.cypress.com under Application Notes for more information.
12. All GPIOs meet the DC GPIO V_{IL} and V_{IH} specifications found in the DC GPIO Specifications sections. The I^2C GPIO pins also meet the above specs.

SAR8 ADC DC Specifications

The following table lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40°C ≤ T_A ≤ 85°C, or 3.0 V to 3.6 V and –40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5 V and 3.3 V at 25°C and are for design guidance only.

Table 22. SAR8 ADC DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
$V_{ADCVREF}$	Reference voltage at pin P3[0] when configured as ADC reference voltage	3.0	–	5.25	V	The voltage level at P3[0] (when configured as ADC reference voltage) must always be maintained to be less than chip supply voltage level on V_{DD} pin. $V_{ADCVREF} < V_{DD}$.
$I_{ADCVREF}$	Current when P3[0] is configured as ADC V_{REF}	3	–	–	mA	
INL	Integral non-linearity	–1.5	–	+1.5	LSB	
INL (limited range)	Integral non-linearity accommodating a shift in the offset at 0x80	–1.2[12]	–	+1.2	LSB	The maximum LSB is over a sub-range not exceeding 1/16 of the full-scale range. 0x7F and 0x80 points specs are excluded here
DNL	Differential non-linearity	–2.3	–	+2.3	LSB	ADC conversion is monotonic over full range
DNL (limited range)	Differential non-linearity excluding 0x7F-0x80 transition	–1	–	+1	LSB	ADC conversion is monotonic over full range. 0x7F to 0x80 transition specs are excluded here.

Note

12. SAR converters require a stable input voltage during the sampling period. If the voltage into the SAR8 changes by more than 1 LSB during the sampling period then the accuracy specifications may not be met

AC GPIO Specifications

The following table lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40°C ≤ T_A ≤ 85°C, or 3.0 V to 3.6 V and –40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5 V and 3.3 V at 25°C and are for design guidance only.

Table 24. 5-V and 3.3-V AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO operating frequency	0	–	12.3	MHz	Normal strong mode
TRiseF	Rise time, normal strong mode, cload = 50 pF	3	–	18	ns	V_{DD} = 4.5 V to 5.25 V, 10% - 90%
TFallF	Fall time, normal strong mode, cload = 50 pF	2	–	18	ns	V_{DD} = 4.5 V to 5.25 V, 10% - 90%
TRiseS	Rise time, slow strong mode, cload = 50 pF	10	27	–	ns	V_{DD} = 3 V to 5.25 V, 10% - 90%
TFallS	Fall time, slow strong mode, cload = 50 pF	10	22	–	ns	V_{DD} = 3 V to 5.25 V, 10% - 90%

Figure 12. GPIO Timing Diagram

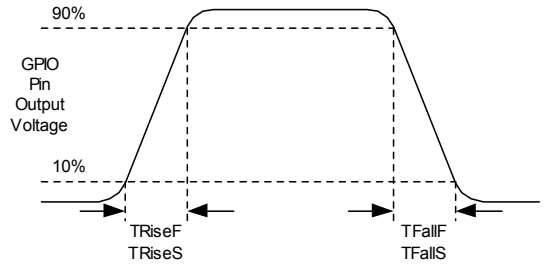
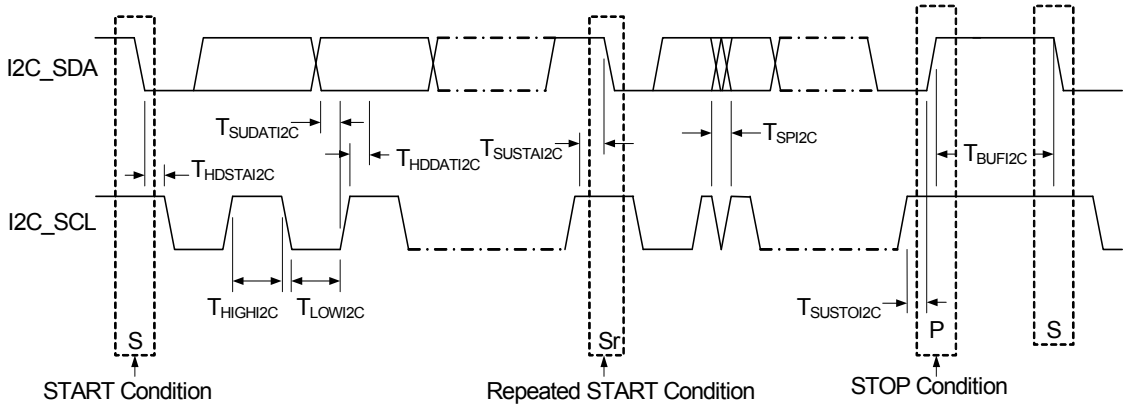


Table 36. AC Characteristics of the I²C SDA and SCL Pins for $V_{DD} < 3.0$ V (Fast Mode Not Supported)

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
F_{SCLI2C}	SCL clock frequency	0	100	–	–	kHz
$T_{HDSTAI2C}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4.0	–	–	–	µs
T_{LOWI2C}	LOW period of the SCL clock	4.7	–	–	–	µs
$T_{HIGHI2C}$	HIGH period of the SCL clock	4.0	–	–	–	µs
$T_{SUSTAI2C}$	Setup time for a repeated START condition	4.7	–	–	–	µs
$T_{HDDATI2C}$	Data hold time	0	–	–	–	µs
$T_{SUDATI2C}$	Data setup time	250	–	–	–	ns
$T_{SUSTOI2C}$	Setup time for STOP condition	4.0	–	–	–	µs
T_{BUFI2C}	Bus free time between a STOP and START condition	4.7	–	–	–	µs
T_{SPI2C}	Pulse width of spikes are suppressed by the input filter.	–	–	–	–	ns

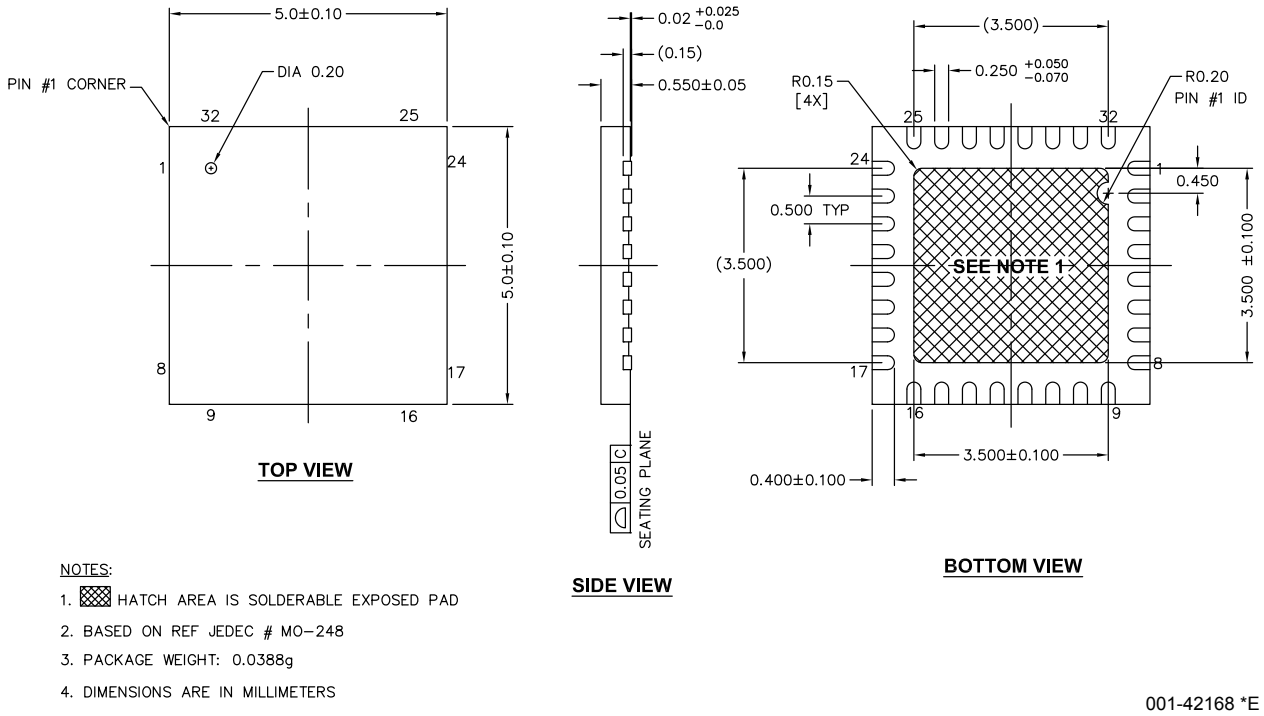
Figure 15. Definition for Timing for Fast/Standard Mode on the I²C Bus



Packaging Information

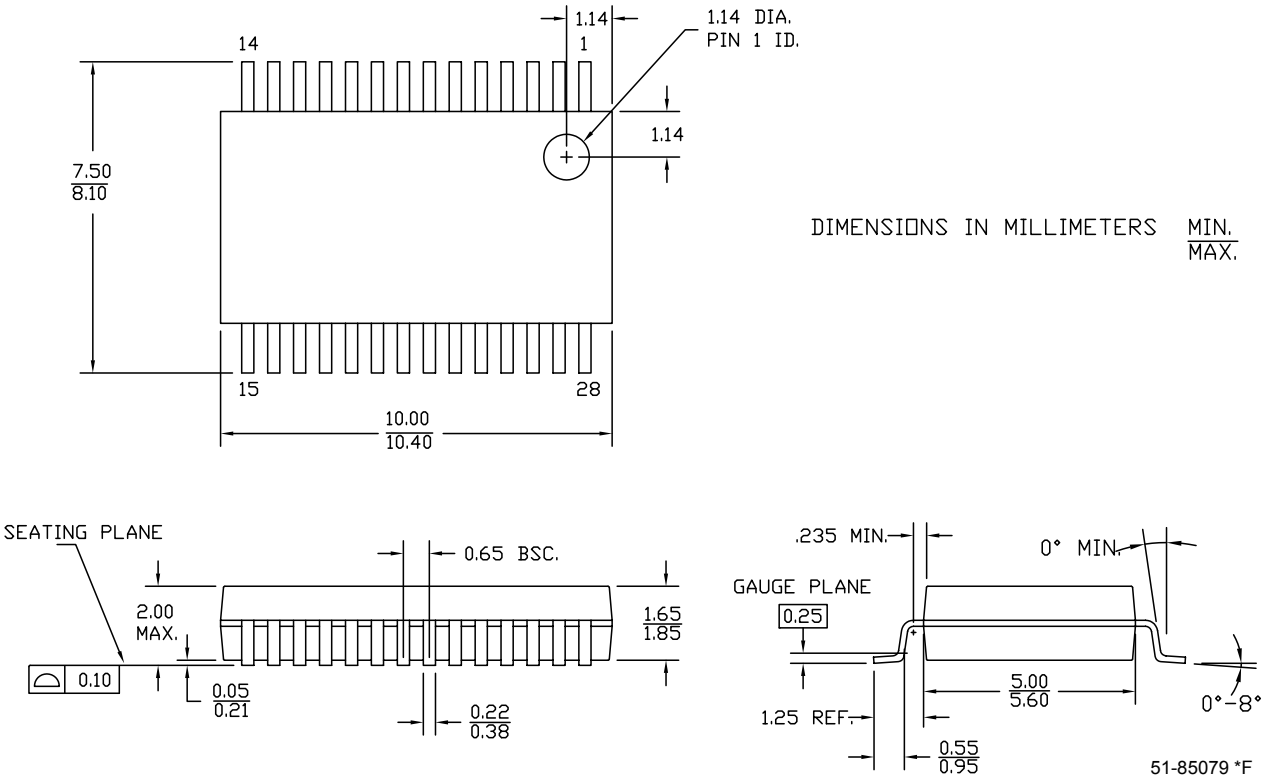
This section illustrates the packaging specifications for the CY8C23x33 PSoC device, along with the thermal impedances for each package, solder reflow peak temperature, and the typical package capacitance on crystal pins.

Figure 16. 32-Pin (5x5 mm) QFN



001-42168 *E

Figure 17. 28-Pin (210-Mil) SSOP



Thermal Impedances

Table 37. Thermal Impedances by Package

Package	Typical θ_{JA} [22]
32 QFN	19.4 °C/W
28 SSOP	95 °C/W

Capacitance on Crystal Pins

Table 38. Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
32 QFN	2.0 pF
28 SSOP	2.8 pF

Solder Reflow Peak Temperature

Following is the minimum solder reflow peak temperature to achieve good solderability.

Table 39. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Time at Maximum Peak Temperature
32 QFN	260 °C	30 s
28 SSOP	260 °C	30 s

Note
22. $T_J = T_A + POWER \times \theta_{JA}$.

Acronyms

Acronyms Used

Table 41 lists the acronyms that are used in this document.

Table 41. Acronyms Used in this Datasheet

Acronym	Description	Acronym	Description
AC	alternating current	MIPS	million instructions per second
ADC	analog-to-digital converter	PCB	printed circuit board
API	application programming interface	PGA	programmable gain amplifier
CPU	central processing unit	PLL	phase-locked loop
CRC	cyclic redundancy check	POR	power on reset
CT	continuous time	PPOR	precision power on reset
DAC	digital-to-analog converter	PRS	pseudo-random sequence
DC	direct current	PSoC®	Programmable System-on-Chip
DNL	differential nonlinearity	PWM	pulse width modulator
DTMF	dual-tone multi-frequency	QFN	quad flat no leads
ECO	external crystal oscillator	RTC	real time clock
EEPROM	electrically erasable programmable read-only memory	SAR	successive approximation
GPIO	general purpose I/O	SC	switched capacitor
ICE	in-circuit emulator	SLIMO	slow IMO
IDE	integrated development environment	SMP	switch mode pump
ILO	internal low speed oscillator	SOIC	small-outline integrated circuit
IMO	internal main oscillator	SPI™	serial peripheral interface
INL	integral nonlinearity	SRAM	static random access memory
I/O	input/output	SROM	supervisory read only memory
IrDA	infrared data association	SSOP	shrink small-outline package
ISSP	in-system serial programming	UART	universal asynchronous reciever / transmitter
LPC	low power comparator	USB	universal serial bus
LVD	low voltage detect	WDT	watchdog timer
MAC	multiply-accumulate	XRES	external reset
MCU	microcontroller unit		

Reference Documents

Design Aids – Reading and Writing PSoC® Flash – AN2015 (001-40459)

Glossary (continued)

port	A group of pins, usually eight.
power on reset (POR)	A circuit that forces the PSoC device to reset when the voltage is lower than a pre-set level. This is one type of hardware reset.
PSoC®	Cypress Semiconductor's PSoC® is a registered trademark and Programmable System-on-Chip™ is a trademark of Cypress.
PSoC Designer™	The software for Cypress' Programmable System-on-Chip technology.
pulse width modulator (PWM)	An output in the form of duty cycle which varies as a function of the applied measurand
RAM	An acronym for random access memory. A data-storage device from which data can be read out and new data can be written in.
register	A storage device with a specific capacity, such as a bit or byte.
reset	A means of bringing a system back to a know state. See hardware reset and software reset.
ROM	An acronym for read only memory. A data-storage device from which data can be read out, but new data cannot be written in.
serial	1. Pertaining to a process in which all events occur one after the other. 2. Pertaining to the sequential or consecutive occurrence of two or more related activities in a single device or channel.
settling time	The time it takes for an output signal or value to stabilize after the input has changed from one value to another.
shift register	A memory storage device that sequentially shifts a word either left or right to output a stream of serial data.
slave device	A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device.
SRAM	An acronym for static random access memory. A memory device allowing users to store and retrieve data at a high rate of speed. The term static is used because, after a value has been loaded into an SRAM cell, it remains unchanged until it is explicitly altered or until power is removed from the device.
SROM	An acronym for supervisory read only memory. The SROM holds code that is used to boot the device, calibrate circuitry, and perform Flash operations. The functions of the SROM may be accessed in normal user code, operating from Flash.
stop bit	A signal following a character or block that prepares the receiving device to receive the next character or block.
synchronous	1. A signal whose data is not acknowledged or acted upon until the next active edge of a clock signal. 2. A system whose operation is synchronized by a clock signal.

Document History Page

Document Title: CY8C23433, CY8C23533 PSoC® Programmable System-on-Chip™ Document Number: 001-44369				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2044848	KIY / AESA	01/30/2008	Data sheet creation
*A	2482967	HMI / AESA	05/14/2008	Moved from Preliminary to Final. Part number changed to CY8C23433, CY8C23533. Adjusted placement of the block diagram; updated description of DAC; updated package pinout description, updated POR and LVD spec, Added Csc , Flash Vdd, SAR ADC spec. Updated package diagram 001-42168 to *A. Updated data sheet template.
*B	2616862	OGNE / AESA	12/05/2008	Changed title to: “CY8C23433, CY8C23533 PSoC® Programmable System-on-Chip™” Updated package diagram 001-42168 to *C. Changed names of registers on page 11. "SARADC_C0" to "SARADC_CR0" "SARADC_C1" to "SARADC_CR1"
*C	2883928	JVY	02/24/2010	Updated the following parameters: DC_{ILO}, $SR_{POWERUP}$, F32K_U, F_{IMO6}, $T_{POWERUP}$, T_{ERASE_ALL}, $T_{PROGRAM\_HOT}$, $T_{PROGRAM\_COLD}$ Updated package diagrams Added Table of Contents
*D	3118801	NJF	12/23/10	Updated PSoC Device Characteristics table . Added DC I^2C Specifications table. Added Tjit_IMO specification, removed existing jitter specifications. Updated 3.3 V operational amplifier specifications and DC analog reference specifications tables. Updated Units of Measure, Acronyms, Glossary, and References sections. Updated solder reflow specifications. No specific changes were made to AC Digital Block Specifications table and I^2C Timing Diagram. They were updated for clearer understanding. Updated Figure 13 since the labelling for y-axis was incorrect. Added ordering code definitions.
*E	3283782	SHOB	08/16/11	Updated Getting Started, Development Tools and Designing with PSoC Designer. Updated Solder Reflow Peak Temperature Removed reference to obsolete Application Note AN2012.
*F	3598316	LURE / XZNG	04/24/2012	Changed the PWM description string from “8- to 32-bit” to “8- and 16-bit”.
*G	3993381	GVH	05/08/2013	Updated Packaging Information: spec 001-42168 – Changed revision from *D to *E. Updated Reference Documents (Removed 001-14503 spec related information). Added Errata.
*H		SEG		Corrected the units for R_{OUTOB} parameter.