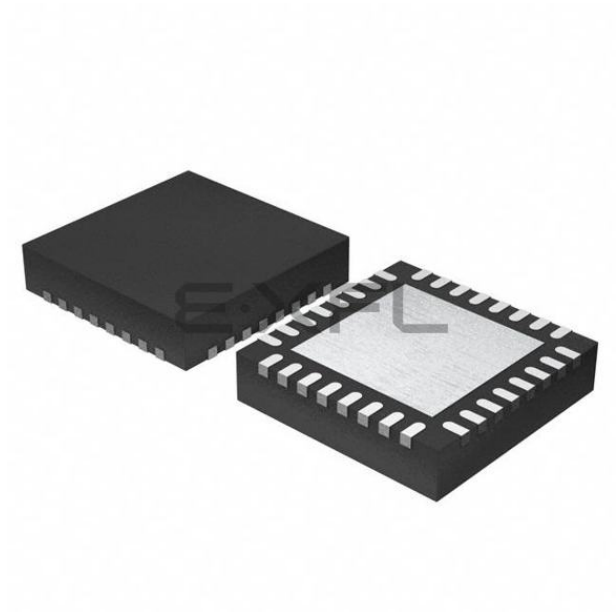

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	26
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 8x14b; D/A 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c23533-24lqxi

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Development Tools

PSoC Designer™ is the revolutionary integrated design environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
  - Hardware and software I^2C slaves and masters
  - Full-speed USB 2.0
  - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

PSoC Designer Software Subsystems

Design Entry

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are analog-to-digital converters (ADCs), digital-to-analog converters (DACs), amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this lets you to use more than 100 percent of PSoC's resources for an application.

Code Generation Tools

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

Assemblers. The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and are linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices.

The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow the designer to read and program and read and write data memory, and read and write I/O registers, read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows the designer to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an online support forum to aid the designer in getting started.

In-Circuit Emulator

A low cost, high functionality ICE is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24-MHz) operation.

Table 5. Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW		40			80			C0	
PRT0IE	01	RW		41			81			C1	
PRT0GS	02	RW		42			82			C2	
PRT0DM2	03	RW		43			83			C3	
PRT1DR	04	RW		44		ASD11CR0	84	RW		C4	
PRT1IE	05	RW		45		ASD11CR1	85	RW		C5	
PRT1GS	06	RW		46		ASD11CR2	86	RW		C6	
PRT1DM2	07	RW		47		ASD11CR3	87	RW		C7	
PRT2DR	08	RW		48			88			C8	
PRT2IE	09	RW		49			89			C9	
PRT2GS	0A	RW		4A			8A			CA	
PRT2DM2	0B	RW		4B			8B			CB	
PRT3DR	0C	RW		4C			8C			CC	
PRT3IE	0D	RW		4D			8D			CD	
PRT3GS	0E	RW		4E			8E			CE	
PRT3DM2	0F	RW		4F			8F			CF	
	10			50			90			D0	
	11			51			91			D1	
	12			52			92			D2	
	13			53			93			D3	
	14			54		ASC21CR0	94	RW		D4	
	15			55		ASC21CR1	95	RW		D5	
	16			56		ASC21CR2	96	RW	I2C_CFG	D6	RW
	17			57		ASC21CR3	97	RW	I2C_SCR	D7	#
	18			58			98		I2C_DR	D8	RW
	19			59			99		I2C_MSCR	D9	#
	1A			5A			9A		INT_CLR0	DA	RW
	1B			5B			9B		INT_CLR1	DB	RW
	1C			5C			9C			DC	
	1D			5D			9D		INT_CLR3	DD	RW
	1E			5E			9E		INT_MSK3	DE	RW
	1F			5F			9F			DF	
DBB00DR0	20	#	AMX_IN	60	RW		A0		INT_MSK0	E0	RW
DBB00DR1	21	W		61			A1		INT_MSK1	E1	RW
DBB00DR2	22	RW		62			A2		INT_VC	E2	RC
DBB00CR0	23	#	ARF_CR	63	RW		A3		RES_WDT	E3	W
DBB01DR0	24	#	CMP_CR0	64	#		A4		DEC_DH	E4	RC
DBB01DR1	25	W	ASY_CR	65	#		A5		DEC_DL	E5	RC
DBB01DR2	26	RW	CMP_CR1	66	RW		A6		DEC_CR0	E6	RW
DBB01CR0	27	#	SARADC_DL	67	RW		A7		DEC_CR1	E7	RW
DCB02DR0	28	#		68			A8		MUL0_X	E8	W
DCB02DR1	29	W	SARADC_CR0	69	#		A9		MUL0_Y	E9	W
DCB02DR2	2A	RW	SARADC_CR1	6A	RW		AA		MUL0_DH	EA	R
DCB02CR0	2B	#		6B			AB		MUL0_DL	EB	R
DCB03DR0	2C	#	TMP_DR0	6C	RW		AC		ACC0_DR1	EC	RW
DCB03DR1	2D	W	TMP_DR1	6D	RW		AD		ACC0_DR0	ED	RW
DCB03DR2	2E	RW	TMP_DR2	6E	RW		AE		ACC0_DR3	EE	RW
DCB03CR0	2F	#	TMP_DR3	6F	RW		AF		ACC0_DR2	EF	RW
	30		ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
	31		ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
	32		ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34		ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
	35		ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
	36		ACB01CR1 *	76	RW	RDI0RO1	B6	RW		F6	
	37		ACB01CR2 *	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA			FA	
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD			FD	
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Gray fields are reserved. # Access is bit specific.

Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C23433 PSoC device. For up-to-date latest electrical specifications, visit http://www.cypress.com.

Specifications are valid for –40°C ≤ T_A ≤ 85°C and T_J ≤ 100°C, except where noted.

Refer to Table 23 on page 30 for the electrical specifications for the IMO using SLIMO mode.

Figure 5. Voltage versus CPU Frequency

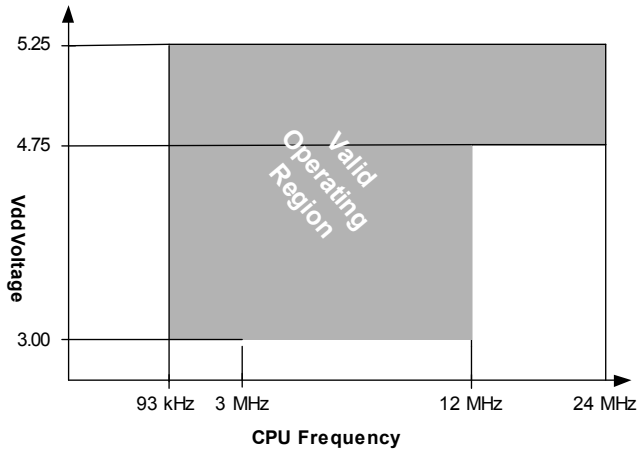
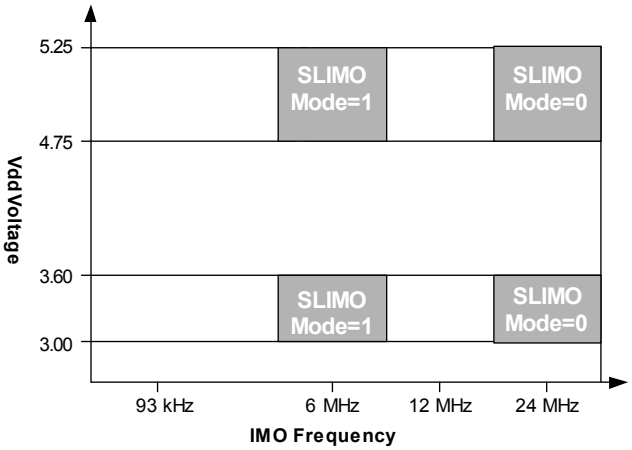


Figure 8. IMO Frequency Trim Options



Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 7. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage temperature	–55	25	+100	°C	Higher storage temperatures reduce data retention time. Recommended storage temperature is +25°C ± 25°C. Extended duration storage temperatures above 65°C degrade reliability.
$T_{BAKETEMP}$	Bake temperature	–	125	See package label	°C	
$T_{BAKETIME}$	Bake time	See package label	–	72	Hours	
T_A	Ambient temperature with power applied	–40	–	+85	°C	
Vdd	Supply voltage on V_{DD} relative to V_{SS}	–0.5	–	+6.0	V	
V_{IO}	DC input voltage	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
V_{IOZ}	DC voltage applied to tri-state	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
I_{MIO}	Maximum current into any port pin	–25	–	+50	mA	
ESD	Electrostatic discharge voltage	2000	–	–	V	Human Body Model ESD.
LU	Latch-up current	–	–	200	mA	

Operating Temperature

Table 8. Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T_A	Ambient temperature	–40	–	+85	°C	
T_J	Junction temperature	–40	–	+100	°C	The temperature rise from ambient to junction is package specific. See Table 37 on page 41. You must limit the power consumption to comply with this requirement.

DC Analog Output buffer specifications

The following table lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40°C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 14. 5-V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
C_L	Load capacitance	–	–	200	pF	This specification applies to the external circuit that is being driven by the analog output buffer.
V_{OSOB}	Input offset voltage (absolute value)	–	3	12	mV	
TCV_{OSOB}	Average input offset voltage drift	–	+6	–	µV/°C	
V_{CMOB}	Common-mode input voltage range	0.5	–	V_{DD} – 1.0	V	
R_{OUTOB}	Output resistance Power = low Power = high	 – –	 1 1	 – –	 Ω Ω	
$V_{OHIGHOB}$	High output voltage swing (Load = 32 ohms to V_{DD}/2) Power = low Power = high	 0.5 x V_{DD} + 1.1 0.5 x V_{DD} + 1.1	 – –	 – –	 V V	
V_{OLOWOB}	Low output voltage swing (Load = 32 ohms to V_{DD}/2) Power = low Power = high	 – –	 – –	 0.5 x V_{DD} - 1.3 0.5 x V_{DD} - 1.3	 V V	
I_{SOB}	Supply current including bias cell (no load) Power = low Power = high	 – –	 1.1 2.6	 5.1 8.8	 mA mA	
$PSRR_{OB}$	Supply voltage rejection ratio	52	64	–	dB	V_{OUT} >(V_{DD} - 1.25)

Table 15. 3.3-V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
C_L	Load capacitance	–	–	200	pF	This specification applies to the external circuit that is being driven by the analog output buffer.
V_{OSOB}	Input offset voltage (absolute value)	–	3	12	mV	
TCV_{OSOB}	Average input offset voltage drift	–	+6	–	µV/°C	
V_{CMOB}	Common-mode input voltage range	0.5	–	V_{DD} – 1.0	V	
R_{OUTOB}	Output resistance Power = low Power = high	 – –	 1 1	 – –	 Ω Ω	
$V_{OHIGHOB}$	High output voltage swing (Load = 1k ohms to V_{DD}/2) Power = low Power = high	 0.5 x V_{DD} + 1.0 0.5 x V_{DD} + 1.0	 – –	 – –	 V V	
V_{OLOWOB}	Low output voltage swing (Load = 1k ohms to V_{DD}/2) Power = low Power = high	 – –	 – –	 0.5 x V_{DD} - 1.0 0.5 x V_{DD} - 1.0	 V V	
I_{SOB}	Supply current including bias cell (no load) Power = low Power = high	 –	 0.8 2.0	 2.0 4.3	 mA mA	
$PSRR_{OB}$	Supply voltage rejection ratio	52	64	–	dB	V_{OUT} > (V_{DD} - 1.25)

Table 16. 5-V DC Analog Reference Specifications (continued)

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b100	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.481 + P2[6]	2.569 + P2[6]	2.639 + P2[6]	V
		V_{AGND}	AGND	2 × Bandgap	2.511	2.590	2.658	V
		V_{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.515 – P2[6]	2.602 – P2[6]	2.654 – P2[6]	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.498 + P2[6]	2.579 + P2[6]	2.642 + P2[6]	V
		V_{AGND}	AGND	2 × Bandgap	2.518	2.592	2.652	V
		V_{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.513 – P2[6]	2.598 – P2[6]	2.650 – P2[6]	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.504 + P2[6]	2.583 + P2[6]	2.646 + P2[6]	V
		V_{AGND}	AGND	2 × Bandgap	2.521	2.592	2.650	V
		V_{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.513 – P2[6]	2.596 – P2[6]	2.649 – P2[6]	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	2 × Bandgap + P2[6] (P2[6] = 1.3 V)	2.505 + P2[6]	2.586 + P2[6]	2.648 + P2[6]	V
		V_{AGND}	AGND	2 × Bandgap	2.521	2.594	2.648	V
		V_{REFLO}	Ref Low	2 × Bandgap – P2[6] (P2[6] = 1.3 V)	2.513 – P2[6]	2.595 – P2[6]	2.648 – P2[6]	V
0b101	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	P2[4] + Bandgap (P2[4] = V_{DD}/2)	P2[4] + 1.228	P2[4] + 1.284	P2[4] + 1.332	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap (P2[4] = V_{DD}/2)	P2[4] – 1.358	P2[4] – 1.293	P2[4] – 1.226	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	P2[4] + Bandgap (P2[4] = V_{DD}/2)	P2[4] + 1.236	P2[4] + 1.289	P2[4] + 1.332	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap (P2[4] = V_{DD}/2)	P2[4] – 1.357	P2[4] – 1.297	P2[4] – 1.229	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	P2[4] + Bandgap (P2[4] = V_{DD}/2)	P2[4] + 1.237	P2[4] + 1.291	P2[4] + 1.337	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap (P2[4] = V_{DD}/2)	P2[4] – 1.356	P2[4] – 1.299	P2[4] – 1.232	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	P2[4] + Bandgap (P2[4] = V_{DD}/2)	P2[4] + 1.237	P2[4] + 1.292	P2[4] + 1.337	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap (P2[4] = V_{DD}/2)	P2[4] – 1.357	P2[4] – 1.300	P2[4] – 1.233	V

Table 17. 3.3-V DC Analog Reference Specifications

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b000	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.170	$V_{DD}/2$ + 1.288	$V_{DD}/2$ + 1.376	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.098	$V_{DD}/2$ + 0.003	$V_{DD}/2$ + 0.097	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.386	$V_{DD}/2$ – 1.287	$V_{DD}/2$ – 1.169	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.210	$V_{DD}/2$ + 1.290	$V_{DD}/2$ + 1.355	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.055	$V_{DD}/2$ + 0.001	$V_{DD}/2$ + 0.054	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.359	$V_{DD}/2$ – 1.292	$V_{DD}/2$ – 1.214	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.198	$V_{DD}/2$ + 1.292	$V_{DD}/2$ + 1.368	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.041	$V_{DD}/2$	$V_{DD}/2$ + 0.04	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.362	$V_{DD}/2$ – 1.295	$V_{DD}/2$ – 1.220	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.202	$V_{DD}/2$ + 1.292	$V_{DD}/2$ + 1.364	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.033	$V_{DD}/2$	$V_{DD}/2$ + 0.030	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.364	$V_{DD}/2$ – 1.297	$V_{DD}/2$ – 1.222	V
0b001	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.072	P2[4] + P2[6] – 0.017	P2[4] + P2[6] + 0.041	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.029	P2[4] – P2[6] + 0.010	P2[4] – P2[6] + 0.048	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.066	P2[4] + P2[6] – 0.010	P2[4] + P2[6] + 0.043	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.024	P2[4] – P2[6] + 0.004	P2[4] – P2[6] + 0.034	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.073	P2[4] + P2[6] – 0.007	P2[4] + P2[6] + 0.053	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.028	P2[4] – P2[6] + 0.002	P2[4] – P2[6] + 0.033	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.073	P2[4] + P2[6] – 0.006	P2[4] + P2[6] + 0.056	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.030	P2[4] – P2[6]	P2[4] – P2[6] + 0.032	V

Table 17. 3.3-V DC Analog Reference Specifications (continued)

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b010	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.102	V_{DD} – 0.003	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.040	$V_{DD}/2$ + 0.001	$V_{DD}/2$ + 0.039	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.005	V_{SS} + 0.020	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.082	V_{DD} – 0.002	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.031	$V_{DD}/2$	$V_{DD}/2$ + 0.028	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.003	V_{SS} + 0.015	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.083	V_{DD} – 0.002	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.032	$V_{DD}/2$ – 0.001	$V_{DD}/2$ + 0.029	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.002	V_{SS} + 0.014	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.081	V_{DD} – 0.002	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.033	$V_{DD}/2$ – 0.001	$V_{DD}/2$ + 0.029	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.002	V_{SS} + 0.013	V
0b011	All power settings Not allowed at 3.3 V	–	–	–	–	–	–	–
0b100	All power settings Not allowed at 3.3 V	–	–	–	–	–	–	–
0b101	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.211	P2[4] + 1.285	P2[4] + 1.348	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.354	P2[4] – 1.290	P2[4] – 1.197	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.209	P2[4] + 1.289	P2[4] + 1.353	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.352	P2[4] – 1.294	P2[4] – 1.222	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.218	P2[4] + 1.291	P2[4] + 1.351	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.351	P2[4] – 1.296	P2[4] – 1.224	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.215	P2[4] + 1.292	P2[4] + 1.354	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.352	P2[4] – 1.297	P2[4] – 1.227	V

Table 23. 5-V and 3.3-V AC Chip-Level Specifications (continued)

Symbol	Description	Min	Typ	Max	Units	Notes
SR_{POWER_UP}	Power supply slew rate	–	–	250	V/ms	V_{DD} slew rate during power up.
$T_{POWERUP}$	Time from end of POR to CPU executing code	–	16	100	ms	Power up from 0V. See the System Resets section of the PSoC technical reference manual.
t_{jit_IMO} [18]	24 MHz IMO cycle-to-cycle jitter (RMS)	–	200	700	ps	
	24 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	300	900	ps	N = 32
	24 MHz IMO period jitter (RMS)	–	100	400	ps	
t_{jit_PLL} [18]	24 MHz IMO cycle-to-cycle jitter (RMS)	–	200	800	ps	
	24 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	300	1200	ps	N = 32
	24 MHz IMO period jitter (RMS)	–	100	700	ps	

Figure 9. PLL Lock Timing Diagram

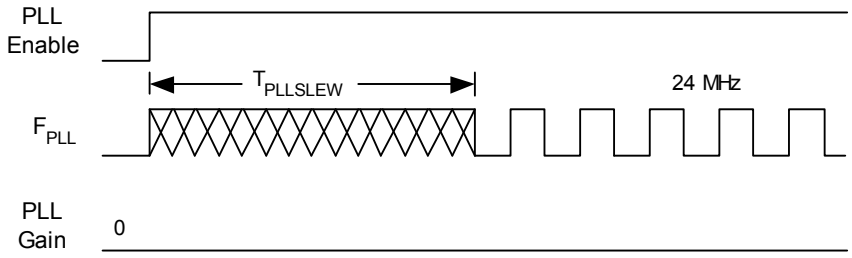


Figure 10. PLL Lock for Low Gain Setting Timing Diagram

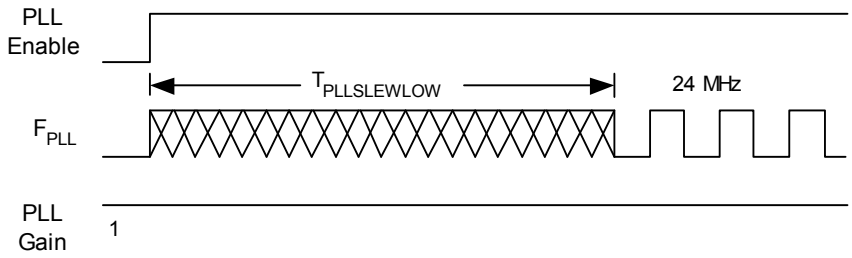
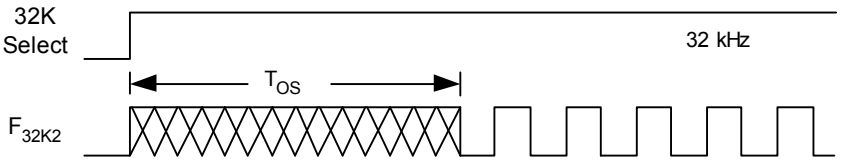


Figure 11. External Crystal Oscillator Startup Timing Diagram



AC Operational Amplifier Specifications

The following table lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40°C ≤ T_A ≤ 85°C, or 3.0 V to 3.6 V and –40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5 V and 3.3 V at 25°C and are for design guidance only.

Settling times, slew rates, and gain bandwidth are based on the analog continuous time PSoC block.

Power = high and Opamp bias = high is not supported at 3.3 V.

Table 25. 5-V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units
T_{ROA}	Rising settling time from 80% of ΔV to 0.1% of ΔV (10 pF load, unity gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = high	 – – –	 – – –	 3.9 0.72 0.62	 µs µs µs
T_{SOA}	Falling settling time from 20% of ΔV to 0.1% of ΔV (10 pF load, unity gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = high	 – – –	 – – –	 5.9 0.92 0.72	 µs µs µs
SR_{ROA}	Rising slew rate (20% to 80%)(10 pF load, unity gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = high	 0.15 1.7 6.5	 – – –	 – – –	 V/µs V/µs V/µs
SR_{FOA}	Falling slew rate (20% to 80%)(10 pF load, unity gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = high	 0.01 0.5 4.0	 – – –	 – – –	 V/µs V/µs V/µs
BW_{OA}	Gain bandwidth product Power = low, Opamp bias = low Power = medium, Opamp bias = high Power = high, Opamp bias = high	 0.75 3.1 5.4	 – – –	 – – –	 MHz MHz MHz

Table 26. 3.3-V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units
T_{ROA}	Rising settling time from 80% of ΔV to 0.1% of ΔV (10 pF load, unity gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high	 – –	 – –	 3.92 0.72	 µs µs
T_{SOA}	Falling settling time from 20% of ΔV to 0.1% of ΔV (10 pF load, unity gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high	 – –	 – –	 5.41 0.72	 µs µs
SR_{ROA}	Rising slew rate (20% to 80%)(10 pF load, unity gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high	 0.31 2.7	 – –	 – –	 V/µs V/µs
SR_{FOA}	Falling slew rate (20% to 80%)(10 pF load, unity gain) Power = low, Opamp bias = low Power = medium, Opamp bias = high	 0.24 1.8	 – –	 – –	 V/µs V/µs
BW_{OA}	Gain bandwidth product Power = low, Opamp bias = low Power = medium, Opamp bias = high	 0.67 2.8	 – –	 – –	 MHz MHz

AC Analog Output Buffer Specifications

The following table lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40°C ≤ T_A ≤ 85°C, or 3.0 V to 3.6 V and –40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5 V and 3.3 V at 25°C and are for design guidance only.

Table 29. 5-V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units
T_{ROB}	Rising settling time to 0.1%, 1 V step, 100 pF load Power = low Power = high	 – –	 – –	 2.5 2.5	 µs µs
T_{SOB}	Falling settling time to 0.1%, 1 V step, 100 pF load Power = low Power = high	 – –	 – –	 2.2 2.2	 µs µs
SR_{ROB}	Rising slew rate (20% to 80%), 1 V step, 100 pF load Power = low Power = high	 0.65 0.65	 – –	 – –	 V/µs V/µs
SR_{FOB}	Falling slew rate (80% to 20%), 1 V step, 100 pF load Power = low Power = high	 0.65 0.65	 – –	 – –	 V/µs V/µs
BW_{OB}	Small signal bandwidth, 20 mV_{pp}, 3 dB BW, 100 pF load Power = low Power = high	 0.8 0.8	 – –	 – –	 MHz MHz
BW_{OB}	Large signal bandwidth, 1 V_{pp}, 3 dB BW, 100 pF load Power = low Power = high	 300 300	 – –	 – –	 kHz kHz

Table 30. 3.3-V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units
T_{ROB}	Rising settling time to 0.1%, 1 V step, 100 pF load Power = low Power = high	 – –	 – –	 3.8 3.8	 µs µs
T_{SOB}	Falling settling time to 0.1%, 1 V step, 100 pF load Power = low Power = high	 – –	 – –	 2.6 2.6	 µs µs
SR_{ROB}	Rising slew rate (20% to 80%), 1 V step, 100 pF load Power = low Power = high	 0.5 0.5	 – –	 – –	 V/µs V/µs
SR_{FOB}	Falling slew rate (80% to 20%), 1 V step, 100 pF load Power = low Power = high	 0.5 0.5	 – –	 – –	 V/µs V/µs
BW_{OB}	Small signal bandwidth, 20 mV_{pp}, 3 dB BW, 100 pF load Power = low Power = high	 0.7 0.7	 – –	 – –	 MHz MHz
BW_{OB}	Large signal bandwidth, 1 V_{pp}, 3 dB BW, 100 pF load Power = low Power = high	 200 200	 – –	 – –	 kHz kHz

AC External Clock Specifications

The following table lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25°C and are for design guidance only.

Table 31. 5-V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units
F_{OSCEXT}	Frequency	0.093	–	24.6	MHz
–	High period	20.6	–	5300	ns
–	Low period	20.6	–	–	ns
–	Power up IMO to switch	150	–	–	µs

Table 32. 3.3-V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units
F_{OSCEXT}	Frequency with CPU clock divide by 1[20]	0.093	–	12.3	MHz
F_{OSCEXT}	Frequency with CPU clock divide by 2 or greater[21]	0.186	–	24.6	MHz
–	High period with CPU clock divide by 1	41.7	–	5300	ns
–	Low period with CPU clock divide by 1	41.7	–	–	ns
–	Power up IMO to switch	150	–	–	µs

AC Programming Specifications

The following table lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 33. AC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{RSCLK}	Rise time of SCLK	1	–	20	ns	
T_{FSCLK}	Fall time of SCLK	1	–	20	ns	
T_{SSCLK}	Data set up time to falling edge of SCLK	40	–	–	ns	
T_{HSCLK}	Data hold time from falling edge of SCLK	40	–	–	ns	
F_{SCLK}	Frequency of SCLK	0	–	8	MHz	
T_{ERASEB}	Flash erase time (block)	–	20	–	ms	
T_{WRITE}	Flash block write time	–	20	–	ms	
T_{DSCLK}	Data out delay from falling edge of SCLK	–	–	45	ns	$V_{DD} > 3.6$
T_{DSCLK3}	Data out delay from falling edge of SCLK	–	–	50	ns	$3.0 \le V_{DD} \le 3.6$
$T_{ERASEALL}$	Flash erase time (bulk)	–	80	–	ms	Erase all Blocks and protection fields at once
$T_{PROGRAM\_HOT}$	Flash block erase + Flash block write time	–	–	100[23]	ms	0 °C <= Tj <= 100°C
$T_{PROGRAM\_COLD}$	Flash block erase + Flash block write time	–	–	200[23]	ms	–40 °C <= Tj <= 0 °C

Notes

20. Maximum CPU frequency is 12 MHz at 3.3 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
21. If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met.
22. The max sample rate in this R2R ADC is 3.0/8=375KSPS
23. For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at http://www.cypress.com under Application Notes for more information.

SAR8 ADC AC Specifications

The following table lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25°C and are for design guidance only.

Table 34. SAR8 ADC AC Specifications[22]

Symbol	Description	Min	Typ	Max	Units
$Freq_3$	Input clock frequency 3 V	–	–	3.075	MHz
$Freq_5$	Input clock frequency 5 V	–	–	3.075	MHz

AC I^2C Specifications

The following table lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40°C ≤ T_A ≤ 85°C, or 3.0 V to 3.6 V and –40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5 V and 3.3 V at 25°C and are for design guidance only.

Table 35. AC Characteristics of the I^2C SDA and SCL Pins for V_{DD} > 3.0 V

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
F_{SCLI2C}	SCL clock frequency	0	100	0	400	kHz
$T_{HDSTAI2C}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	µs
T_{LOWI2C}	LOW period of the SCL clock	4.7	–	1.3	–	µs
$T_{HIGHI2C}$	HIGH period of the SCL clock	4.0	–	0.6	–	µs
$T_{SUSTAI2C}$	Setup time for a repeated START condition	4.7	–	0.6	–	µs
$T_{HDDATI2C}$	Data hold time	0	–	0	–	µs
$T_{SUDATI2C}$	Data setup time	250	–	100[24]	–	ns
$T_{SUSTOI2C}$	Setup Time for STOP condition	4.0	–	0.6	–	µs
T_{BUFI2C}	Bus free time between a STOP and START condition	4.7	–	1.3	–	µs
T_{SPI2C}	Pulse width of spikes are suppressed by the input filter.	–	–	0	50	ns

Note
24. A Fast-Mode I2C-bus device can be used in a Standard-Mode I2C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I2C-bus specification) before the SCL line is released.

Document Conventions

Units of Measure

Table 42 lists the unit sof measures.

Table 42. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
kB	1024 bytes	ms	millisecond
dB	decibels	ns	nanosecond
°C	degree Celsius	ps	picosecond
fF	femto farad	µV	microvolts
pF	picofarad	mV	millivolts
kHz	kilohertz	mVpp	millivolts peak-to-peak
MHz	megahertz	nV	nanovolts
LSB	least significant bit	V	volts
kΩ	kilohm	µW	microwatts
µA	microampere	W	watt
mA	milliampere	mm	millimeter
nA	nanoampere	ppm	parts per million
pA	pikoampere	%	percent
µs	microsecond		

Numeric Conventions

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’ or ‘b’ are decimals.

Glossary

active high	1. A logic signal having its asserted state as the logic 1 state. 2. A logic signal having the logic 1 state as the higher voltage of the two states.
analog blocks	The basic programmable opamp circuits. These are SC (switched capacitor) and CT (continuous time) blocks. These blocks can be interconnected to provide ADCs, DACs, multi-pole filters, gain stages, and much more.
analog-to-digital (ADC)	A device that changes an analog signal to a digital signal of corresponding magnitude. Typically, an ADC converts a voltage to a digital number. The digital-to-analog (DAC) converter performs the reverse operation.
API (Application Programming Interface)	A series of software routines that comprise an interface between a computer application and lower level services and functions (for example, user modules and libraries). APIs serve as building blocks for programmers that create software applications.
asynchronous	A signal whose data is acknowledged or acted upon immediately, irrespective of any clock signal.
Bandgap reference	A stable voltage reference design that matches the positive temperature coefficient of VT with the negative temperature coefficient of VBE, to produce a zero temperature coefficient (ideally) reference.
bandwidth	1. The frequency range of a message or information processing system measured in hertz. 2. The width of the spectral region over which an amplifier (or absorber) has substantial gain (or loss); it is sometimes represented more specifically as, for example, full width at half maximum.
bias	1. A systematic deviation of a value from a reference value. 2. The amount by which the average of a set of values departs from a reference value. 3. The electrical, mechanical, magnetic, or other force (field) applied to a device to establish a reference level to operate the device.
block	1. A functional unit that performs a single function, such as an oscillator. 2. A functional unit that may be configured to perform one of several functions, such as a digital PSoC block or an analog PSoC block.
buffer	1. A storage area for data that is used to compensate for a speed difference, when transferring data from one device to another. Usually refers to an area reserved for IO operations, into which data is read, or from which data is written. 2. A portion of memory set aside to store data, often before it is sent to an external device or as it is received from an external device. 3. An amplifier used to lower the output impedance of a system.
bus	1. A named connection of nets. Bundling nets together in a bus makes it easier to route nets with similar routing patterns. 2. A set of signals performing a common function and carrying similar data. Typically represented using vector notation; for example, address[7:0]. 3. One or more conductors that serve as a common connection for a group of related devices.
clock	The device that generates a periodic signal with a fixed frequency and duty cycle. A clock is sometimes used to synchronize different logic blocks.
comparator	An electronic circuit that produces an output voltage or current whenever two input levels simultaneously satisfy predetermined amplitude requirements.

Glossary (continued)

compiler	A program that translates a high level language, such as C, into machine language.
configuration space	In PSoC devices, the register space accessed when the XIO bit, in the CPU_F register, is set to '1'.
crystal oscillator	An oscillator in which the frequency is controlled by a piezoelectric crystal. Typically a piezoelectric crystal is less sensitive to ambient temperature than other circuit components.
cyclic redundancy check (CRC)	A calculation used to detect errors in data communications, typically performed using a linear feedback shift register. Similar calculations may be used for a variety of other purposes such as data compression.
data bus	A bi-directional set of signals used by a computer to convey information from a memory location to the central processing unit and vice versa. More generally, a set of signals used to convey data between digital functions.
debugger	A hardware and software system that allows the user to analyze the operation of the system under development. A debugger usually allows the developer to step through the firmware one step at a time, set break points, and analyze memory.
dead band	A period of time when neither of two or more signals are in their active state or in transition.
digital blocks	The 8-bit logic blocks that can act as a counter, timer, serial receiver, serial transmitter, CRC generator, pseudo-random number generator, or SPI.
digital-to-analog (DAC)	A device that changes a digital signal to an analog signal of corresponding magnitude. The analog-to-digital (ADC) converter performs the reverse operation.
duty cycle	The relationship of a clock period high time to its low time, expressed as a percent.
emulator	Duplicates (provides an emulation of) the functions of one system with a different system, so that the second system appears to behave like the first system.
external reset (XRES)	An active high signal that is driven into the PSoC device. It causes all operation of the CPU and blocks to stop and return to a pre-defined state.
flash	An electrically programmable and erasable, non-volatile technology that provides users with the programmability and data storage of EPROMs, plus in-system erasability. Non-volatile means that the data is retained when power is off.
Flash block	The smallest amount of Flash ROM space that may be programmed at one time and the smallest amount of Flash space that may be protected. A Flash block holds 64 bytes.
frequency	The number of cycles or events per unit of time, for a periodic function.
gain	The ratio of output current, voltage, or power to input current, voltage, or power, respectively. Gain is usually expressed in dB.
I^2C	A two-wire serial computer bus by Philips Semiconductors (now NXP Semiconductors). I2C is an Inter-Integrated Circuit. It is used to connect low-speed peripherals in an embedded system. The original system was created in the early 1980s as a battery control interface, but it was later used as a simple internal bus system for building control electronics. I2C uses only two bi-directional pins, clock and data, both running at +5V and pulled high with resistors. The bus operates at 100 kbits/second in standard mode and 400 kbits/second in fast mode.

Glossary (continued)

port	A group of pins, usually eight.
power on reset (POR)	A circuit that forces the PSoC device to reset when the voltage is lower than a pre-set level. This is one type of hardware reset.
PSoC®	Cypress Semiconductor's PSoC® is a registered trademark and Programmable System-on-Chip™ is a trademark of Cypress.
PSoC Designer™	The software for Cypress' Programmable System-on-Chip technology.
pulse width modulator (PWM)	An output in the form of duty cycle which varies as a function of the applied measurand
RAM	An acronym for random access memory. A data-storage device from which data can be read out and new data can be written in.
register	A storage device with a specific capacity, such as a bit or byte.
reset	A means of bringing a system back to a know state. See hardware reset and software reset.
ROM	An acronym for read only memory. A data-storage device from which data can be read out, but new data cannot be written in.
serial	1. Pertaining to a process in which all events occur one after the other. 2. Pertaining to the sequential or consecutive occurrence of two or more related activities in a single device or channel.
settling time	The time it takes for an output signal or value to stabilize after the input has changed from one value to another.
shift register	A memory storage device that sequentially shifts a word either left or right to output a stream of serial data.
slave device	A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device.
SRAM	An acronym for static random access memory. A memory device allowing users to store and retrieve data at a high rate of speed. The term static is used because, after a value has been loaded into an SRAM cell, it remains unchanged until it is explicitly altered or until power is removed from the device.
SROM	An acronym for supervisory read only memory. The SROM holds code that is used to boot the device, calibrate circuitry, and perform Flash operations. The functions of the SROM may be accessed in normal user code, operating from Flash.
stop bit	A signal following a character or block that prepares the receiving device to receive the next character or block.
synchronous	1. A signal whose data is not acknowledged or acted upon until the next active edge of a clock signal. 2. A system whose operation is synchronized by a clock signal.

Errata

This section describes the errata for the CY8C23433, CY8C23533 PSoC® programmable system-on-chip family. Details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability.

Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

Part Number	Ordering Information
CY8C23433	CY8C23433-24PVXI
	CY8C23433-24PVXIT
CY8C23533	CY8C23533-24LQXI
	CY8C23533-24LQXIT

CY8C23433 Qualification Status

Product Status: Production

CY8C23433 Errata Summary

The following table defines the errata applicability to available CY8C23433 family devices. An "X" indicates that the errata pertains to the selected device.

Note Errata items, in the table below, are hyperlinked. Click on any item entry to jump to its description.

Items	Part Number	Silicon Revision	Fix Status
[1.]. Internal Main Oscillator (IMO) Tolerance Deviation at Temperature Extremes	CY8C23433	A	Silicon fix is planned.

1. **Internal Main Oscillator (IMO) Tolerance Deviation at Temperature Extremes**
   - **Problem Definition**
     Asynchronous Digital Communications Interfaces may fail framing beyond 0 to 70°C. This problem does not affect end-product usage between 0 and 70 °C.
   - **Parameters Affected**
     The IMO frequency tolerance. The worst case deviation when operated below 0 °C and above +70 °C and within the upper and lower datasheet temperature range is ±5%.
   - **Trigger Condition(S)**
     The asynchronous Rx/Tx clock source IMO frequency tolerance may deviate beyond the data sheet limit of ±2.5% when operated beyond the temperature range of 0 to +70 °C.
   - **Scope of Impact**
     This problem may affect UART, IrDA, and FSK implementations.
   - **Workaround**
     Implement a quartz crystal stabilized clock source on at least one end of the asynchronous digital communications interface.
   - **Fix Status**
     The cause of this problem and its solution has been identified. Silicon fix is planned to correct the deficiency in silicon.

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