Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	16MHz
Connectivity	CANbus, EBI/EMI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	48
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	68-LCC (J-Lead)
Supplier Device Package	68-PLCC (24.18x24.18)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p80c592ffa-00-518

7.1 Program Memory

The Program Memory of the P8xC592 consists of 16 kbytes ROM on-chip, externally expandible up to 64 kbytes.

Table 3 Instruction fetch controlled by $\overline{EA}$

PIN $\overline{EA}$ (note 1)		INSTRUCTIONS FETCHED FROM:	ADDRESS LOCATION
DURING RESET LATCHED TO:	AFTER RESET		
H	–	internal Program Memory (note 2)	0000H → 3FFFH
H	–	external Program Memory	4000H → FFFFH
L	–		0000H → FFFFH
–	'don't care'	–	–

Notes

1. This implementation prevents reading of the internal program code by switching from external Program Memory during a MOVC instruction.
2. By setting a security bit the internal Program Memory content is protected, which means it cannot be read out. If the security bit has been set to LOW there are no restrictions for the MOVC instruction.

7.2 Internal Data Memory

The internal Data Memory is physically built-up and accessible as shown in Table 4 (see Fig.5).

Table 4 Internal Data Memory size and address mode

INTERNAL DATA MEMORY	SIZE	LOCATION	ADDRESS MODE		POINTERS
			DIRECT	INDIRECT	
MAIN RAM (note 1)	256 bytes	0 to 127	X	X	address pointers are R0 and R1 of the selected register bank
		128 to 255	–	X	
AUXILIARY RAM (note 2)	256 bytes	0 to 255	–	X	address pointers are R0 and R1 of the selected register bank and the DPTR
SFRs (note 3)	128 bytes	128 to 255	X	–	–

Notes

1. MAIN RAM can be addressed directly and indirectly as in the 80C51.
2. AUXILIARY RAM (0 to 255):
   a) Is indirectly addressable in the same way as the external Data Memory with MOVX instructions.
   b) Access will not affect the ports P0, P2, P3.6 and P3.7 during internal program execution.
3. SFRs = Special Function Registers.

7.2.1 MAIN RAM

Four 8-bit register banks occupy the lower RAM area,

- BANK 0: location 0 to 7
- BANK 1: location 8 to 15
- BANK 2: location 16 to 23
- BANK 4: location 24 to 31.

Only one of these banks may be enabled at the same time.

The next 16 bytes, locations 32 through 45, contains 128 directly addressable bit locations.

The stack can be located anywhere in the internal MAIN RAM address space. The stack depth is only limited by the internal RAM space available. All registers except the program counter and the four 8-bit register banks reside in the SFR address space.

7.3 External Data Memory

An access to external Data Memory locations higher than 255 will be performed with the MOVX @DPTR instructions in the same way as in the 80C51 structure,
i.e. with P0 and P2 as data/address bus and P3.6 and P3.7 as Write and Read strobe signals.

Note that these external Data Memory locations cannot be accessed with R0 or R1 as address pointer.

7FH	(MSB)							(LSB)	127
2FH	7F	7E	7D	7C	7B	7A	79	78	47
2EH	77	76	75	74	73	72	71	70	46
2DH	6F	6E	6D	6C	6B	6A	69	68	45
2CH	67	66	65	64	63	62	61	60	44
2BH	5F	5E	5D	5C	5B	5A	59	58	43
2AH	57	56	55	54	53	52	51	50	42
29H	4F	4E	4D	4C	4B	4A	49	48	41
28H	47	46	45	44	43	42	41	40	40
27H	3F	3E	3D	3C	3B	3A	39	38	39
26H	37	36	35	34	33	32	31	30	38
25H	2F	2E	2D	2C	2B	2A	29	28	37
24H	27	26	25	24	23	22	21	20	36
23H	1F	1E	1D	1C	1B	1A	19	18	35
22H	17	16	15	14	13	12	11	10	34
21H	0F	0E	0D	0C	0B	0A	09	08	33
20H	07	06	05	04	03	02	01	00	32
1FH – 18H	BANK 3								31 – 24
17H – 10H	BANK 2								23 – 16
0FH – 08H	BANK 1								15 – 8
07H – 00H	BANK 0								7 – 0

MGA152

Fig.5 Internal MAIN RAM bit addresses.

9.1 Prescaler frequency control register (PWMP)

Table 7 Prescaler frequency control register (address FEH)

7	6	5	4	3	2	1	0
PWMP.7	PWMP.6	PWMP.5	PWMP.4	PWMP.3	PWMP.2	PWMP.1	PWMP.0

Table 8 Description of PWMP bits

BIT	SYMBOL	FUNCTION
7 to 0	PWMP.7 to PWMP.0	**Prescaler division factor**. The Prescaler division factor = (PWMP) + 1.

9.2 Pulse Width Register 0 (PWM0)

Table 9 Pulse Width Register (address FCH)

7	6	5	4	3	2	1	0
PWM0.7	PWM0.6	PWM0.5	PWM0.4	PWM0.3	PWM0.2	PWM0.1	PWM0.0

Table 10 Description of PWM0 bits

BIT	SYMBOL	FUNCTION
7 to 0	PWM0.7 to PWM0.0	**Pulse width ratio.** LOW/HIGH ratio of $\overline{PWMn}$ signals $= \frac{(PWMn)}{255 - (PWMn)}$

9.3 Pulse Width Register 1 (PWM1)

Table 11 Pulse width register (address FDH)

7	6	5	4	3	2	1	0
PWM1.7	PWM1.6	PWM1.5	PWM1.4	PWM1.3	PWM1.2	PWM1.1	PWM1.0

Table 12 Description of PWM1 bits

BIT	SYMBOL	FUNCTION
7 to 0	PWM1.7 to PWM1.0	**Pulse width ratio.** LOW/HIGH ratio of $\overline{PWMn}$ signals $= \frac{(PWMn)}{255 - (PWMn)}$

10.1 ADC Control register (ADCON)

Table 13 ADC Control register (address C5H)

7	6	5	4	3	2	1	0
ADC.1	ADC.0	ADEX	ADCI	ADCS	AADR2	AADR1	AADR0

Table 14 Description of the ADCON bits

BIT	SYMBOL	FUNCTION
7	ADC.1	Bit 1 of ADC converted value.
6	ADC.0	Bit 0 of ADC converted value.
5	ADEX	Enable external start of conversion by STADC. If ADEX is: LOW, then conversion cannot be started externally by STADC (only by software by setting ADCS) HIGH, then conversion can be started externally by a rising edge on STADC or externally.
4	ADCI	**ADC interrupt flag.** This flag is set when an analog-to-digital conversion result is ready to be read. If enabled, an interrupt is invoked. The flag must be cleared by software. It cannot be set by software (see Table 15).
3	ADCS	**ADC start and status.** Setting this bit starts an analog-to-digital conversion. It may be set by software or by the external signal STADC. The ADC logic ensures that this signal is HIGH while the ADC is busy. On completion of the conversion, ADCS is reset at the same time the interrupt flag ADCI is set. ADCS can not be reset by software (see Table 15).
2	AADR2	**Analog input select**. This binary coded address selects one of the eight analog port pins of P5 to be input to the converter. It can only be changed when ADCI and ADCS are both LOW. AADR2 is the MSB. (e.g. 100B selects the analog input channel ADC4)
1	AADR1	
0	AADR0	

Table 15 ADCI and ADCS operating modes

If ADCI is cleared by software while ADCS is set at the same time a new analog-to-digital conversion with the same channel-number may be started. It is recommended to reset ADCI before ADCS is set.

ADCI	ADCS	OPERATION
0	0	ADC not busy, a conversion can be started.
0	1	ADC busy, start of a new conversion is blocked.
1	X (don’t care)	Conversion completed; see note 1.

Note

1. Start of a new conversion requires ADCI = 0.

13.5 Control Segment and Message Buffer description

The CAN-controller appears to the CPU as a memory-mapped peripheral, guaranteeing the independent operation of both parts.

13.5.1 ADDRESS ALLOCATION

The address area of the CAN-controller consists of the Control Segment and the message buffers. The Control Segment is programmed during an initialization down-load in order to configure communication parameters (e.g. bit timing). The communication over the CAN-bus is also controlled via this segment by the CPU. A message which is to be transmitted, must be written to the Transmit Buffer. After a successful reception the CPU may read the message from the Receive Buffer and then release it for further use.

13.5.2 CONTROL SEGMENT LAYOUT

The exchange of status, control and command signals between the CPU and the CAN-controller is performed in the control segment. The layout of this segment is shown in Fig.15. After an initial down-load, the contents of the registers Acceptance Code, Acceptance Mask, Bus Timing 0, Bus Timing 1 and Output Control should not be changed. These registers may only be accessed when the Reset Request bit in the Control Register is set HIGH (see Tables 30, 31 and 32).

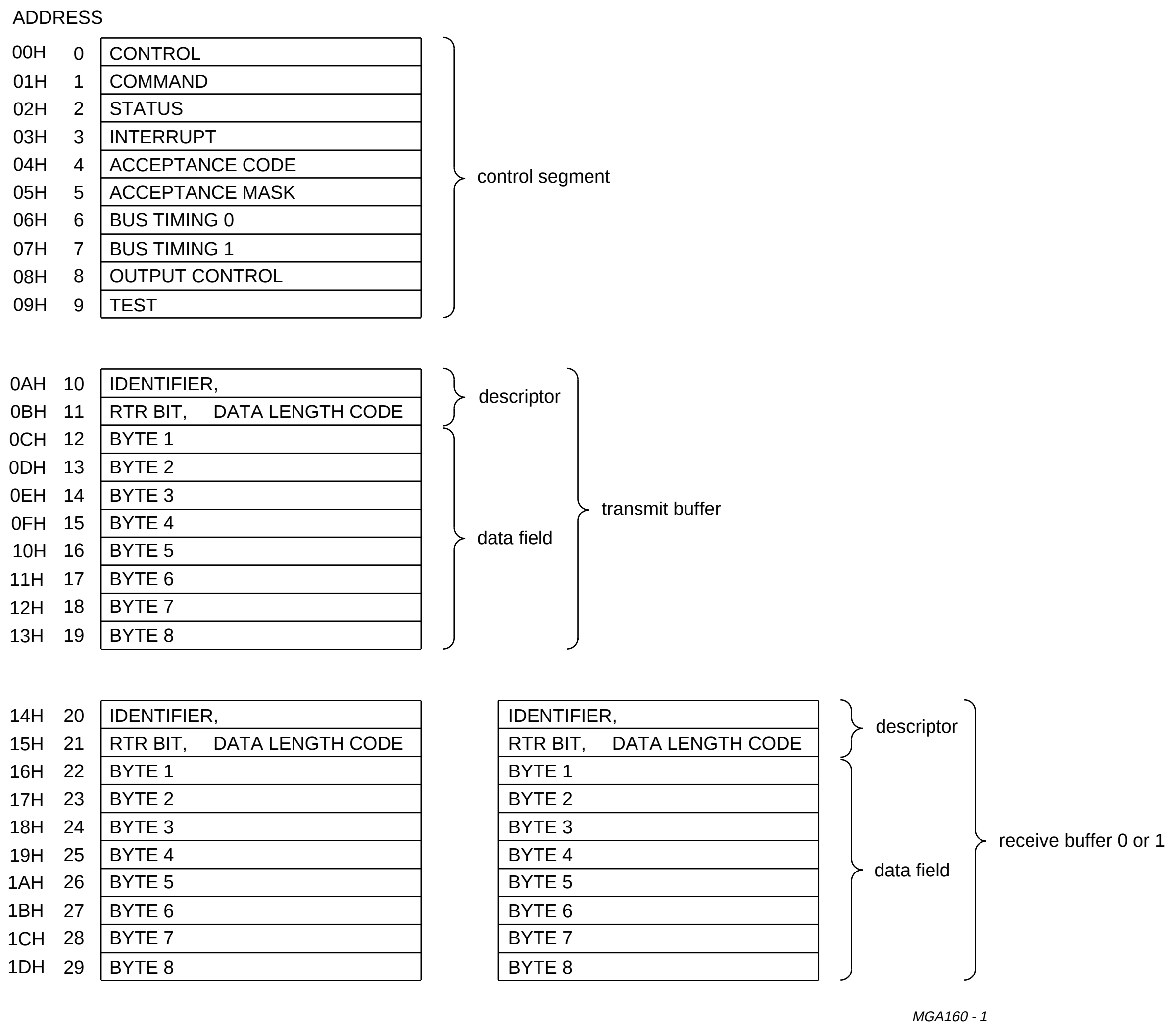


Fig.15 CAN-controller internal address allocation.

13.5.4 COMMAND REGISTER (CMR)

A command bit initiates an action within the transfer layer of the CAN-controller. The Command Register appears to the CPU as a read/write memory, except for the bits CMR.0 (TR) to CMR.3 (COS), which return a HIGH if being read.

Table 33 Command Register (address 1)

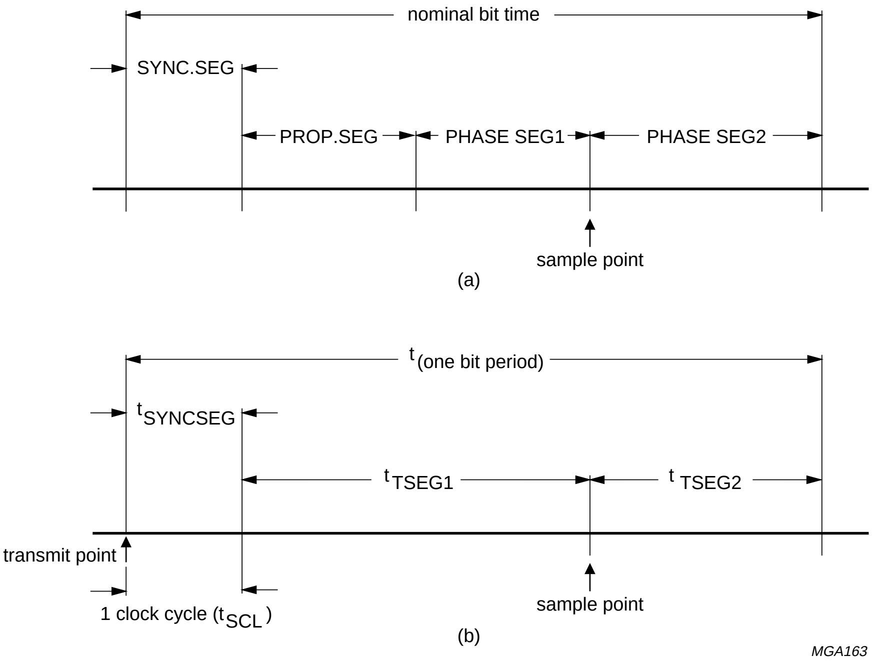
7	6	5	4	3	2	1	0
RX0A	RX1A	WUM	SLP	COS	RRB	AT	TR

Table 34 Description of the CMR bits

BIT	SYMBOL	FUNCTION
7	RX0A	**RX0 Active**. See Table 35; note 1.
6	RX1A	**RX1 Active**. See Table 35; note 1.
5	WUM	**Wake-up Mode** (note 2). If the value of WUM is: HIGH (single ended), then the difference of the RX signals to the internal reference voltage $\frac{1}{2}AV_{DD}$ is used for wake up. LOW (differential), then the differential signal between RX0 and RX1 is used for wake up.
4	SLP	**Sleep** (note 3). If the value of SLP is: HIGH (sleep), then the CAN-controller enters sleep mode if no CAN interrupt is pending and there is no bus activity. LOW (wake up), then the CAN-controller functions normally.
3	COS	**Clear Overrun Status** (note 4). If the value of COS is: HIGH (clear), then the Data Overrun status bit is set to LOW (see Table 37). LOW (no action), then there is no action.
2	RRB	**Release Receive Buffer** (note 5). If the value of RRB is: HIGH (released), then the Receive Buffer attached to the CPU is released. LOW (no action), then there is no action.
1	AT	**Abort Transmission** (note 6). If the value of AT is: HIGH (present) and if not already in progress, a pending Transmission Request is cancelled. LOW (absent), then there is no action.
0	TR	**Transmission Request** (note 7). If the value of TR is: HIGH (present), then a message shall be transmitted. LOW (absent), then there is no action.

Notes to the description of the SR bits

1. When the Bus Status bit is set HIGH (Bus-OFF), the CAN-controller will set the Reset Request bit HIGH (present). It will stay in this state until the CPU sets the Reset Request bit LOW (absent). Once this is completed the CAN-controller will wait the minimum protocol-defined time (128 occurrences of the Bus-Free signal) before setting the Bus Status bit LOW (Bus-ON), the Error Status bit LOW (ok) and resetting the Error Counters. During Bus-OFF the output drivers are switched off (floating); external transceiver circuits should output a recessive level in this case.
2. If both the Receive Status and Transmit Status bits are LOW (idle) the CAN-bus is idle.
3. If the CPU tries to write to the Transmit Buffer when the Transmit Buffer Access bit is LOW (locked), the written bytes will not be accepted and will be lost without this being signalled. The Transmission Complete Status bit is set LOW (incomplete) whenever the Transmission Request bit is set HIGH (present). If an Abort Transmission command is issued, the Transmit Buffer will be released. If the message, which was requested and then aborted, was not transmitted, the Transmission Complete Status bit will remain LOW.
4. If Data Overrun = HIGH (overrun) is detected, the currently received message is dropped. A transmitted message, granted acceptance, is also stored in a Receive Buffer. This occurs because it is not known if the CAN-controller will lose arbitration and so become a receiver of the message. If no Receive Buffer is available, Data Overrun is signalled. However, this transmitted and accepted message does neither cause a Receive Interrupt nor set the Receive Buffer Status bit to HIGH (full). Also, a Data Overrun does not cause the transmission of an Overload Frame (see Sections 13.6.1 and 13.6.5).
5. If the command bit Release Receive Buffer is set HIGH (released) by the CPU, the Receive Buffer Status bit is set LOW (empty) by IML. When a new message is stored in any of the receive buffers, the Receive Buffer Status bit is set HIGH (full) again.



(a) As defined by the CAN-protocol.
(b) As implemented in the P8xC592's on-chip CAN-controller.

Fig.18 Bit period.

13.5.19.2 Time Segment 1 (TSEG1)

This segment determines the location of the sampling point within a bit period, which is at the end of TSEG1. TSEG1 is programmable from 1 to 16 system clock cycles (see Section 13.5.10).

The correct location of the sample point is essential for the correct functioning of a transmission. The following points must be taken into consideration:

- A Start-Of-Frame (see Section 13.6.2) causes all CAN-controllers to perform a ‘hard synchronization’ (see Section 13.5.20) on the first recessive-to-dominant edge.
  During arbitration, however, several CAN-controllers may simultaneously transmit. Therefore it may require twice the sum of bus-line, input comparator and the output driver delay times until the bus is stable.
  This is the propagation delay time.
- To avoid sampling at an incorrect position, it is necessary to include an additional synchronization buffer on both sides of the sample point.
  The main reasons for incorrect sampling are:
  – Incorrect synchronization due to spikes on the bus-line
  – Slight variations in the oscillator frequency of each CAN-controller in the network, which results in a phase error.
- Time Segment 1 consists of the segment for compensation of propagation delays and the synchronization buffer segment directly before the sample point (see Fig.18).

13.5.19.3 Time Segment 2 (TSEG2)

This time segment provides:

- Additional time at the sample point for calculation of the subsequent bit levels (e.g. arbitration)
- Synchronization buffer segment directly after the sample point.

TSEG2 is programmable from 1 to 8 system clock cycles (see Section 13.5.10).

13.5.19.4 Synchronisation Jump Width (SJW)

SJW defines the maximum number of clock cycles (t_{SCL}) a period may be reduced or increased by one resynchronization. SJW is programmable from 1 to 4 system clock cycles, see Section 13.5.2.

13.5.19.5 Propagation Delay Time (t_{prop})

The Propagation Delay Time is:

$$t_{prop} = 2 \times (\text{physical bus delay} + \text{input comparator delay} + \text{output driver delay}).$$

t_{prop} is rounded up to the nearest multiple of t_{SCL}.

13.5.19.6 Bit Timing Restrictions

Restrictions on the configuration of the bit timing are based on internal processing. The restrictions are:

- $t_{TSEG2} \geq 2t_{SCL}$
- $t_{TSEG2} \geq t_{SJW}$
- $t_{TSEG1} \geq t_{SEG2}$
- $t_{TSEG1} \geq t_{SJW} + t_{prop}$.

The three sample mode (SAM = HIGH) has the effect of introducing a delay of one system clock cycle on the bus-line. This must be taken into account for the correct calculation of TSEG1 and TSEG2:

- $t_{TSEG1} \geq t_{SJW} + t_{prop} + 2t_{SCL}$
- $t_{TSEG2} \geq 3t_{SCL}$.

13.5.20 SYNCHRONIZATION

Synchronization is performed by a state machine which compares the incoming edge with its actual bit timing and adapts the bit timing by hard synchronization or resynchronization.

This type of synchronization occurs only at the beginning of a message.

The CAN-controller synchronizes on the first incoming recessive-to-dominant edge of a message (being the leading edge of a message's Start-Of-Frame bit; see Section 13.6.2.

Resynchronization occurs during the transmission of a message's bit stream to compensate for:

- Variations in individual CAN-controller oscillator frequencies
- Changes introduced by switching from one transmitter to another (e.g. during arbitration).

As a result of resynchronization either t_{TSEG1} may be increased by up to a maximum of t_{SJW} or t_{TSEG2} may be decreased by up to a maximum of t_{SJW}:

- $t_{TSEG1} \leq t_{SCL}$ [(TSEG1 + 1) + (SJW + 1)]
- $t_{TSEG2} \geq t_{SCL}$ [(TSEG2 + 1) – (SJW + 1)].

TSEG1, TSEG2 and SJW are the programmed numerical values.

The phase error (e) of an edge is given by the position of the edge relative to SYNCSEG, measured in system clock cycles (t_{SCL}).

The value of the phase error is defined as:

- e = 0, if the edge occurs within SYNCSEG
- e > 0, if the edge occurs within TSEG1
- e < 0, if the edge occurs within TSEG2.

The effect of resynchronization is:

- The same as that of a hard synchronization, if the magnitude of the phase error (e) is less or equal to the programmed value of t_{SJW}
- To increase a bit period by the amount of t_{SJW}, if the phase error is positive and the magnitude of the phase error is larger than t_{SJW}
- To decrease a bit period by the amount of t_{SJW}, if the phase error is negative and the magnitude of the phase error is larger than t_{SJW}.

13.6.2.4 RTR bit

A CAN-controller, acting as a receiver for certain information may initiate the transmission of the respective data by transmitting a Remote Frame to the network, addressing the data source via the Identifier and setting the RTR bit HIGH (remote; recessive bus level). If the data source simultaneously transmits a Data Frame containing the requested data, it uses the same Identifier. No bus access conflict occurs due to the RTR bit being set LOW (data; dominant bus level) in the Data Frame.

13.6.2.5 Control Field

This field consists of six bits. It includes two reserved bits (for future expansions of the CAN-protocol), transmitted with a dominant bus level, and is followed by the Data Length Code (4 bits).
The number of bytes (destuffed; number of data bytes to be transmitted/received) in the Data Field is indicated by the Data Length Code. Admissible values of the Data Length Code, and hence the number of bytes in the (destuffed) Data Field, are {0, 1, ..., 8}. A logic 0 (logic 1) in the Data Length Code is transmitted as dominant (recessive) bus level, respectively.

13.6.2.6 Data Field

The data, stored within the Data Field of the Transmit Buffer, are transmitted according to the Data Length Code. Conversely, data of a received Data Frame will be stored in the Data Field of a Receive Buffer. The Data Field can contain from 0 up to 8 bytes. The most significant bit of the first data byte (lowest address) is transmitted/received first.

13.6.2.7 Cyclic Redundancy Code Field (CRC)

The CRC Field consists of the CRC Sequence (15 bits) and the CRC Delimiter (1 recessive bit). The Cyclic Redundancy Code (CRC) encloses the destuffed bit stream of the Start-Of-Frame, Arbitration Field, Data Field and CRC Sequence. The most significant bit of the CRC Sequence is transmitted/received first. This frame check sequence, implemented in the CAN-controller is derived from a cyclic redundancy code best suited for frames with a total bit count of less than 127 bits, see Section 13.6.8.3. With Start-Of-Frame (dominant bit) included in the code word, any rotation of the code word can be detected by the absence of the CRC Delimiter (recessive bit).

13.6.2.8 Acknowledge Field (ACK)

The Acknowledge Field consists of two bits, the Acknowledge Slot and the Acknowledge Delimiter, which are transmitted with a recessive level by the transmitter of the Data Frame. All CAN-controllers having received the matching CRC Sequence, report this by overwriting the transmitter's recessive bit in the Acknowledge Slot with a dominant bit. Thereby a transmitter, still monitoring the bus level recognizes that at least one receiver within the network has received a complete and correct message (i.e. no error was found). The Acknowledge Delimiter (recessive bit) is the second bit of the Acknowledge Field. As a result, the Acknowledge Slot is surrounded by two recessive bits: the CRC Delimiter and the Acknowledge Delimiter.

All nodes within a CAN network may use all the information coming to the network by all CAN-controllers (shared memory concept). Therefore, acknowledgement and error handling are defined to provide all information in a consistent way throughout this shared memory. Hence, there is no reason to discriminate different receivers of a message in the acknowledge field. If a node is disconnected from the network due to bus failure, this particular node is no longer part of the shared memory. To identify a ‘lost node’ additional and application specific precautions are required.

13.6.2.9 End-Of-Frame

Each Data Frame or Remote Frame is delimited by the End-Of-Frame bit sequence which consists of seven recessive bits (exceeds the bit stuff width by two bits). Using this method a receiver detects the end of a frame independent of a previous transmission error because the receiver expects all bits up to the end of the CRC Sequence to be coded by the method of bit-stuffing, see Section 13.6.7.3. The bit-stuffing logic is deactivated during the End-Of-Frame sequence.

13.6.3 REMOTE FRAME

A CAN-controller acting as a receiver for certain information may initiate the transmission of the respective data by transmitting a Remote Frame to the network, addressing the data source via the Identifier and setting the RTR bit HIGH (remote; recessive bus level). The Remote Frame is similar to the Data Frame with the following exceptions:

- RTR bit is set HIGH
- Data Length Code is ignored
- No Data Field contained.

Note that the value of the Data Length Code should be the one of the corresponding Data Frame, although it is ignored for a Remote Frame.

A Remote Frame is composed of six different bit fields:

- Start-of-Frame
- Arbitration Field
- Control Field
- CRC Field
- Acknowledge Field
- End-Of-Frame.

See Section 13.6.2 for more detailed explanation of the Remote Frame bit fields.

13.6.4 ERROR FRAME

The Error Frame consists of two different fields:

- The first field, accomplished by the superimposing of Error Flags contributed from different CAN-controllers
- The second field is the Error Delimiter.

13.6.4.1 Error Flag

There are two forms of an Error Flag:

- Active Error Flag, consists of six consecutive dominant bits.
- Passive Error Flag, consists of six consecutive recessive bits unless it is overwritten by dominant bits from other CAN-controllers.

An error-active CAN-controller (see Section 13.6.9) detecting an error condition signals this by transmission of an Active Error Flag. This Error Flag's form violates the bit-stuffing rule (see Section 13.6.7) applied to all fields, from Start-Of-Frame to CRC Delimiter, or destroys the fixed form of the fields Acknowledge Field or End-Of-Frame (see Fig.20).

Consequently, all other CAN-controllers detect an error condition and start transmission of an Error Flag. Therefore the sequence of dominant bits, which can be monitored on the bus, results from a superposition of different Error Flags transmitted by individual CAN-controllers. The total length of this sequence varies between six (minimum) and twelve (maximum) bits.

An error-passive CAN-controller (see Section 13.6.9) detecting an error condition tries to signal this by transmission of a Passive Error Flag. The error-passive CAN-controller waits for six consecutive bits with identical polarity, beginning at the start of the Passive Error Flag. The Passive Error Flag is complete when these six identical bits have been detected.

13.6.4.2 Error Delimiter

The Error Delimiter consists of eight recessive bits and has the same format as the Overload Delimiter. After transmission of an Error Flag, each CAN-controller monitors the bus-line until it detects a transition from a dominant-to-recessive bit level. At this point in time, every CAN-controller has finished sending its Error Flag and has additionally sent the first out of the 8 recessive bits of the Error Delimiter. Afterwards all CAN-controllers transmit the remaining recessive bits. After this event and an Intermission Field all error-active CAN-controllers within the network can start a transmission simultaneously.

If a detected error is signalled during transmission of a Data Frame or Remote Frame, the current message is spoiled and a retransmission of the message is initiated.

If a CAN-controller monitors any deviation of the Error Frame, a new Error Frame will be transmitted. Several consecutive Error Frames may result in the CAN-controller becoming error-passive and leaving the network unblocked.

In order to terminate an Error Flag correctly, an error-passive CAN-controller requires the bus to be Bus-Idle (see Section 13.6.6) for at least three bit periods (if there is a local error at an error-passive-receiver). Therefore a CAN-bus should not be 100% permanently loaded.

13.6.7.4 Error Signalling

A CAN-controller which detects an error condition, transmits an Error Flag. Whenever a Bit Error, Stuff Error, Form Error or an Acknowledgement Error is detected, transmission of an Error Flag is started at the next bit. Whenever a CRC Error is detected, transmission of an Error Flag starts at the bit following the Acknowledge Delimiter, unless an Error Flag for another error condition has already started. An Error Flag violates the bit-stuffing law or corrupts the fixed form bit fields. A violation of the bit-stuffing law affects any CAN-controller which detects the error condition. These devices will also transmit an Error Flag.

An error-passive CAN-controller (see Section 13.6.9) which detects an error condition, transmits a Passive Error Flag. A Passive Error Flag is not able to interrupt a current message at different CAN-controllers but this type of Error Flag may be ignored (overwritten) by other CAN-controllers. After having detected an error condition, an error-passive CAN-controller will wait for six consecutive bits with identical polarity and when monitoring them, interpret them as an Error Flag.

After transmission of an Error Flag, each CAN-controller monitors the bus-line until it detects a transition from a dominant-to-recessive bit level. At this point in time, every CAN-controller has finished transmitting its Error Flag and all CAN-controllers start transmitting seven additional recessive bits (Error Delimiter, see Section 13.6.4).

The message format of a Data Frame or Remote Frame is defined in such a way that all detectable errors can be signalled within the message transmission time and therefore it is very simple for the CAN-controllers to associate an Error Frame to the corresponding message and to initiate retransmission of the corrupted message. If a CAN-controller monitors any deviation of the fixed form of an Error Frame, it transmits a new Error Frame.

13.6.7.5 Overload Signalling

Some CAN-controllers (but not the one on-chip of the P8xC592) require to delay the transmission of the next Data Frame or Remote Frame by transmitting one or more Overload Frames. The transmission of an Overload Frame must start during the first bit of an expected Intermission Field. Transmission of Overload Frames which are reactions on a dominant bit during an expected Intermission Field, start one bit after this event.

Though the format of Overload Frame and Error Frame are identical, they are treated differently. Transmission of an Overload Frame during Intermission Field does not initiate the retransmission of any previous Data Frame or Remote Frame. If a CAN-controller which transmitted an Overload Frame monitors any deviation of its fixed form, it transmits an Error Frame.

13.6.8 ERROR DETECTION

The processes described in Sections 13.6.8.1 to 13.6.10.3 are implemented in the P8xC592's on-chip CAN-controller for error detection.

13.6.8.1 Bit Error

A transmitting CAN-controller monitors the bus on a bit-by-bit basis. If the bit level monitored is different from the transmitted one, a Bit Error is signalled.
The exceptions being:

- During the Arbitration Field, a recessive bit can be overwritten by a dominant bit. In this case, the CAN-controller interprets this as a loss of arbitration.
- During the Acknowledge Slot, only the receiving CAN-controllers are able to recognize a Bit Error.

13.6.8.2 Stuff Error

The following bit fields are coded using the bit-stuffing technique:

- Start-Of-Frame
- Arbitration Field
- Control Field
- Data Field
- CRC Sequence.

There are two possible ways of generating a Stuff Error:

- A disturbance generates more than the allowed five consecutive bits with identical polarity. These errors are detected by all CAN-controllers.
- A disturbance falsifies one or more of the five bits preceding the stuff bit. This error situation is not recognized as a Stuff Error by the receivers. Therefore, other error detection processes may detect this error condition such as:
  - CRC check, format violation at the receiving CAN-controllers, or
  - Bit Error detection by the transmitting CAN-controller.

15.1 Power Control Register (PCON)

Table 80 Power Control Register (address 87H)

7	6	5	4	3	2	1	0
SMOD	–	–	WLE	GF1	GF0	PD	IDL

Table 81 Description of the PCON bits

BIT	SYMBOL	FUNCTION
7	SMOD	**Double baud rate bit**. When set to logic 1 the baud rate is doubled when the serial port SIO0 is being used in Modes 1, 2 and 3.
6	–	Reserved.
5	–	
4	WLE	**Watchdog Load Enable**. This flag must be set by software prior to loading T3 (Watchdog timer). It is cleared when T3 is loaded.
3	GF1	**General purpose flag bits.**
2	GF0	
1	PD	**Power-down bit**. Setting this bit activates Power-down mode (note 1). It can only be set if input $\overline{EW}$ is HIGH.
0	IDL	**Idle mode bit**. Setting this bit activates the Idle mode (note 1).

Note

1. If PD and IDL are set to HIGH at the same time, PD takes precedence. The reset value of PCON is 0XX00000B.

15.2 CAN Sleep Mode

In order to reduce power consumption of the P8xC592 the CAN-controller may be switched off (disconnecting the internal clock) by setting the CAN Command Register bit 4 (Sleep) HIGH. The CAN-controller leaves this Sleep mode by detecting either activity on the CAN-bus (dominant bit-level on CRX0/CRX1; see Chapter 5, Table 1) or by setting the Sleep bit to LOW. As the CPU can not only write to the Sleep bit, but can also read it, the CAN-controller status can be determined directly.

15.3 Idle Mode

The instruction that sets bit PCON.0 to HIGH is the last one executed in the normal operating mode before Idle mode is activated.

Once in the Idle mode, the CPU status is preserved in its entirety: the Stack Pointer, Program Counter, Program Status Word, Accumulator, RAM and all other registers maintain their data during Idle mode. The status of the external pins during Idle mode is shown in see Table 82.

There are three ways to terminate the Idle mode:

- Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware, provided that the interrupt source is active during Idle mode. After the interrupt is serviced, the program continues with the instruction immediately after the one, at which the interrupt request was detected.
- The flag bits GF0 and GF1 may be used to determine whether the interrupt was received during normal execution or during the Idle mode. For example, the instruction that writes to PCON.0 can also set or clear one or both flag bits. When Idle mode is terminated by an interrupt, the service routine can examine the status of the flag bits.
- Another way of terminating the Idle mode is an external hardware reset. Since the oscillator is still running, the reset signal is required to be active only for two machine cycles (24 oscillator periods) to complete the reset operation.
- The third way is the internally generated watchdog reset after an overflow of Timer 3.

Table 85 Instruction set description: Logic operations

MNEMONIC		DESCRIPTION	BYTES	CYCLES	OPCODE (HEX)
Logic operations					
ANL	A,Rr	AND register to A	1	1	5*
ANL	A,direct	AND direct byte to A	2	1	55
ANL	A,@Ri	AND indirect RAM to A	1	1	56, 57
ANL	A,#data	AND immediate data to A	2	1	54
ANL	direct,A	AND A to direct byte	2	1	52
ANL	direct,#data	AND immediate data to direct byte	3	2	53
ORL	A,Rr	OR register to A	1	1	4*
ORL	A,direct	OR direct byte to A	2	1	45
ORL	A,@Ri	OR indirect RAM to A	1	1	46, 47
ORL	A,#data	OR immediate data to A	2	1	44
ORL	direct,A	OR A to direct byte	2	1	42
ORL	direct,#data	OR immediate data to direct byte	3	2	43
XRL	A,Rr	Exclusive-OR register to A	1	1	6*
XRL	A,direct	Exclusive-OR direct byte to A	2	1	65
XRL	A,@Ri	Exclusive-OR indirect RAM to A	1	1	66, 67
XRL	A,#data	Exclusive-OR immediate data to A	2	1	64
XRL	direct,A	Exclusive-OR A to direct byte	2	1	62
XRL	direct,#data	Exclusive-OR immediate data to direct byte	3	2	63
CLR	A	Clear A	1	1	E4
CPL	A	Complement A	1	1	F4
RL	A	Rotate A left	1	1	23
RLC	A	Rotate A left through the carry flag	1	1	33
RR	A	Rotate A right	1	1	03
RRC	A	Rotate A right through the carry flag	1	1	13
SWAP	A	Swap nibbles within A	1	1	C4

Table 86 Instruction set description: Data transfer

MNEMONIC		DESCRIPTION	BYTES	CYCLES	OPCODE (HEX)
Data transfer					
MOV	A,Rr	Move register to A	1	1	E*
MOV	A,direct (note 1)	Move direct byte to A	2	1	E5
MOV	A,@Ri	Move indirect RAM to A	1	1	E6, E7
MOV	A,#data	Move immediate data to A	2	1	74
MOV	Rr,A	Move A to register	1	1	F*
MOV	Rr,direct	Move direct byte to register	2	2	A*
MOV	Rr,#data	Move immediate data to register	2	1	7*
MOV	direct,A	Move A to direct byte	2	1	F5
MOV	direct,Rr	Move register to direct byte	2	2	8*
MOV	direct,direct	Move direct byte to direct	3	2	85
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2	86, 87
MOV	direct,#data	Move immediate data to direct byte	3	2	75
MOV	@Ri,A	Move A to indirect RAM	1	1	F6, F7
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2	A6, A7
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1	76, 77
MOV	DPTR,#data16	Load data pointer with a 16-bit constant	3	2	90
MOVC	A,@A+DPTR	Move code byte relative to DPTR to A	1	2	93
MOVC	A,@A+PC	Move code byte relative to PC to A	1	2	83
MOVX	A,@Ri	Move external RAM (8-bit address) to A	1	2	E2, E3
MOVX	A,@DPTR	Move external RAM (16-bit address) to A	1	2	E0
MOVX	@Ri,A	Move A to external RAM (8-bit address)	1	2	F2, F3
MOVX	@DPTR,A	Move A to external RAM (16-bit address)	1	2	F0
PUSH	direct	Push direct byte onto stack	2	2	C0
POP	direct	Pop direct byte from stack	2	2	D0
XCH	A,Rr	Exchange register with A	1	1	C*
XCH	A,direct	Exchange direct byte with A	2	1	C5
XCH	A,@Ri	Exchange indirect RAM with A	1	1	C6, C7
XCHD	A,@Ri	Exchange LOW-order digit indirect RAM with A	1	1	D6, D7

Note

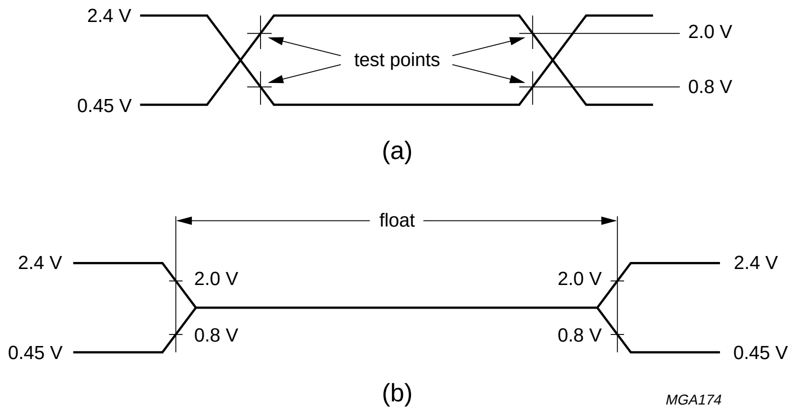
1. MOV A,ACC is not permitted.

Table 88 Description of the mnemonics in the Instruction set

MNEMONIC	DESCRIPTION
Data addressing modes	
Rr	Working register R0-R7.
direct	128 internal RAM locations and any special function register (SFR).
@Ri	Indirect internal RAM location addressed by register R0 or R1 of the actual register bank.
#data	8-bit constant included in instruction.
#data 16	16-bit constant included as bytes 2 and 3 of instruction.
bit	Direct addressed bit in internal RAM or SFR.
addr16	16-bit destination address. Used by LCALL and LJMP. The branch will be anywhere within the 64 kbytes Program Memory address space.
addr11	11-bit destination address. Used by ACALL and AJMP. The branch will be within the same 2 kbytes page of Program Memory as the first byte of the following instruction.
rel	Signed (two's complement) 8-bit offset byte. Used by SJMP and all conditional jumps. Range is –128 to +127 bytes relative to first byte of the following instruction.
Hexadecimal opcode cross-reference	
*	8, 9, A, B, C, D, E, F.
•	1, 3, 5, 7, 9, B, D, F.
♦	0, 2, 4, 6, 8, A, C, E.

Table 90 CAN characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
CAN input comparator/output driver					
t_{sd}	sum of input and output delay	AV_{DD} = 5 V ± 5%; V_{DIF} = ± 32 mV; 1.4 V < V_I < AV_{DD} – 1.4 V	–	60	ns



AC testing inputs are driven at 2.4 V for a HIGH and 0.45 V for a LOW.
Timing measurements are taken at 2.0 V for a HIGH and 0.8 V for a LOW, see Fig.29 (a).
The float state is defined as the point at which a Port 0 pin sinks 3.2 mA or sources 400 µA at the voltage test levels, see Fig.29 (b).

Fig.29 AC testing input, output waveform (a) and float waveform (b).

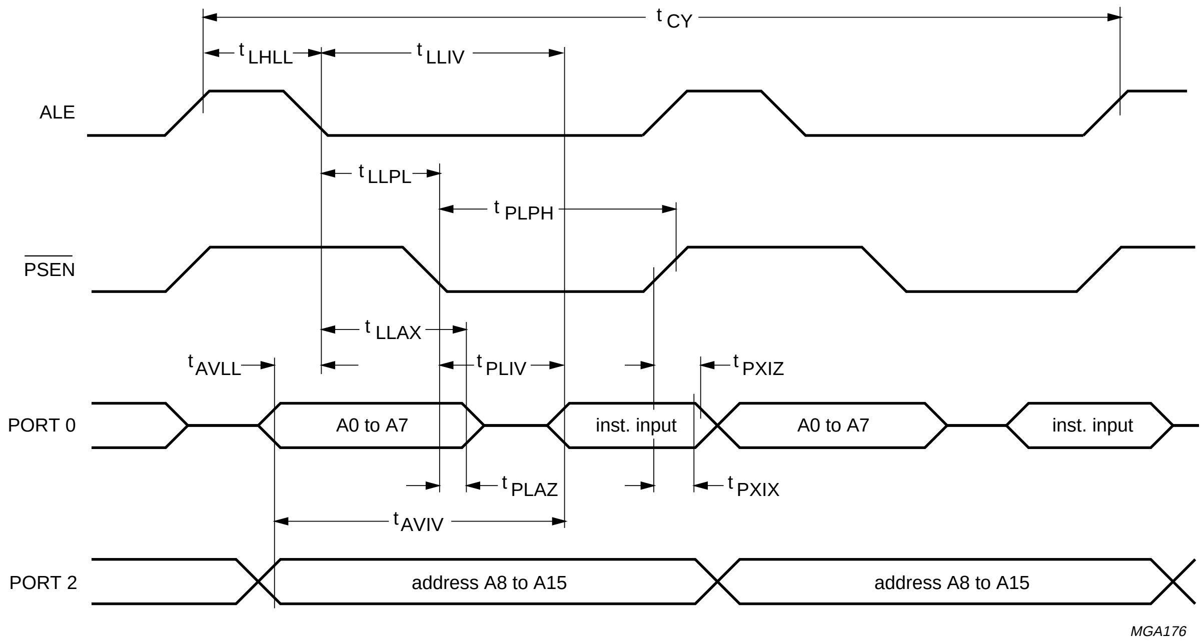


Fig.31 Read from external Program Memory.

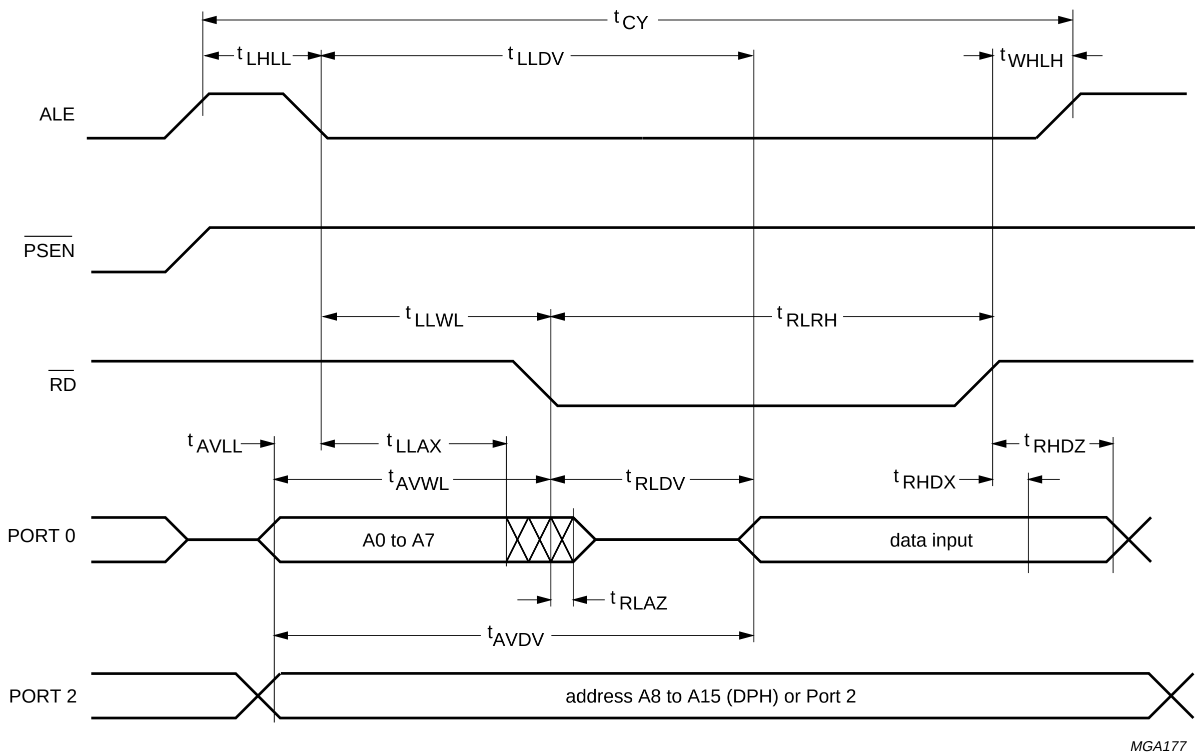


Fig.32 Read from external Data Memory.

```
LOC   OBJ     SOURCE
                    ;commands for the CAN-controller / DMA logic
                    CAN_REF_REL     EQU     00000100B       ;Release Receive Buffer
00A0                CAN_RX_DMA      EQU     80H + 22        ;Rx DMA-transfer
00A1
                    ; addresses of CAN-controller internal registers
                    CAN_REF         EQU     20              ;1st address of Rx-buffer

                    ; masks
                    INT_FLAG_MASK   EQU     00011111B       ;all CAN's interrupt-flags
                    ID2_0_MASK      EQU     11100000B       ;only ID.2 ... ID.0 bits
00A2          ; jump-address for a CAN-controller interrupt


              CSEG at 2BH
      020080        LJMP            CAN_INT_HANDLER         ; CAN's interrupt-vector
00A5
00A7          ; data storage

              DSEG at 20H
                    CAN_INT_IMAGE:  DS      1
00A9
00AB          BSEG at 00H
00AD                CAN_INT_RX:     DBIT    1               ; = CAN_INT_IMAGE.0
                    CAN_INT_TX:     DBIT    1               ; = CAN_INT_IMAGE.1
                    CAN_INT_KR:     DBIT    1               ; = CAN_INT_IMAGE.2
                    CAN_INT_OV:     DBIT    1               ; = CAN_INT_IMAGE.3
                    CAN_INT_WK:     DBIT    1               ; = CAN_INT_IMAGE.4

              ;*****************************************************************************************************
              ;CAN-controller interrupt-handler
00AE          ;
00AF          ;Only the receive-interrupt is coded.
              ;
00B0          ;****************************************************************************************************

              CSEG at 080H

```

Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113, Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213, Tel. +43 1 60 101, Fax. +43 1 60 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6, 220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor, 51 James Bourchier Blvd., 1407 SOFIA, Tel. +359 2 689 211, Fax. +359 2 689 102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS, Tel. +1 800 234 7381, Fax. +1 708 296 8556

China/Hong Kong: 501 Hong Kong Industrial Technology Centre, 72 Tat Chee Avenue, Kowloon Tong, HONG KONG, Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S, Tel. +45 32 88 2636, Fax. +45 31 57 1949

Finland: Sinikalliontie 3, FIN-02630 ESPOO, Tel. +358 615 800, Fax. +358 615 80920

France: 4 Rue du Port-aux-Vins, BP317, 92156 SURESNES Cedex, Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG, Tel. +49 40 23 52 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS, Tel. +30 1 4894 339/911, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Shivsagar Estate, A Block, Dr. Annie Besant Rd. Worli, MUMBAI 400 018, Tel. +91 22 4938 541, Fax. +91 22 4938 722

Indonesia: see Singapore

Ireland: Newstead, Clonskeagh, DUBLIN 14, Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 648 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3, 20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108, Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL, Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR, Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905, Tel. +1 800 234 7381, Fax. +1 708 296 8556

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB, Tel. +31 40 27 83749, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND, Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO, Tel. +47 22 74 8000, Fax. +47 22 74 8341

Philippines: Philips Semiconductors Philippines Inc., 106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI, Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA, Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW, Tel. +7 095 926 5361, Fax. +7 095 564 8323

Singapore: Lorong 1, Toa Payoh, SINGAPORE 1231, Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale, 2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000, Tel. +27 11 470 5911, Fax. +27 11 470 5494

South America: Rua do Rocio 220, 5th floor, Suite 51, 04552-903 São Paulo, SÃO PAULO - SP, Brazil, Tel. +55 11 821 2333, Fax. +55 11 829 1849

Spain: Balmes 22, 08007 BARCELONA, Tel. +34 3 301 6312, Fax. +34 3 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM, Tel. +46 8 632 2000, Fax. +46 8 632 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH, Tel. +41 1 488 2686, Fax. +41 1 481 7730

Taiwan: PHILIPS TAIWAN Ltd., 23-30F, 66, Chung Hsiao West Road, Sec. 1, P.O. Box 22978, TAIPEI 100, Tel. +886 2 382 4443, Fax. +886 2 382 4444

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd., 209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260, Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL, Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 2A Akademika Koroleva str., Office 165, 252148 KIEV, Tel. +380 44 476 0297/1642, Fax. +380 44 476 6991

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes, MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409, Tel. +1 800 234 7381, Fax. +1 708 296 8556

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD, Tel. +381 11 825 344, Fax.+381 11 635 777

For all other countries apply to: Philips Semiconductors, Marketing & Sales Communications, Building BE-p, P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

Internet: http://www.semiconductors.philips.com/ps/

SCA50

Printed in The Netherlands 617021/1200/03/pp108 Date of release: 1996 Jun 27 Document order number: 9397 750 00933

Let's make things better.

Philips Semiconductors

PHILIPS