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Details

Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	24MHz
Connectivity	UART/USART
Peripherals	WDT
Number of I/O	32
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.6x16.6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at89s52-24ji

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



2. Pin Configurations

2.1 40-lead PDIP

	\cup		
(T2) P1.0 🗆	1	40	□ vcc
(T2 EX) P1.1 🗆	2	39	D P0.0 (AD0)
P1.2	3	38	DP0.1 (AD1)
P1.3 🗆	4	37	DP0.2 (AD2)
P1.4 🗆	5	36	D P0.3 (AD3)
(MOSI) P1.5 🗆	6	35	D P0.4 (AD4)
(MISO) P1.6 🗆	7	34	D P0.5 (AD5)
(SCK) P1.7 🗆	8	33	DP0.6 (AD6)
RST 🗆	9	32	D P0.7 (AD7)
(RXD) P3.0 🗆	10	31	□ ĒĀ/VPP
(TXD) P3.1 🗆	11	30	ALE/PROG
(INT0) P3.2 🗆	12	29	D PSEN
(INT1) P3.3 🗆	13	28	🗆 P2.7 (A15)
(T0) P3.4 🗆	14	27	🗆 P2.6 (A14)
(T1) P3.5 🗆	15	26	🗆 P2.5 (A13)
(WR) P3.6 🗆	16	25	🗆 P2.4 (A12)
(RD) P3.7 🗆	17	24	🗆 P2.3 (A11)
XTAL2	18	23	🗆 P2.2 (A10)
XTAL1 🗆	19	22	🗆 P2.1 (A9)
GND 🗆	20	21	🗆 P2.0 (A8)

2.2 44-lead TQFP



2.3 44-lead PLCC



AT89S52

2



4.9 PSEN

Program Store Enable (PSEN) is the read strobe to external program memory.

When the AT89S52 is executing code from external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory.

4.10 **EA**/VPP

External Access Enable. \overline{EA} must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, \overline{EA} will be internally latched on reset.

EA should be strapped to V_{CC} for internal program executions.

This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming.

4.11 XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

4.12 XTAL2

Output from the inverting oscillator amplifier.

5. Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 5-1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Timer 2 Registers: Control and status bits are contained in registers T2CON (shown in Table 5-2) and T2MOD (shown in Table 10-2) for Timer 2. The register pair (RCAP2H, RCAP2L) are the Capture/Reload registers for Timer 2 in 16-bit capture mode or 16-bit auto-reload mode.

Interrupt Registers: The individual interrupt enable bits are in the IE register. Two priorities can be set for each of the six interrupt sources in the IP register.

6

0F8H									0FFH
0F0H	B 00000000								0F7H
0E8H									0EFH
0E0H	ACC 00000000								0E7H
0D8H									0DFH
0D0H	PSW 00000000								0D7H
0C8H	T2CON 00000000	T2MOD XXXXXX00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000			0CFH
0C0H									0C7H
0B8H	IP XX000000								0BFH
0B0H	P3 11111111								0B7H
0A8H	IE 0X000000								0AFH
0A0H	P2 11111111		AUXR1 XXXXXXX0				WDTRST XXXXXXXX		0A7H
98H	SCON 00000000	SBUF XXXXXXXX							9FH
90H	P1 11111111								97H
88H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000	AUXR XXX00XX0		8FH
80H	P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000		PCON 0XXX0000	87H

 Table 5-1.
 AT89S52 SFR Map and Reset Values



Table 5-3.AUXR: Auxiliary Register

AUXR	Address = 8EH Reset Value = XXX00XX0B									
	Not Bit A	Addressable								
		-	_	_	WDIDLE	DISRTO	_	-	DISALE	
	Bit	7	6	5	4	3	2	1	0	
-	Reserved for future expansion									
DISALE	Disable/Enable ALE									
	DISALE	DISALE Operating Mode								
	0	ALE is emitted at a constant rate of 1/6 the oscillator frequency								
	1	ALE is active only during a MOVX or MOVC instruction								
DISRTO	Disable/Enable Reset out									
	DISRTO									
	0	Reset pin	is driven Hig	gh after WD	T times out					
	1	Reset pin	is input only	,						
WDIDLE	Disable/Enal	ble WDT in I	DLE mode							
	WDIDLE									
	0	WDT cont	inues to cou	Int in IDLE I	mode					
	1	WDT halts	counting ir	IDLE mode	e					

Dual Data Pointer Registers: To facilitate accessing both internal and external data memory, two banks of 16-bit Data Pointer Registers are provided: DP0 at SFR address locations 82H-83H and DP1 at 84H-85H. Bit DPS = 0 in SFR AUXR1 selects DP0 and DPS = 1 selects DP1. The user should **ALWAYS** initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

Power Off Flag: The Power Off Flag (POF) is located at bit 4 (PCON.4) in the PCON SFR. POF is set to "1" during power up. It can be set and rest under software control and is not affected by reset.

Table 5-4.AUXR1: Auxiliary Register 1

AUXR1	Address = A2H Reset Value = XXXXXX0B									
	Not Bit Addressable									
		_	_	_	_	_	_	_	DPS	
	Bit	7	6	5	4	3	2	1	0	
-	Reserved for future expansion									
DPS	Data Pointer Register Select									
	DPS									
	0 Selects DPTR Registers DP0L, DP0H									
	1 Selects DPTR Registers DP1L, DP1H									





6. Memory Organization

MCS-51 devices have a separate address space for Program and Data Memory. Up to 64K bytes each of external Program and Data Memory can be addressed.

6.1 Program Memory

If the EA pin is connected to GND, all program fetches are directed to external memory.

On the AT89S52, if \overline{EA} is connected to V_{CC}, program fetches to addresses 0000H through 1FFFH are directed to internal memory and fetches to addresses 2000H through FFFFH are to external memory.

6.2 Data Memory

The AT89S52 implements 256 bytes of on-chip RAM. The upper 128 bytes occupy a parallel address space to the Special Function Registers. This means that the upper 128 bytes have the same addresses as the SFR space but are physically separate from SFR space.

When an instruction accesses an internal location above address 7FH, the address mode used in the instruction specifies whether the CPU accesses the upper 128 bytes of RAM or the SFR space. Instructions which use direct addressing access the SFR space.

For example, the following direct addressing instruction accesses the SFR at location 0A0H (which is P2).

MOV 0A0H, #data

Instructions that use indirect addressing access the upper 128 bytes of RAM. For example, the following indirect addressing instruction, where R0 contains 0A0H, accesses the data byte at address 0A0H, rather than P2 (whose address is 0A0H).

MOV @R0, #data

Note that stack operations are examples of indirect addressing, so the upper 128 bytes of data RAM are available as stack space.

7. Watchdog Timer (One-time Enabled with Reset-out)

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upsets. The WDT consists of a 14-bit counter and the Watchdog Timer Reset (WDTRST) SFR. The WDT is defaulted to disable from exiting reset. To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, it will increment every machine cycle while the oscillator is running. The WDT timeout period is dependent on the external clock frequency. There is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST pin.

7.1 Using the WDT

To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, the user needs to service it by writing 01EH and 0E1H to WDTRST to avoid a WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH), and this will reset the device. When the WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycles. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write-only register. The WDT counter cannot be read or written. When



10. Timer 2

Timer 2 is a 16-bit Timer/Counter that can operate as either a timer or an event counter. The type of operation is selected by bit $C/\overline{12}$ in the SFR T2CON (shown in Table 5-2). Timer 2 has three operating modes: capture, auto-reload (up or down counting), and baud rate generator. The modes are selected by bits in T2CON, as shown in Table 10-1. Timer 2 consists of two 8-bit registers, TH2 and TL2. In the Timer function, the TL2 register is incremented every machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency.

RCLK +TCLK	CP/RL2	TR2	MODE		
0	0	1	16-bit Auto-reload		
0	1	1	16-bit Capture		
1	Х	1	Baud Rate Generator		
Х	Х	0	(Off)		

 Table 10-1.
 Timer 2 Operating Modes

In the Counter function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T2. In this function, the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected. Since two machine cycles (24 oscillator periods) are required to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. To ensure that a given level is sampled at least once before it changes, the level should be held for at least one full machine cycle.

10.1 Capture Mode

In the capture mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 is a 16-bit timer or counter which upon overflow sets bit TF2 in T2CON. This bit can then be used to generate an interrupt. If EXEN2 = 1, Timer 2 performs the same operation, but a 1-to-0 transition at external input T2EX also causes the current value in TH2 and TL2 to be captured into RCAP2H and RCAP2L, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 bit, like TF2, can generate an interrupt. The capture mode is illustrated in Figure 10-1.

10.2 Auto-reload (Up or Down Counter)

Timer 2 can be programmed to count up or down when configured in its 16-bit auto-reload mode. This feature is invoked by the DCEN (Down Counter Enable) bit located in the SFR T2MOD (see Table 10-2). Upon reset, the DCEN bit is set to 0 so that timer 2 will default to count up. When DCEN is set, Timer 2 can count up or down, depending on the value of the T2EX pin.

11. Baud Rate Generator

Timer 2 is selected as the baud rate generator by setting TCLK and/or RCLK in T2CON (Table 5-2). Note that the baud rates for transmit and receive can be different if Timer 2 is used for the receiver or transmitter and Timer 1 is used for the other function. Setting RCLK and/or TCLK puts Timer 2 into its baud rate generator mode, as shown in Figure 11-1.

The baud rate generator mode is similar to the auto-reload mode, in that a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software.

The baud rates in Modes 1 and 3 are determined by Timer 2's overflow rate according to the following equation.

Modes 1 and 3 Baud Rates = $\frac{\text{Timer 2 Overflow Rate}}{16}$

The Timer can be configured for either timer or counter operation. In most applications, it is configured for timer operation (CP/T2 = 0). The timer operation is different for Timer 2 when it is used as a baud rate generator. Normally, as a timer, it increments every machine cycle (at 1/12 the oscillator frequency). As a baud rate generator, however, it increments every state time (at 1/2 the oscillator frequency). The baud rate formula is given below.

 $\frac{\text{Modes 1 and 3}}{\text{Baud Rate}} = \frac{\text{Oscillator Frequency}}{32 \times [65536-\text{RCAP2H},\text{RCAP2L})]}$

where (RCAP2H, RCAP2L) is the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

Timer 2 as a baud rate generator is shown in Figure 11-1. This figure is valid only if RCLK or TCLK = 1 in T2CON. Note that a rollover in TH2 does not set TF2 and will not generate an interrupt. Note too, that if EXEN2 is set, a 1-to-0 transition in T2EX will set EXF2 but will not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). Thus, when Timer 2 is in use as a baud rate generator, T2EX can be used as an extra external interrupt.

Note that when Timer 2 is running (TR2 = 1) as a timer in the baud rate generator mode, TH2 or TL2 should not be read from or written to. Under these conditions, the Timer is incremented every state time, and the results of a read or write may not be accurate. The RCAP2 registers may be read but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers.



Figure 12-1. Timer 2 in Clock-Out Mode



13. Interrupts

The AT89S52 has a total of six interrupt vectors: two external interrupts (INT0 and INT1), three timer interrupts (Timers 0, 1, and 2), and the serial port interrupt. These interrupts are all shown in Figure 13-1.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

Note that Table 13-1 shows that bit position IE.6 is unimplemented. User software should not write a 1 to this bit position, since it may be used in future AT89 products.

Timer 2 interrupt is generated by the logical OR of bits TF2 and EXF2 in register T2CON. Neither of these flags is cleared by hardware when the service routine is vectored to. In fact, the service routine may have to determine whether it was TF2 or EXF2 that generated the interrupt, and that bit will have to be cleared in software.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle. However, the Timer 2 flag, TF2, is set at S2P2 and is polled in the same cycle in which the timer overflows.





19. Programming the Flash – Serial Mode

The Code memory array can be programmed using the serial ISP interface while RST is pulled to V_{cc} . The serial interface consists of pins SCK, MOSI (input) and MISO (output). After RST is set high, the Programming Enable instruction needs to be executed first before other operations can be executed. Before a reprogramming sequence can occur, a Chip Erase operation is required.

The Chip Erase operation turns the content of every memory location in the Code array into FFH.

Either an external system clock can be supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK) frequency should be less than 1/16 of the crystal frequency. With a 33 MHz oscillator clock, the maximum SCK frequency is 2 MHz.

20. Serial Programming Algorithm

To program and verify the AT89S52 in the serial programming mode, the following sequence is recommended:

- 1. Power-up sequence:
 - a. Apply power between VCC and GND pins.
 - b. Set RST pin to "H".

If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 33 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.

- 2. Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 16.
- 3. The Code array is programmed one byte at a time in either the Byte or Page mode. The write cycle is self-timed and typically takes less than 0.5 ms at 5V.
- 4. Any memory location can be verified by using the Read instruction which returns the content at the selected address at serial output MISO/P1.6.
- 5. At the end of a programming session, RST can be set low to commence normal device operation.

Power-off sequence (if needed):

- 1. Set XTAL1 to "L" (if a crystal is not used).
- 2. Set RST to "L".
- 3. Turn V_{CC} power off.

Data Polling: The Data Polling feature is also available in the serial mode. In this mode, during a write cycle an attempted read of the last byte written will result in the complement of the MSB of the serial output byte on MISO.

21. Serial Programming Instruction Set

The Instruction Set for Serial Programming follows a 4-byte protocol and is shown in Table 24-1.

22. Programming Interface – Parallel Mode

Every code byte in the Flash array can be programmed by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

Most major worldwide programming vendors offer support for the Atmel AT89 microcontroller series. Please contact your local programming vendor for the appropriate software revision.

				ALE/	EA/						P0.7-0	P2.4-0	P1.7-0
Mode	V _{cc}	RST	PSEN	PROG	V _{PP}	P2.6	P2.7	P3.3	P3.6	P3.7	Data	Add	ress
Write Code Data	5V	н	L	(2)	12V	L	Н	Н	Н	н	D _{IN}	A12-8	A7-0
Read Code Data	5V	н	L	Н	Н	L	L	L	Н	н	D _{OUT}	A12-8	A7-0
Write Lock Bit 1	5V	н	L	(3)	12V	н	Н	Н	Н	Н	х	х	х
Write Lock Bit 2	5V	н	L	(3)	12V	н	Н	Н	L	L	х	х	х
Write Lock Bit 3	5V	н	L	(3)	12V	н	L	Н	Н	L	х	х	х
Read Lock Bits 1, 2, 3	5V	н	L	н	н	н	н	L	н	L	P0.2, P0.3, P0.4	х	х
Chip Erase	5V	н	L	(1)	12V	н	L	Н	L	L	х	х	х
Read Atmel ID	5V	н	L	Н	Н	L	L	L	L	L	1EH	X 0000	00H
Read Device ID	5V	н	L	Н	Н	L	L	L	L	L	52H	X 0001	00H
Read Device ID	5V	Н	L	Н	Н	L	L	L	L	L	06H	X 0010	00H

 Table 22-1.
 Flash Programming Modes

Notes: 1. Each PROG pulse is 200 ns - 500 ns for Chip Erase.

2. Each PROG pulse is 200 ns - 500 ns for Write Code Data.

3. Each PROG pulse is 200 ns - 500 ns for Write Lock Bits.

4. RDY/BSY signal is output on P3.0 during programming.

5. X = don't care.







Figure 22-1. Programming the Flash Memory (Parallel Mode)

Figure 22-2. Verifying the Flash Memory (Parallel Mode)



	Table 24-1.	Serial Programming Instruction Se
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	Instruction Format				
Instruction	Byte 1	Byte 2	Byte 3	Byte 4	Operation
Programming Enable	1010 1100	0101 0011	XXXX XXXX	xxxx xxxx 0110 1001 (Output on MISO)	Enable Serial Programming while RST is high
Chip Erase	1010 1100	100x xxxx	XXXX XXXX	XXXX XXXX	Chip Erase Flash memory array
Read Program Memory (Byte Mode)	0010 0000	A11 2 A11 2 A90 A30 A11 2 A12	AAAA AAAA 7700 4000000000000000000000000000000000	0000 0000 0000 0000	Read data from Program memory in the byte mode
Write Program Memory (Byte Mode)	0100 0000	A11 2 A11 2 A200 A200 A200 A200 A200 A200 A200 A2	AAAA 45601 01203 45601	0000 0000 2000 0000	Write data to Program memory in the byte mode
Write Lock Bits ⁽¹⁾	1010 1100	1110 00 🔤 🛗	xxxx xxxx	xxxx xxxx	Write Lock bits. See Note (1).
Read Lock Bits	0010 0100	XXXX XXXX	XXXX XXXX	XXX EB3 LB2 XXX EB1	Read back current status of the lock bits (a programmed lock bit reads back as a "1")
Read Signature Bytes	0010 1000	A12 A11 A12 A11 A12 A12 A12	⊱xxx xxx0	Signature Byte	Read Signature Byte
Read Program Memory (Page Mode)	0011 0000	A12 XXX A11 2 A11 2 A12 XXX A12 XXX A12 XXX	Byte 0	Byte 1 Byte 255	Read data from Program memory in the Page Mode (256 bytes)
Write Program Memory (Page Mode)	0101 0000	A12 XXX A11 2 A11 2 A12 XXX	Byte 0	Byte 1 Byte 255	Write data to Program memory in the Page Mode (256 bytes)

Note:

1. B1 = 0, $B2 = 0 \longrightarrow Mode 1$, no lock protection

 $B1 = 0, B2 = 1 \dots$ Mode 2, lock bit 1 activated $B1 = 1, B2 = 0 \dots$ Mode 3, lock bit 2 activated

B1 = 1, B2 = 1 ---> Mode 4, lock bit 3 activated

Each of the lock bit modes needs to be activated sequentially before Mode 4 can be executed.

After Reset signal is high, SCK should be low for at least 64 system clocks before it goes high to clock in the enable data bytes. No pulsing of Reset signal is necessary. SCK should be no faster than 1/16 of the system clock at XTAL1.

For Page Read/Write, the data always starts from byte 0 to 255. After the command byte and upper address byte are latched, each byte thereafter is treated as data until all 256 bytes are shifted in/out. Then the next instruction will be ready to be decoded.





25. Serial Programming Characteristics

Figure 25-1. Serial Programming Timing



Table 25-1.Serial Programming Characteristics, $T_A = -40$ · C to 85· C, $V_{CC} = 4.0 - 5.5V$ (Unless Otherwise Noted)

Symbol	Parameter	Min	Тур	Max	Units
1/t _{CLCL}	Oscillator Frequency	3		33	MHz
t _{CLCL}	Oscillator Period	30			ns
t _{SHSL}	SCK Pulse Width High	8 t _{CLCL}			ns
t _{SLSH}	SCK Pulse Width Low	8 t _{CLCL}			ns
t _{OVSH}	MOSI Setup to SCK High	t _{CLCL}			ns
t _{SHOX}	MOSI Hold after SCK High	2 t _{CLCL}			ns
t _{SLIV}	SCK Low to MISO Valid	10	16	32	ns
t _{ERASE}	Chip Erase Instruction Cycle Time			500	ms
t _{SWC}	Serial Byte Write Cycle Time			64 t _{CLCL} + 400	μs



28. AC Characteristics

Under operating conditions, load capacitance for Port 0, ALE/ \overline{PROG} , and $\overline{PSEN} = 100 \text{ pF}$; load capacitance for all other outputs = 80 pF.

		12 MHz	Oscillator	Variable	Oscillator	
Symbol	Parameter	Min	Max	Min	Мах	Units
1/t _{CLCL}	Oscillator Frequency			0	33	MHz
t _{LHLL}	ALE Pulse Width	127		2t _{CLCL} -40		ns
t _{AVLL}	Address Valid to ALE Low	43		t _{CLCL} -25		ns
t _{LLAX}	Address Hold After ALE Low	48		t _{CLCL} -25		ns
t _{LLIV}	ALE Low to Valid Instruction In		233		4t _{CLCL} -65	ns
t _{LLPL}	ALE Low to PSEN Low	43		t _{CLCL} -25		ns
t _{PLPH}	PSEN Pulse Width	205		3t _{CLCL} -45		ns
t _{PLIV}	PSEN Low to Valid Instruction In		145		3t _{CLCL} -60	ns
t _{PXIX}	Input Instruction Hold After PSEN	0		0		ns
t _{PXIZ}	Input Instruction Float After PSEN		59		t _{CLCL} -25	ns
t _{PXAV}	PSEN to Address Valid	75		t _{CLCL} -8		ns
t _{AVIV}	Address to Valid Instruction In		312		5t _{CLCL} -80	ns
t _{PLAZ}	PSEN Low to Address Float		10		10	ns
t _{RLRH}	RD Pulse Width	400		6t _{CLCL} -100		ns
t _{wLWH}	WR Pulse Width	400		6t _{CLCL} -100		ns
t _{RLDV}	RD Low to Valid Data In		252		5t _{CLCL} -90	ns
t _{RHDX}	Data Hold After RD	0		0		ns
t _{RHDZ}	Data Float After RD		97		2t _{CLCL} -28	ns
t _{LLDV}	ALE Low to Valid Data In		517		8t _{CLCL} -150	ns
t _{AVDV}	Address to Valid Data In		585		9t _{CLCL} -165	ns
t _{LLWL}	ALE Low to RD or WR Low	200	300	3t _{CLCL} -50	3t _{CLCL} +50	ns
t _{AVWL}	Address to RD or WR Low	203		4t _{CLCL} -75		ns
t _{QVWX}	Data Valid to WR Transition	23		t _{CLCL} -30		ns
t _{QVWH}	Data Valid to WR High	433		7t _{CLCL} -130		ns
t _{WHQX}	Data Hold After WR	33		t _{CLCL} -25		ns
t _{RLAZ}	RD Low to Address Float		0		0	ns
t _{wn n}	RD or WR High to ALE High	43	123	t _{ci ci} -25	t _{ci ci} +25	ns

28.1 External Program and Data Memory Characteristics

29. External Program Memory Read Cycle



30. External Data Memory Read Cycle







31. External Data Memory Write Cycle



32. External Clock Drive Waveforms



33. External Clock Drive

Symbol	Parameter	Min	Мах	Units
1/t _{CLCL}	Oscillator Frequency	0	33	MHz
t _{CLCL}	Clock Period	30		ns
t _{CHCX}	High Time	12		ns
t _{CLCX}	Low Time	12		ns
t _{CLCH}	Rise Time		5	ns
t _{CHCL}	Fall Time		5	ns

34. Serial Port Timing: Shift Register Mode Test Conditions

		12 MI	Iz Osc	Variable Oscillator		
Symbol	Parameter	Min	Max	Min	Мах	Units
t _{XLXL}	Serial Port Clock Cycle Time	1.0		12 t _{CLCL}		μs
t _{QVXH}	Output Data Setup to Clock Rising Edge	700		10 t _{CLCL} -133		ns
t _{XHQX}	Output Data Hold After Clock Rising Edge	50		2 t _{CLCL} -80		ns
t _{XHDX}	Input Data Hold After Clock Rising Edge	0		0		ns
t _{XHDV}	Clock Rising Edge to Input Data Valid		700		10 t _{CLCL} -133	ns

The values in this table are valid for V_{CC} = 4.0V to 5.5V and Load Capacitance = 80 pF.

35. Shift Register Mode Timing Waveforms



36. AC Testing Input/Output Waveforms⁽¹⁾



Note: 1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

37. Float Waveforms⁽¹⁾



Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.



39. Packaging Information

39.1 44A – TQFP





39.3 40P6 – PDIP







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