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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	5
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 4x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.154", 3.90mm Width)
Supplier Device Package	8-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12lf1840-i-sn

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 2	2		1			1	1		1		
10Ch	LATA	_	_	LATA5	LATA4	_	LATA2	LATA1	LATA0	xx -xxx	uu -uuu
10Dh to 110h	_	Unimplement	ted							_	_
111h	CM1CON0	C10N	C10UT	C10E	C1POL	_	C1SP	C1HYS	C1SYNC	0000 -100	0000 -100
112h	CM1CON1	C1INTP	C1INTN	C1PCH	H<1:0>	_	_		C1NCH	00000	00000
113h	—	Unimplement	ted	•		•				_	
114h	—	Unimplement	ted							_	
115h	CMOUT	_	_	_	_	_	_		MC10UT	0	0
116h	BORCON	SBOREN	BORFS	_	_	_	_		BORRDY	10q	uuu
117h	FVRCON	FVREN	FVRRDY	TSEN	TSRNG	CDAFV	/R<1:0>	ADFV	R<1:0>	0q00 0000	0q00 0000
118h	DACCON0	DACEN	ACEN DACLPS DACOE — DACPSS<1:0> — —				000- 00	000- 00			
119h	DACCON1	_	— — — DACR<4:0>				0 0000	0 0000			
11Ah	SRCON0	SRLEN		SRCLK<2:0>		SRQEN	SRNQEN	SRPS	SRPR	0000 0000	0000 0000
11Bh	SRCON1	SRSPE	SRSCKE	Reserved	SRSC1E	SRRPE	SRRCKE	Reserved	SRRC1E	0000 0000	0000 0000
11Ch	—	Unimplemented							_	_	
11Dh	APFCON	RXDTSEL	SDOSEL	SSSEL		T1GSEL	TXCKSEL	P1BSEL	CCP1SEL	000- 0000	000- 0000
11Eh	_	Unimplement	Jnimplemented							_	_
11Fh	—	Unimplement	Jnimplemented							_	
Bank 3	3										
18Ch	ANSELA	_	_		ANSA4	_	ANSA2	ANSA1	ANSA0	1 -111	1 -111
18Dh to 190h	_	Unimplement	ted		•		•		1	_	_
191h	EEADRL	EEPROM/Pro	ogram Memor	y Address Reg	ister Low Byte	9				0000 0000	0000 0000
192h	EEADRH	(3)	EEPROM / P	rogram Memo	ry Address Re	egister High B	syte			1000 0000	1000 0000
193h	EEDATL	EEPROM/Pro	ogram Memor	y Read Data R	legister Low B	syte				xxxx xxxx	uuuu uuuu
194h	EEDATH	—	—	EEPROM / P	rogram Memo	ry Read Data	Register Hig	jh Byte		xx xxxx	uu uuuu
195h	EECON1	EEPGD	CFGS	LWLO	FREE	WRERR	WREN	WR	RD	0000 x000	0000 q000
196h	EECON2	EEPROM co	ntrol register 2	2						0000 0000	0000 0000
197h	VREGCON ⁽²⁾	_	_	_	_	_	_	VREGPM	Reserved	01	01
198h	—	Unimplement	ted							_	_
199h	RCREG	USART Rece	eive Data Regi	ster						0000 0000	0000 0000
19Ah	TXREG	USART Trans	smit Data Reg	ister						0000 0000	0000 0000
19Bh	SPBRGL	Baud Rate G	enerator Data	Register Low						0000 0000	0000 0000
19Ch	SPBRGH	Baud Rate G	enerator Data	Register High						0000 0000	0000 0000
19Dh	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000x
19Eh	TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	0000 0010	0000 0010
19Fh	BAUDCON	ABDOVF	RCIDL		SCKP	BRG16		WUE	ABDEN	01-0 0-00	01-0 0-00

TADIE 2 6. EUNICTION DECISTED SUMMARY (CONTINUED) ODECIAL

x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, r = reserved. Shaded locations are unimplemented, read as '0'. Legend:

Note 1: These registers can be addressed from any bank.

PIC12F1840 only. 2:

3: Unimplemented, read as '1'.





3.5.2 OVERFLOW/UNDERFLOW RESET

If the STVREN bit in Configuration Words is programmed to '1', the device will be reset if the stack is PUSHed beyond the sixteenth level or POPed beyond the first level, setting the appropriate bits (STKOVF or STKUNF, respectively) in the PCON register.

3.6 Indirect Addressing

The INDFn registers are not physical registers. Any instruction that accesses an INDFn register actually accesses the register at the address specified by the File Select Registers (FSR). If the FSRn address specifies one of the two INDFn registers, the read will return '0' and the write will not occur (though Status bits may be affected). The FSRn register value is created by the pair FSRnH and FSRnL.

The FSR registers form a 16-bit address that allows an addressing space with 65536 locations. These locations are divided into three memory regions:

- Traditional Data Memory
- · Linear Data Memory
- Program Flash Memory

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0			
	_			TUN	<5:0>					
bit 7							bit 0			
Legend:										
R = Readable	bit	W = Writable	bit	U = Unimplemented bit, read as '0'						
u = Bit is unch	anged	x = Bit is unkr	nown	-n/n = Value at POR and BOR/Value at all other Rese						
'1' = Bit is set		'0' = Bit is clea	ared							
bit 7-6	Unimpleme	nted: Read as '	0'							
bit 5-0	TUN<5:0>: Frequency Tuning bits									
	100000 = N	linimum frequer	ncy							
	•									
	•									
	•									
	111111									
	000000 = O	scillator module	e is running at	the factory-call	brated frequen	су.				
	•									
	-									
	011111 = N	laximum freque	ncv							
	~ <u> </u>		,							

REGISTER 5-3: OSCTUNE: OSCILLATOR TUNING REGISTER

TABLE 5-2. JUIVIIVIANT OF REGISTERS ASSOCIATED WITH CLOCK SOURCE	TABLE 5-2:	SUMMARY OF REGISTERS ASSOCIATED WITH CLOCK SOURCES
--	------------	--

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
OSCCON	SPLLEN		IRCF	<3:0>		—	SCS	53	
OSCSTAT	T10SCR	PLLR	OSTS	HFIOFR	HFIOFL	MFIOFR	LFIOFR	HFIOFS	54
OSCTUNE	_	-		TUN<5:0>					
PIE2	OSFIE		C1IE	EEIE	BCL1IE	_		_	74
PIR2	OSFIF		C1IF	EEIF	BCL1IF				76
T1CON	TMR1C	S<1:0>	T1CKP	S<1:0>	T10SCEN	T1SYNC	_	TMR10N	154

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by clock sources.

TABLE 5-3: SUMMARY OF CONFIGURATION WORD WITH CLOCK SOURCES

Name	Bits	Bit -/7	Bit -/6	Bit 13/5	Bit 12/4	Bit 11/3	Bit 10/2	Bit 9/1	Bit 8/0	Register on Page
0015104	13:8	_	—	FCMEN	IESO	CLKOUTEN	BOREN<1:0> CF		CPD	
CONFIGT	7:0	CP	MCLRE	PWRTE	WDTE<1:0> FOSC<2:0>			33		

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by clock sources.

TABLE 10-3:	SUMMARY OF REGISTERS ASSOCIATED WITH WATCHDOG TIMER
-------------	---

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
OSCCON	SPLLEN		IRCF	<3:0>		—	SCS<1:0>		53
STATUS	—	—	—	TO	PD	Z	DC	С	15
WDTCON	—	—		١	WDTPS<4:0	>		SWDTEN	83

TABLE 10-4: SUMMARY OF CONFIGURATION WORD WITH WATCHDOG TIMER

Name	Bits	Bit -/7	Bit -/6	Bit 13/5	Bit 12/4	Bit 11/3	Bit 10/2	Bit 9/1	Bit 8/0	Register on Page
	13:8	_	—	FCMEN	IESO	CLKOUTEN	BOREN<1:0> -		—	22
CONFIGT	7:0	CP	MCLRE	PWRTE	WDTE<1:0>		FOSC<2:0>			- 33

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by Watchdog Timer.

13.6 Register Definitions: Interrupt-on-Change Control

REGISTER 13-1: IOCAP: INTERRUPT-ON-CHANGE PORTA POSITIVE EDGE REGISTER

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0			
—	—	IOCAP5	IOCAP4	IOCAP3	IOCAP2	IOCAP1	IOCAP0			
bit 7	•					•	bit 0			
Legend:										
R = Readable b	R = Readable bit W = Writable bit			U = Unimplemented bit, read as '0'						
u = Bit is unchanged x = Bit is unknown			own	-n/n = Value at POR and BOR/Value at all other Resets						
'1' = Bit is set '0' = Bit is cleared			ired							

bit 7-6 Unimplemented: Read as '0'

bit 5-0 IOCAP<5:0>: Interrupt-on-Change PORTA Positive Edge Enable bits

- 1 = Interrupt-on-Change enabled on the pin for a positive going edge. Associated Status bit and interrupt flag will be set upon detecting an edge.
- 0 = Interrupt-on-Change disabled for the associated pin.

REGISTER 13-2: IOCAN: INTERRUPT-ON-CHANGE PORTA NEGATIVE EDGE REGISTER

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	IOCAN5	IOCAN4	IOCAN3	IOCAN2	IOCAN1	IOCAN0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 Unimplemented: Read as '0'

bit 5-0

bit 5-0

- **IOCAN<5:0>:** Interrupt-on-Change PORTA Negative Edge Enable bits 1 = Interrupt-on-Change enabled on the pin for a negative going edge. Associated Status bit and interrupt
 - flag will be set upon detecting an edge.
- 0 = Interrupt-on-Change disabled for the associated pin.

REGISTER 13-3: IOCAF: INTERRUPT-ON-CHANGE PORTA FLAG REGISTER

U-0	U-0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0
—	—	IOCAF5	IOCAF4	IOCAF3	IOCAF2	IOCAF1	IOCAF0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HS - Bit is set in hardware

bit 7-6 Unimplemented: Read as '0'

IOCAF<5:0>: Interrupt-on-Change PORTA Flag bits

- 1 = An enabled change was detected on the associated pin.
 - Set when IOCAPx = 1 and a rising edge was detected on RAx, or when IOCANx = 1 and a falling edge was detected on RAx.
 - 0 = No change was detected, or the user cleared the detected change.

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ADCON0	—			CHS<4:0>			GO/DONE	ADON	120
ADCON1	ADFM		ADCS<2:0>		—	—	ADPRE	F<1:0>	121
ADRESH	ADC Result	Register Hig	h						122, 123
ADRESL	ADC Result	Register Lov	v						122, 123
ANSELA	—	—	—	ANSA4	—	ANSA2	ANSA1	ANSA0	103
CCP1CON	P1M·	<1:0>	DC1E	8<1:0>	<1:0> CCP1M<3:0>				
DACCON0	DACEN	DACLPS	DACOE	—	DACPS	SS<1:0>	—	—	130
DACCON1	—	—	—			DACR<4:0>			130
FVRCON	FVREN	FVRRDY	TSEN	TSRNG	CDAFVR<1:0> ADFVR<1:0>			R<1:0>	111
INTCON	GIE	PEIE	TMR0IE	INTE	IOCE	TMR0IF	INTF	IOCF	72
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	73
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	75
TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	102

TABLE 16-3: SUMMARY OF REGISTERS ASSOCIATED WITH ADC

Legend: — = unimplemented read as '0'. Shaded cells are not used for ADC module.

20.0 TIMER0 MODULE

The Timer0 module is an 8-bit timer/counter with the following features:

- 8-bit timer/counter register (TMR0)
- 8-bit prescaler (independent of Watchdog Timer)
- · Programmable internal or external clock source
- · Programmable external clock edge selection
- · Interrupt on overflow
- TMR0 can be used to gate Timer1

Figure 20-1 is a block diagram of the Timer0 module.

20.1 Timer0 Operation

The Timer0 module can be used as either an 8-bit timer or an 8-bit counter.

20.1.1 8-BIT TIMER MODE

The Timer0 module will increment every instruction cycle, if used without a prescaler. 8-bit Timer mode is selected by clearing the TMR0CS bit of the OPTION_REG register.

When TMR0 is written, the increment is inhibited for two instruction cycles immediately following the write.

Note:	The value written to the TMR0 register
	can be adjusted, in order to account for
	the two instruction cycle delay when
	TMR0 is written.

20.1.2 8-BIT COUNTER MODE

In 8-Bit Counter mode, the Timer0 module will increment on every rising or falling edge of the T0CKI pin or the Capacitive Sensing Oscillator (CPSCLK) signal.

8-Bit Counter mode using the T0CKI pin is selected by setting the TMR0CS bit in the OPTION_REG register to '1' and resetting the T0XCS bit in the CPSCON0 register to '0'.

8-Bit Counter mode using the Capacitive Sensing Oscillator (CPSCLK) signal is selected by setting the TMR0CS bit in the OPTION_REG register to '1' and setting the T0XCS bit in the CPSCON0 register to '1'.

The rising or falling transition of the incrementing edge for either input source is determined by the TMR0SE bit in the OPTION_REG register.



R/W-x/u	R/W-x/u	R/W-x/u	U-0	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
MDCHODIS	MDCHPOL	MDCHSYNC	_		MDCH	l<3:0>	
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable I	bit	U = Unimplen	nented bit, read	as '0'	
u = Bit is uncha	anged	x = Bit is unkn	own	-n/n = Value a	t POR and BO	R/Value at all c	ther Resets
'1' = Bit is set		'0' = Bit is clea	ared				
bit 7	MDCHODIS	Modulator High	n Carrier Outp	out Disable bit			
	1 = Output s	ignal driving the	e peripheral o peripheral o	utput pin (selec	ted by MDCH<	3:0>) is disable	ed d
bit 6		Modulator High	Carrier Polar	ity Select hit		0.0×) 13 Chabic	u
bit o	1 = Selected	high carrier sig	nal is inverte	d			
	0 = Selected	high carrier sig	nal is not inv	erted			
bit 5	MDCHSYNC	: Modulator Hig	h Carrier Syr	hchronization Er	nable bit		
	1 = Modulat	or waits for a fa	lling edge on	the high time of	arrier signal be	fore allowing a	a switch to the
	low time	carrier	ovpobropizor	to the high tim		(1)	
hit 4			synchionized	a to the high tim	e carrier signal	()	
DIL 4		Medulatar Data) Lligh Corrier	Coloction hito (1)		
DIE 3-0	MDCH<3:0>		High Carrier		- /		
	•	erveu. No char	iner connecte	eu.			
	•						
	•						
	0101 = Res	erved. No char	nel connecte	ed.			
	0100 = CCI	- I output (PVVIV	odule signal (
	0011 - Rei0010 = MD	CIN2 port pin	ouule signal (
	0001 = MD	CIN1 port pin					
	0000 = Vss						

REGISTER 23-3: MDCARH: MODULATION HIGH CARRIER CONTROL REGISTER

Note 1: Narrowed carrier pulse widths or spurs may occur in the signal stream if the carrier is not synchronized.

24.3.2 SETUP FOR PWM OPERATION

The following steps should be taken when configuring the CCP1 module for standard PWM operation:

- 1. Disable the CCP1 pin output driver by setting the associated TRIS bit.
- 2. Load the PR2 register with the PWM period value.
- Configure the CCP1 module for the PWM mode by loading the CCP1CON register with the appropriate values.
- Load the CCPR1L register and the DC1B1 bits of the CCP1CON register, with the PWM duty cycle value.
- 5. Configure and start Timer2:
 - Clear the TMR2IF interrupt flag bit of the PIR1 register. See Note below.
 - Configure the T2CKPS bits of the T2CON register with the Timer prescale value.
 - Enable the Timer by setting the TMR2ON bit of the T2CON register.
- 6. Enable PWM output pin:
 - Wait until the Timer overflows and the TMR2IF bit of the PIR1 register is set. See Note below.
 - Enable the CCP1 pin output driver by clearing the associated TRIS bit.
 - **Note:** In order to send a complete duty cycle and period on the first PWM output, the above steps must be included in the setup sequence. If it is not critical to start with a complete PWM signal on the first output, then step 6 may be ignored.

24.3.3 PWM PERIOD

The PWM period is specified by the PR2 register of Timer2. The PWM period can be calculated using the formula of Equation 24-1.

EQUATION 24-1: PWM PERIOD

 $PWM Period = [(PR2) + 1] \bullet 4 \bullet Tosc \bullet$ (TMR2 Prescale Value)

Note 1: Tosc = 1/Fosc

When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

- TMR2 is cleared
- The CCP1 pin is set. (Exception: If the PWM duty cycle = 0%, the pin will not be set.)
- The PWM duty cycle is latched from CCPR1L into CCPR1H.

Note: The Timer postscaler (see Section 22.1 "Timer2 Operation") is not used in the determination of the PWM frequency.

24.3.4 PWM DUTY CYCLE

The PWM duty cycle is specified by writing a 10-bit value to multiple registers: CCPR1L register and DC1B<1:0> bits of the CCP1CON register. The CCPR1L contains the eight MSbs and the DC1B<1:0> bits of the CCP1CON register contain the two LSbs. CCPR1L and DC1B<1:0> bits of the CCP1CON register can be written to at any time. The duty cycle value is not latched into CCPR1H until after the period completes (i.e., a match between PR2 and TMR2 registers occurs). While using the PWM, the CCPR1H register is read-only.

Equation 24-2 is used to calculate the PWM pulse width.

Equation 24-3 is used to calculate the PWM duty cycle ratio.

EQUATION 24-2: PULSE WIDTH

$$Pulse Width = (CCPR1L:CCP1CON < 5:4>) \bullet$$

TOSC • (TMR2 Prescale Value)

EQUATION 24-3: DUTY CYCLE RATIO

 $Duty Cycle Ratio = \frac{(CCPR1L:CCP1CON < 5:4>)}{4(PR2 + 1)}$

The CCPR1H register and a 2-bit internal latch are used to double buffer the PWM duty cycle. This double buffering is essential for glitchless PWM operation.

The 8-bit timer TMR2 register is concatenated with either the 2-bit internal system clock (Fosc), or 2 bits of the prescaler, to create the 10-bit time base. The system clock is used if the Timer2 prescaler is set to 1:1.

When the 10-bit time base matches the CCPR1H and 2-bit latch, then the CCP1 pin is cleared (see Figure 24-4).

FIGURE 25-4: SPI MASTER AND MULTIPLE SLAVE CONNECTION



25.2.1 SPI MODE REGISTERS

The MSSP1 module has five registers for SPI mode operation. These are:

- MSSP1 STATUS register (SSP1STAT)
- MSSP1 Control register 1 (SSP1CON1)
- MSSP1 Control register 3 (SSP1CON3)
- MSSP1 Data Buffer register (SSP1BUF)
- MSSP1 Address register (SSP1ADD)
- MSSP1 Shift register (SSP1SR) (Not directly accessible)

SSP1CON1 and SSP1STAT are the control and STATUS registers in SPI mode operation. The SSP1CON1 register is readable and writable. The lower 6 bits of the SSP1STAT are read-only. The upper two bits of the SSP1STAT are read/write.

In one SPI master mode, SSP1ADD can be loaded with a value used in the Baud Rate Generator. More information on the Baud Rate Generator is available in **Section 25.7 "Baud Rate Generator"**.

SSP1SR is the shift register used for shifting data in and out. SSP1BUF provides indirect access to the SSP1SR register. SSP1BUF is the buffer register to which data bytes are written, and from which data bytes are read.

In receive operations, SSP1SR and SSP1BUF together create a buffered receiver. When SSP1SR receives a complete byte, it is transferred to SSP1BUF and the SSP1IF interrupt is set.

During transmission, the SSP1BUF is not buffered. A write to SSP1BUF will write to both SSP1BUF and SSP1SR.

25.2.2 SPI MODE OPERATION

When initializing the SPI, several options need to be specified. This is done by programming the appropriate control bits (SSP1CON1<5:0> and SSP1STAT<7:6>). These control bits allow the following to be specified:

- Master mode (SCK1 is the clock output)
- Slave mode (SCK1 is the clock input)
- Clock Polarity (Idle state of SCK1)
- Data Input Sample Phase (middle or end of data output time)
- Clock Edge (output data on rising/falling edge of SCK1)
- · Clock Rate (Master mode only)
- Slave Select mode (Slave mode only)

To enable the serial port, SSP1 Enable bit, SSP1EN of the SSP1CON1 register must be set. To reset or reconfigure SPI mode, clear the SSP1EN bit, re-initialize the SSP1CONx registers and then set the SSP1EN bit. This configures the SDI, SDO, SCK and SS pins as serial port pins. For the pins to behave as the serial port function, some must have their data direction bits (in the TRIS register) appropriately programmed as follows:

- · SDI must have corresponding TRIS bit set
- SDO must have corresponding TRIS bit cleared
- SCK (Master mode) must have corresponding
 TRIS bit cleared
- SCK (Slave mode) must have corresponding
 TRIS bit set
- SS must have corresponding TRIS bit set

Any serial port function that is not desired may be overridden by programming the corresponding data direction (TRIS) register to the opposite value.

The MSSP1 consists of a transmit/receive shift register (SSP1SR) and a buffer register (SSP1BUF). The SSP1SR shifts the data in and out of the device, MSb first. The SSP1BUF holds the data that was written to the SSP1SR until the received data is ready. Once the 8 bits of data have been received, that byte is moved to the SSP1BUF register. Then, the Buffer Full Detect bit, BF of the SSP1STAT register, and the interrupt flag bit, SSP1IF, are set. This double-buffering of the received data (SSP1BUF) allows the next byte to start reception before reading the data that was just received. Any SSP1BUF the write to register during transmission/reception of data will be ignored and the write collision detect bit, WCOL, of the SSP1CON1 register, will be set. User software must clear the WCOL bit to allow the following write(s) to the SSP1BUF register to complete successfully.

When the application software is expecting to receive valid data, the SSP1BUF should be read before the next byte of data to transfer is written to the SSP1BUF. The Buffer Full bit, BF of the SSP1STAT register, indicates when SSP1BUF has been loaded with the received data (transmission is complete). When the SSP1BUF is read, the BF bit is cleared. This data may be irrelevant if the SPI is only a transmitter. Generally, the MSSP1 interrupt is used to determine when the transmission/reception has completed. If the interrupt method is not going to be used, then software polling can be done to ensure that a write collision does not occur.

The SSP1SR is not directly readable or writable and can only be accessed by addressing the SSP1BUF register. Additionally, the SSP1STAT register indicates the various Status conditions.

25.6 I²C MASTER MODE

Master mode is enabled by setting and clearing the appropriate SSPM bits in the SSP1CON1 register and by setting the SSPEN bit. In Master mode, the SDA and SCK pins must be configured as inputs. The MSSP peripheral hardware will override the output driver TRIS controls when necessary to drive the pins low.

Master mode of operation is supported by interrupt generation on the detection of the Start and Stop conditions. The Stop (P) and Start (S) bits are cleared from a Reset or when the MSSP1 module is disabled. Control of the I^2C bus may be taken when the P bit is set, or the bus is Idle.

In Firmware Controlled Master mode, user code conducts all I²C bus operations based on Start and Stop bit condition detection. Start and Stop condition detection is the only active circuitry in this mode. All other communication is done by the user software directly manipulating the SDA and SCL lines.

The following events will cause the SSP1 Interrupt Flag bit, SSP1IF, to be set (SSP1 interrupt, if enabled):

- Start condition detected
- Stop condition detected
- Data transfer byte transmitted/received
- Acknowledge transmitted/received
- Repeated Start generated
 - **Note 1:** The MSSP1 module, when configured in I²C Master mode, does not allow queuing of events. For instance, the user is not allowed to initiate a Start condition and immediately write the SSP1BUF register to initiate transmission before the Start condition is complete. In this case, the SSP1BUF will not be written to and the WCOL bit will be set, indicating that a write to the SSP1BUF did not occur
 - 2: When in Master mode, Start/Stop detection is masked and an interrupt is generated when the SEN/PEN bit is cleared and the generation is complete.

25.6.1 I²C MASTER MODE OPERATION

The master device generates all of the serial clock pulses and the Start and Stop conditions. A transfer is ended with a Stop condition or with a Repeated Start condition. Since the Repeated Start condition is also the beginning of the next serial transfer, the I²C bus will not be released.

In Master Transmitter mode, serial data is output through SDA, while SCL outputs the serial clock. The first byte transmitted contains the slave address of the receiving device (7 bits) and the Read/Write (R/W) bit. In this case, the R/W bit will be logic '0'. Serial data is transmitted eight bits at a time. After each byte is transmitted, an Acknowledge bit is received. Start and Stop conditions are output to indicate the beginning and the end of a serial transfer.

In Master Receive mode, the first byte transmitted contains the slave address of the transmitting device (7 bits) and the R/W bit. In this case, the R/W bit will be logic '1'. Thus, the first byte transmitted is a 7-bit slave address followed by a '1' to indicate the receive bit. Serial data is received via SDA, while SCL outputs the serial clock. Serial data is received 8 bits at a time. After each byte is received, an Acknowledge bit is transmitted. Start and Stop conditions indicate the beginning and end of transmission.

A Baud Rate Generator is used to set the clock frequency output on SCL. See **Section 25.7 "Baud Rate Generator"** for more detail.

26.4.2 AUTO-BAUD OVERFLOW

During the course of automatic baud detection, the ABDOVF bit of the BAUDCON register will be set if the baud rate counter overflows before the fifth rising edge is detected on the RX pin. The ABDOVF bit indicates that the counter has exceeded the maximum count that can fit in the 16 bits of the SPBRGH:SPBRGL register pair. After the ABDOVF bit has been set, the counter continues to count until the fifth rising edge is detected on the RX pin. Upon detecting the fifth RX edge, the hardware will set the RCIF interrupt flag and clear the ABDEN bit of the BAUDCON register. The RCIF flag can be subsequently cleared by reading the RCREG register. The ABDOVF flag of the BAUDCON register can be cleared by software directly.

To terminate the auto-baud process before the RCIF flag is set, clear the ABDEN bit then clear the ABDOVF bit of the BAUDCON register. The ABDOVF bit will remain set if the ABDEN bit is not cleared first.

26.4.3 AUTO-WAKE-UP ON BREAK

During Sleep mode, all clocks to the EUSART are suspended. Because of this, the Baud Rate Generator is inactive and a proper character reception cannot be performed. The Auto-Wake-up feature allows the controller to wake-up due to activity on the RX/DT line. This feature is available only in Asynchronous mode.

The Auto-Wake-up feature is enabled by setting the WUE bit of the BAUDCON register. Once set, the normal receive sequence on RX/DT is disabled, and the EUSART remains in an Idle state, monitoring for a wake-up event independent of the CPU mode. A wake-up event consists of a high-to-low transition on the RX/DT line. (This coincides with the start of a Sync Break or a wake-up signal character for the LIN protocol.)

The EUSART module generates an RCIF interrupt coincident with the wake-up event. The interrupt is generated synchronously to the Q clocks in normal CPU operating modes (Figure 26-7), and asynchronously if the device is in Sleep mode (Figure 26-8). The interrupt condition is cleared by reading the RCREG register.

The WUE bit is automatically cleared by the low-to-high transition on the RX line at the end of the Break. This signals to the user that the Break event is over. At this point, the EUSART module is in Idle mode waiting to receive the next character.

26.4.3.1 Special Considerations

Break Character

To avoid character errors or character fragments during a wake-up event, the wake-up character must be all zeros.

When the wake-up is enabled the function works independent of the low time on the data stream. If the WUE bit is set and a valid non-zero character is received, the low time from the Start bit to the first rising edge will be interpreted as the wake-up event. The remaining bits in the character will be received as a fragmented character and subsequent characters can result in framing or overrun errors.

Therefore, the initial character in the transmission must be all '0's. This must be ten or more bit times, 13-bit times recommended for LIN bus, or any number of bit times for standard RS-232 devices.

Oscillator Start-up Time

Oscillator start-up time must be considered, especially in applications using oscillators with longer start-up intervals (i.e., LP, XT or HS/PLL mode). The Sync Break (or wake-up signal) character must be of sufficient length, and be followed by a sufficient interval, to allow enough time for the selected oscillator to start and provide proper initialization of the EUSART.

WUE Bit

The wake-up event causes a receive interrupt by setting the RCIF bit. The WUE bit is cleared in hardware by a rising edge on RX/DT. The interrupt condition is then cleared in software by reading the RCREG register and discarding its contents.

To ensure that no actual data is lost, check the RCIDL bit to verify that a receive operation is not in process before setting the WUE bit. If a receive operation is not occurring, the WUE bit may then be set just prior to entering the Sleep mode.

27.5 Timer Resources

To measure the change in frequency of the capacitive sensing oscillator, a fixed time base is required. For the period of the fixed time base, the capacitive sensing oscillator is used to clock either Timer0 or Timer1. The frequency of the capacitive sensing oscillator is equal to the number of counts in the timer divided by the period of the fixed time base.

27.6 Fixed Time Base

To measure the frequency of the capacitive sensing oscillator, a fixed time base is required. Any timer resource or software loop can be used to establish the fixed time base. It is up to the end user to determine the method in which the fixed time base is generated.

Note:	The fixed time base can not be generated
	by the timer resource that the capacitive
	sensing oscillator is clocking.

27.6.1 TIMER0

To select Timer0 as the timer resource for the CPS module:

- Set the T0XCS bit of the CPSCON0 register.
- Clear the TMR0CS bit of the OPTION_REG register.

When Timer0 is chosen as the timer resource, the capacitive sensing oscillator will be the clock source for Timer0. Refer to **Section 20.0 "Timer0 Module"** for additional information.

27.6.2 TIMER1

To select Timer1 as the timer resource for the CPS module, set the TMR1CS<1:0> of the T1CON register to '11'. When Timer1 is chosen as the timer resource, the capacitive sensing oscillator will be the clock source for Timer1. Because the Timer1 module has a gate control, developing a time base for the frequency measurement can be simplified by using the Timer0 overflow flag.

It is recommend that the Timer0 overflow flag, in conjunction with the Toggle mode of the Timer1 Gate, be used to develop the fixed time base required by the software portion of the CPS module. Refer to **Section 21.6 "Timer1 Gate**" for additional information.

TABLE 27-2: TIMER1 ENABLE FUNCTION

TMR10N	TMR1GE	Timer1 Operation
0	0	Off
0	1	Off
1	0	On
1	1	Count Enabled by input

27.7 Software Control

The software portion of the CPS module is required to determine the change in frequency of the capacitive sensing oscillator. This is accomplished by the following:

- Setting a fixed time base to acquire counts on Timer0 or Timer1.
- Establishing the nominal frequency for the capacitive sensing oscillator.
- Establishing the reduced frequency for the capacitive sensing oscillator due to an additional capacitive load.
- Set the frequency threshold.

27.7.1 NOMINAL FREQUENCY (NO CAPACITIVE LOAD)

To determine the nominal frequency of the capacitive sensing oscillator:

- Remove any extra capacitive load on the selected CPSx pin.
- At the start of the fixed time base, clear the timer resource.
- At the end of the fixed time base save the value in the timer resource.

The value of the timer resource is the number of oscillations of the capacitive sensing oscillator for the given time base. The frequency of the capacitive sensing oscillator is equal to the number of counts on in the timer, divided by the period of the fixed time base.

27.7.2 REDUCED FREQUENCY (ADDITIONAL CAPACITIVE LOAD)

The extra capacitive load will cause the frequency of the capacitive sensing oscillator to decrease. To determine the reduced frequency of the capacitive sensing oscillator:

- Add a typical capacitive load on the selected CPSx pin.
- Use the same fixed time base as the nominal frequency measurement.
- At the start of the fixed time base, clear the timer resource.
- At the end of the fixed time base, save the value in the timer resource.

The value of the timer resource is the number of oscillations of the capacitive sensing oscillator with an additional capacitive load. The frequency of the capacitive sensing oscillator is equal to the number of counts on in the timer, divided by the period of the fixed time base. This frequency should be less than the value obtained during the nominal frequency measurement.

TABLE 30-14:	SPI MODE	REQUIREMENTS
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Param No.	Symbol	Characteristic	Min.	Тур†	Max.	Units	Conditions	
SP70*	TssL2scH, TssL2scL	SS↓ to SCK↓ or SCK↑ input		2.25 TCY		—	ns	
SP71*	TscH	SCK input high time (Slave mode	e)	TCY + 20	_	—	ns	
SP72*	TscL	SCK input low time (Slave mode)	Tcy + 20	_	—	ns	
SP73*	TDIV2scH, TDIV2scL	Setup time of SDI data input to S	SCK edge	100	_	_	ns	
SP74*	TscH2diL, TscL2diL	Hold time of SDI data input to SCK edge		100	_	—	ns	
SP75*	TDOR	SDO data output rise time	3.0-5.5V	—	10	25	ns	
			1.8-5.5V	—	25	50	ns	
SP76*	TDOF	SDO data output fall time		—	10	25	ns	
SP77*	TssH2doZ	SS↑ to SDO output high-impedance		10	_	50	ns	
SP78*	TscR	SCK output rise time	3.0-5.5V	—	10	25	ns	
		(Master mode)	1.8-5.5V	_	25	50	ns	
SP79*	TscF	SCK output fall time (Master mo	de)	—	10	25	ns	
SP80*	TscH2doV,	SDO data output valid after	3.0-5.5V	—	_	50	ns	
	TscL2doV	SCK edge	1.8-5.5V	_	_	145	ns	
SP81*	TDOV2scH, TDOV2scL	SDO data output setup to SCK edge		Тсу	_	—	ns	
SP82*	TssL2doV	SDO data output valid after $\overline{SS}\downarrow$ edge		_		50	ns	
SP83*	TscH2ssH, TscL2ssH	SS [↑] after SCK edge		1.5Tcy + 40	_	—	ns	

These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

*

31.0 DC AND AC CHARACTERISTICS GRAPHS AND CHARTS

The graphs and tables provided in this section are for design guidance and are not tested.

In some graphs or tables, the data presented are **outside specified operating range** (i.e., outside specified VDD range). This is for **information only** and devices are ensured to operate properly only within the specified range.

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

"Typical" represents the mean of the distribution at 25°C. "MAXIMUM", "Max.", "MINIMUM" or "Min." represents (mean + 3σ) or (mean - 3σ) respectively, where σ is a standard deviation, over each temperature range.

FIGURE 31-7: IDD, EXTERNAL CLOCK (ECL), LOW-POWER MODE, Fosc = 32 kHz, PIC12LF1840 ONLY



FIGURE 31-8: IDD, EXTERNAL CLOCK (ECL), LOW-POWER MODE, Fosc = 32 kHz, PIC12F1840 ONLY









32.11 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM[™] and dsPICDEM[™] demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ[®] security ICs, CAN, IrDA[®], PowerSmart battery management, SEEVAL[®] evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

32.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent[®] and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika[®]

8-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Ν	ILLIMETER	S	
Dimension	MIN	NOM	MAX	
Contact Pitch		0.65 BSC		
Optional Center Pad Width	W2			2.40
Optional Center Pad Length	T2			1.55
Contact Pad Spacing	C1		3.10	
Contact Pad Width (X8)	X1			0.35
Contact Pad Length (X8)	Y1			0.65
Distance Between Pads	G	0.30		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2062B