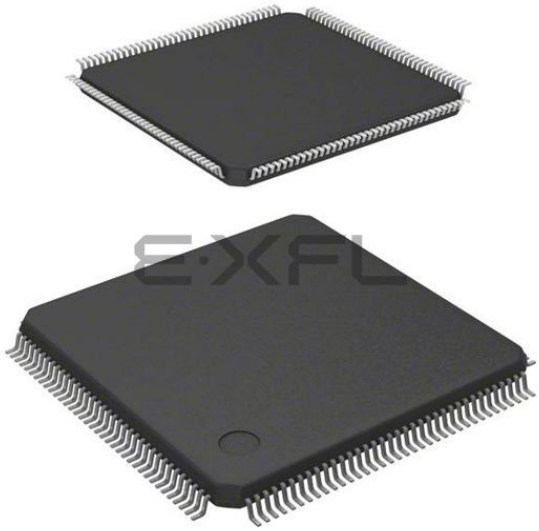

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST10
Core Size	16-Bit
Speed	48MHz
Connectivity	ASC, CANbus, EBI/EMI, I²C, SSC, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	111
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/f271-bag5-t-tr

5.5.6 XBus flash volatile temporary access unprotection register (XFVTAUR0) . 39
5.5.7 Access protection 39
5.5.8 Write protection 40
5.5.9 Temporary unprotection 40
5.6 Write operation examples 41
5.7 Write operation summary 44

6 Bootstrap loader 45
6.1 Selection among user-code, standard or selective bootstrap 45
6.2 Standard bootstrap loader 45
6.3 Alternate and selective boot mode (ABM and SBM) 46
6.3.1 Activation of the ABM and SBM 46
6.3.2 User mode signature integrity check 46
6.3.3 Selective boot mode 46

7 Central processing unit (CPU) 47
7.1 Multiplier-accumulator unit (MAC) 48
7.2 Instruction set summary 49
7.3 MAC co-processor specific instructions 51

8 External bus controller 52

9 Interrupt system 53
9.1 X-Peripheral interrupt 55
9.2 Exception and error traps list 57

10 Capture / compare (CAPCOM) units 58

11 General purpose timer unit 60
11.1 GPT1 60
11.2 GPT2 62

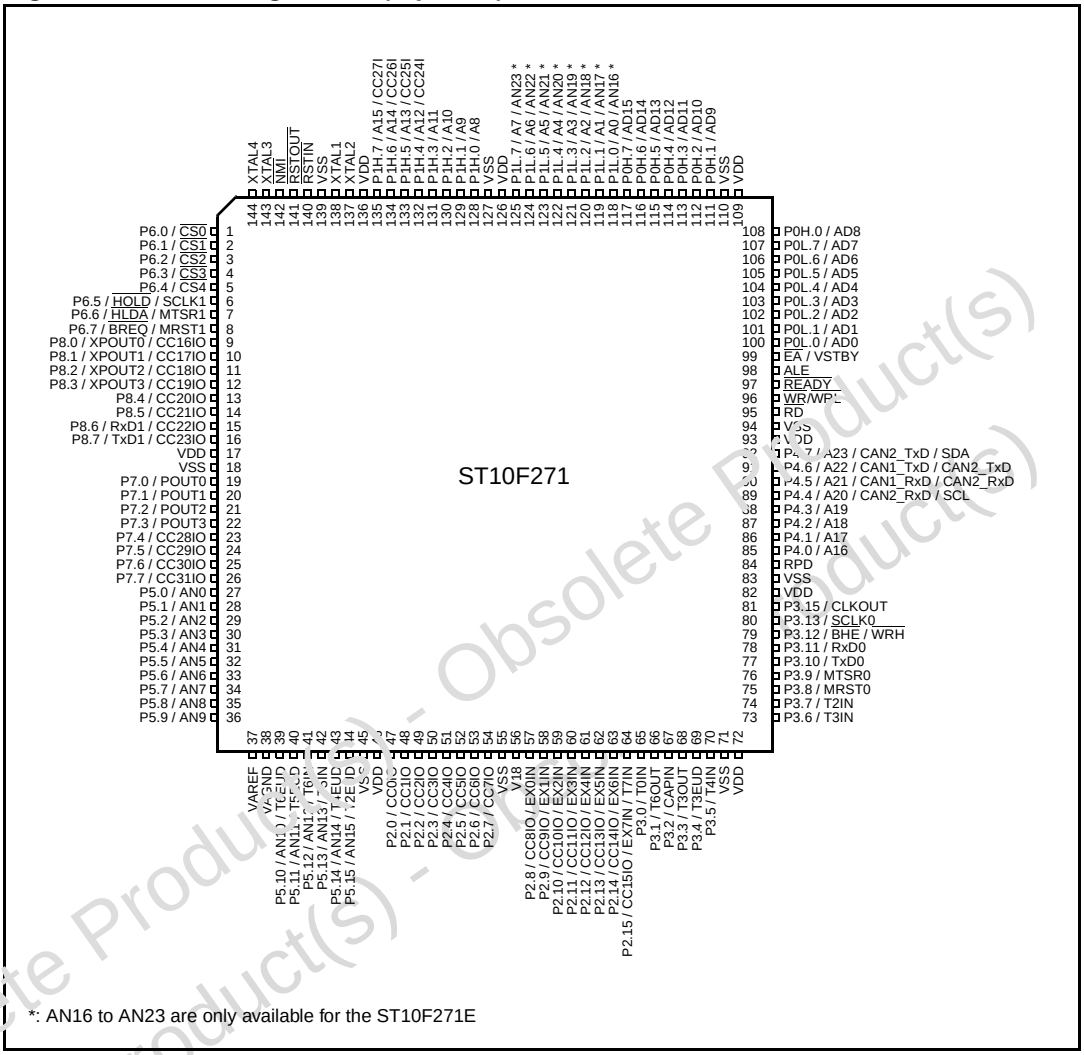
12 PWM modules 64

13 Parallel ports 65
13.1 Introduction 65

Table 48. Reset event definition . . . 80
Table 49. Reset event . . . 103
Table 50. PORT0 latched configuration for the different reset events . . . 104
Table 51. Power reduction modes summary . . . 110
Table 52. List of special function registers . . . 112
Table 53. List of XBus registers . . . 119
Table 54. List of flash registers . . . 124
Table 55. IDMANUF . . . 125
Table 56. IDCHIP . . . 125
Table 57. IDMEM . . . 125
Table 58. IDPROG . . . 126
Table 59. Absolute maximum ratings . . . 127
Table 60. Recommended operating conditions . . . 128
Table 61. Thermal characteristics . . . 129
Table 62. Package characteristics . . . 129
Table 63. DC characteristics . . . 130
Table 64. Flash characteristics . . . 135
Table 65. Flash data retention characteristics . . . 136
Table 66. A/D converter characteristics . . . 136
Table 67. A/D converter programming . . . 138
Table 68. On-chip clock generator selections . . . 147
Table 69. Internal PLL divider mechanism . . . 149
Table 70. PLL characteristics (V_{DD} = 5V ± 10%, V_{SS} = 0V, T_A = –40 to +125°C) . . . 153
Table 71. Main oscillator characteristics . . . 153
Table 72. Main oscillator negative resistance (module) . . . 154
Table 73. 32kHz oscillator characteristics . . . 154
Table 74. Minimum values of negative resistance (module) for 32kHz oscillator . . . 155
Table 75. External clock drive . . . 155
Table 76. Memory cycle variables . . . 156
Table 77. Multiplexed bus timings . . . 157
Table 78. Demultiplexed bus timings . . . 163
Table 79. CLKOUT and READY timings . . . 169
Table 80. External bus arbitration timings . . . 171
Table 81. SSC master mode timings . . . 173
Table 82. SSC slave mode timings . . . 174
Table 83. Order codes . . . 178
Table 84. Document revision history . . . 179

2 Pin data

Figure 2. Pin configuration (top view)



*: AN16 to AN23 are only available for the ST10F271E

Table 1. Pin description (continued)

Symbol	Pin	Type	Function		
P3.0 - P3.5 P3.6 - P3.13, P3.15	65-70, 73-80, 81	I/O I/O I/O	15-bit (P3.14 is missing) bidirectional I/O port, bit-wise programmable for input or output via direction bit. Programming an I/O pin as input forces the corresponding output driver to high impedance state. Port 3 outputs can be configured as push-pull or open drain drivers. The input threshold of Port 3 is selectable (TTL or CMOS). The following Port 3 pins have alternate functions:		
	65	I	P3.0	T0IN	CAPCOM1: timer T0 count input
	66	O	P3.1	T6OUT	GPT2: timer T6 toggle latch output
	67	I	P3.2	CAPIN	GPT2: register CAPREL capture input
	68	O	P3.3	T3OUT	GPT1: timer T3 toggle latch output
	69	I	P3.4	T3EUD	GPT1: timer T3 external up/down control input
	70	I	P3.5	T4IN	GPT1; timer T4 input for count/gate/reload/capture
	73	I	P3.6	T3IN	GPT1: timer T3 count/gate input
	74	I	P3.7	T2IN	GPT1: timer T2 input for count/gate/reload / capture
	75	I/O	P3.8	MRST0	SSC0: master-receiver/slave-transmitter I/O
	76	I/O	P3.9	MTSR0	SSC0: master-transmitter/slave-receiver O/I
	77	O	P3.10	TxD0	ASC0: clock / data output (asynchronous/synchronous)
	78	I/O	P3.11	RxD0	ASC0: data input (asynchronous) or I/O (synchronous)
	79	O	P3.12	$\overline{BHE}$	External memory high byte enable signal
				$\overline{WRH}$	External memory high byte write strobe
	80	I/O	P3.13	SCLK0	SSC0: master clock output / slave clock input
	81	O	P3.15	CLKOUT	System clock output (programmable divider on CPU clock)

5.4.2 Flash control register 0 high

The Flash Control Register 0 High (FCR0H) together with the Flash Control Register 0 Low (FCR0L) is used to enable and to monitor all the write operations on the IFLASH. The user has no access in write mode to the Test-Flash (B0TF). Besides, Test-Flash block is seen by the user in Bootstrap Mode only.

FCR0H (0x08 0002) FCR Reset value: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WMS	SUSP	WPG	DWPG	SER	reserved		SPR	reserved							
RW	RW	RW	RW	RW			RW								

Table 8. Flash control register 0 high

Bit	Function
SPR	Set Protection This bit must be set to select the Set Protection operation. The Set Protection operation allows to program 0s in place of 1s in the Flash Non Volatile Protection Registers. The Flash Address in which to program must be written in the FARH/L registers, while the Flash Data to be programmed must be written in the FDR0H/L before starting the execution by setting bit WMS. A sequence error is flagged by bit SEQER of FER if the address written in FARH/L is not in the range 0x0E8FB0-0x08DFBF. SPR bit is automatically reset at the end of the Set Protection operation.
SER	Sector Erase This bit must be set to select the Sector Erase operation in the Flash modules. The Sector Erase operation allows to erase all the Flash locations to value 0xFF. From 1 to all the sectors of the same Bank (excluded Test-Flash for Bank B0) can be selected to be erased through bits BxFy of FCR1H/L registers before starting the execution by setting bit WMS. It is not necessary to pre-program the sectors to 0x00, because this is done automatically. SER bit is automatically reset at the end of the Sector Erase operation.
DWPG	Double Word Program This bit must be set to select the Double Word (64 bits) Program operation in the Flash module. The Double Word Program operation allows to program 0s in place of 1s. The Flash Address in which to program (aligned with even words) must be written in the FARH/L registers, while the 2 Flash Data to be programmed must be written in the FDR0H/L registers (even word) and FDR1H/L registers (odd word) before starting the execution by setting bit WMS. DWPG bit is automatically reset at the end of the Double Word Program operation.
WPG	Word Program This bit must be set to select the Word (32 bits) Program operation in the Flash module. The Word Program operation allows to program 0s in place of 1s. The Flash Address to be programmed must be written in the FARH/L registers, while the Flash Data to be programmed must be written in the FDR0H/L registers before starting the execution by setting bit WMS. WPG bit is automatically reset at the end of the Word Program operation.

5.4.6 Flash data register 0 high

FDR0H (0x08 000A) FCR Reset value: FFFFh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIN31	DIN30	DIN29	DIN28	DIN27	DIN26	DIN25	DIN24	DIN23	DIN22	DIN21	DIN20	DIN19	DIN18	DIN17	DIN16
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 13. Flash data register 0 high

Bit	Function
DIN(31:16)	Data Input 31:16 These bits must be written with the Data to program the Flash with the following operations: Word Program (32-bit), Double Word Program (64-bit) and Set Protection.

5.4.7 Flash data register 1 low

FDR1L (0x08 000C) FCR Reset value: FFFFh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIN15	DIN14	DIN13	DIN12	DIN11	DIN10	DIN9	DIN8	DIN7	DIN6	DIN5	DIN4	DIN3	DIN2	DIN1	DIN0
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 14. Flash data register 1 low

Bit	Function
DIN(15:0)	Data Input 15:0 These bits must be written with the Data to program the Flash with the following operations: Word Program (32-bit), Double Word Program (64-bit) and Set Protection.

5.4.8 Flash data register 1 high

FDR1H (0x08 000E) FCR Reset value: FFFFh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIN31	DIN30	DIN29	DIN28	DIN27	DIN26	DIN25	DIN24	DIN23	DIN22	DIN21	DIN20	DIN19	DIN18	DIN17	DIN16
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 15. Flash data register 1 high

Bit	Function
DIN(31:16)	Data Input 31:16 These bits must be written with the Data to program the Flash with the following operations: Word Program (32-bit), Double Word Program (64-bit) and Set Protection.

5.5.3 Flash non volatile access protection register 0

FNVAPR0 (0x08 DFB8) NVR Reset value: ACFFh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved														DBGP	ACCP
														RW	RW

Table 20. Flash non volatile access protection register 0

Bit	Function
ACCP	Access Protection This bit, if programmed at 0, disables any access (read/write) to data mapped inside IFlash Module address space, unless the current instruction is fetched from IFlash.
DBGP	Debug Protection This bit, if erased at 1, allows to by-pass all the protections using the Debug features through the Test Interface. If programmed at 0 on the contrary, all the debug features, the Test Interface and all the Flash Test Modes are disabled. Even STMicroelectronics will not be able to access the device to run any eventual failure analysis.

5.5.4 Flash non volatile access protection register 1 low

FNVAPR1L (0x08 DFBC) NVR Delivery value:: FFFFh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PDS15	PDS14	PDS13	PDS12	PDS11	PDS10	PDS9	PDS8	PDS7	PDS6	PDS5	PDS4	PDS3	PDS2	PDS1	PDS0
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 21. Flash non volatile access protection register 1 low

Bit	Function
PDS(15:0)	Protections Disable 15-0 If bit PDSx is programmed at 0 and bit PENx is erased at 1, the action of bit ACCP is disabled. Bit PDS0 can be programmed at 0 only if both bits DBGP and ACCP have already been programmed at 0. Bit PDSx can be programmed at 0 only if bit PENx-1 has already been programmed at 0.

8 External bus controller

All of the external memory accesses are performed by the on-chip external bus controller.

The EBC can be programmed to single chip mode when no external memory is required, or to one of four different external memory access modes:

- 16- / 18- / 20- / 24-bit addresses and 16-bit data, demultiplexed
- 16- / 18- / 20- / 24-bit addresses and 16-bit data, multiplexed
- 16- / 18- / 20- / 24-bit addresses and 8-bit data, multiplexed
- 16- / 18- / 20- / 24-bit addresses and 8-bit data, demultiplexed

In demultiplexed bus modes addresses are output on PORT1 and data is input / output on PORT0 or P0L, respectively. In the multiplexed bus modes both addresses and data use PORT0 for input / output.

Timing characteristics of the external bus interface (memory cycle time, memory tri-state time, length of ALE and read / write delay) are programmable giving the choice of a wide range of memories and external peripherals.

Up to four independent address windows may be defined (using register pairs ADDRSELx / BUSCONx) to access different resources and bus characteristics.

These address windows are arranged hierarchically where BUSCON4 overrides BUSCON3 and BUSCON2 overrides BUSCON1.

All accesses to locations not covered by these four address windows are controlled by BUSCON0. Up to five external $\overline{CS}$ signals (four windows plus default) can be generated in order to save external glue logic. Access to very slow memories is supported by a 'Ready' function.

A $\overline{HOLD}$ / $\overline{HLDA}$ protocol is available for bus arbitration which shares external resources with other bus masters.

The bus arbitration is enabled by setting bit HLDEN in register PSW. After setting HLDEN once, pins P6.7...P6.5 ($\overline{BREQ}$, $\overline{HLDA}$, $\overline{HOLD}$) are automatically controlled by the EBC. In master mode (default after reset) the $\overline{HLDA}$ pin is an output. By setting bit DP6.7 to'1' the slave mode is selected where pin $\overline{HLDA}$ is switched to input. This directly connects the slave controller to another master controller without glue logic.

For applications which require less external memory space, the address space can be restricted to 1 Mbyte, 256 Kbytes or to 64 Kbytes. Port 4 outputs all eight address lines if an address space of 16M Bytes is used, otherwise four, two or no address lines.

Chip select timing can be made programmable. By default (after reset), the $\overline{CSx}$ lines change half a CPU clock cycle after the rising edge of ALE. With the CSCFG bit set in the SYSCON register the $\overline{CSx}$ lines change with the rising edge of ALE.

The active level of the READY pin can be set by bit RDYPOL in the BUSCONx registers. When the READY function is enabled for a specific address window, each bus cycle within the window must be terminated with the active level defined by bit RDYPOL in the associated BUSCON register.

12 PWM modules

Two pulse width modulation modules are available on ST10F271: standard PWM0 and XBus PWM1. They can generate up to four PWM output signals each, using edge-aligned or centre-aligned PWM. In addition, the PWM modules can generate PWM burst signals and single shot outputs. The *Table 38* and *Table 39* show the PWM frequencies for different resolutions. The level of the output signals is selectable and the PWM modules can generate interrupt requests.

Figure 12. Block diagram of PWM module

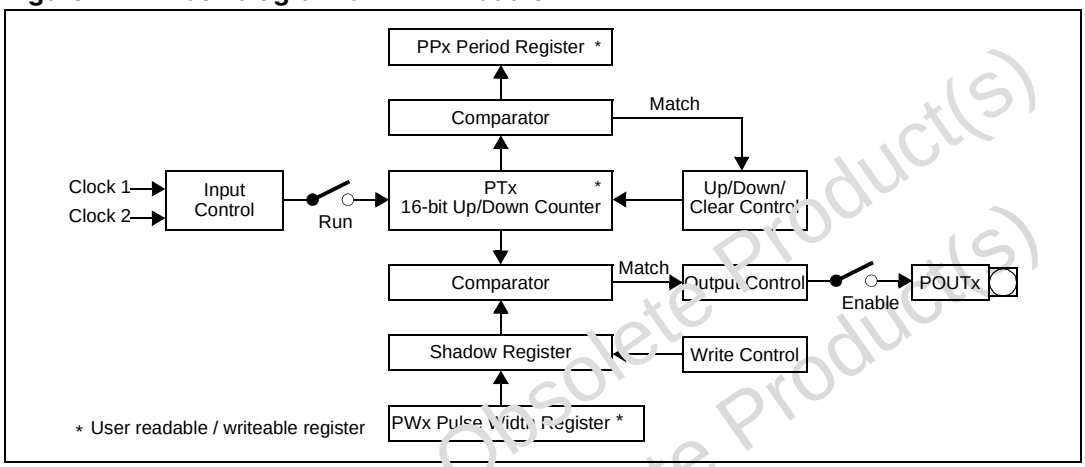


Table 38. PWM unit frequencies and resolutions at 40 MHz CPU clock

Mode 0	Resolution	8-bit	10-bit	12-bit	14-bit	16-bit
CPU Clock/1	25ns	156.25 kHz	39.1 kHz	9.77 kHz	2.44Hz	610Hz
CPU Clock/64	1.6µs	2.44 kHz	610Hz	152.6Hz	38.15Hz	9.54Hz
Mode 1	**Resolution**	**8-bit**	**10-bit**	**12-bit**	**14-bit**	**16-bit**
CPU Clock/1	25ns	78.12 kHz	19.53 kHz	4.88 kHz	1.22 kHz	305.2Hz
CPU Clock/64	1.6µs	1.22 kHz	305.17Hz	76.29Hz	19.07Hz	4.77Hz

Table 39. PWM unit frequencies and resolutions at 64 MHz CPU clock

Mode 0	Resolution	8-bit	10-bit	12-bit	14-bit	16-bit
CPU Clock/1	15.6ns	250 kHz	62.5 kHz	15.63 kHz	3.91Hz	977Hz
CPU Clock/64	1.0µs	3.91 kHz	976.6Hz	244.1Hz	61.01Hz	15.26Hz
Mode 1	**Resolution**	**8-bit**	**10-bit**	**12-bit**	**14-bit**	**16-bit**
CPU Clock/1	15.6ns	125 kHz	31.25 kHz	7.81 kHz	1.95 kHz	488.3Hz
CPU Clock/64	1.0µs	1.95 kHz	488.28Hz	122.07Hz	30.52Hz	7.63Hz

This is done by setting or clearing the direction control bit DPx.y of the pin before enabling the alternate function.

There are port lines, however, where the direction of the port line is switched automatically.

For instance, in the multiplexed external bus modes of PORT0, the direction must be switched several times for an instruction fetch in order to output the addresses and to input the data.

Obviously, this cannot be done through instructions. In these cases, the direction of the port line is switched automatically by hardware if the alternate function of such a pin is enabled.

To determine the appropriate level of the port output latches check how the alternate data output is combined with the respective port latch output.

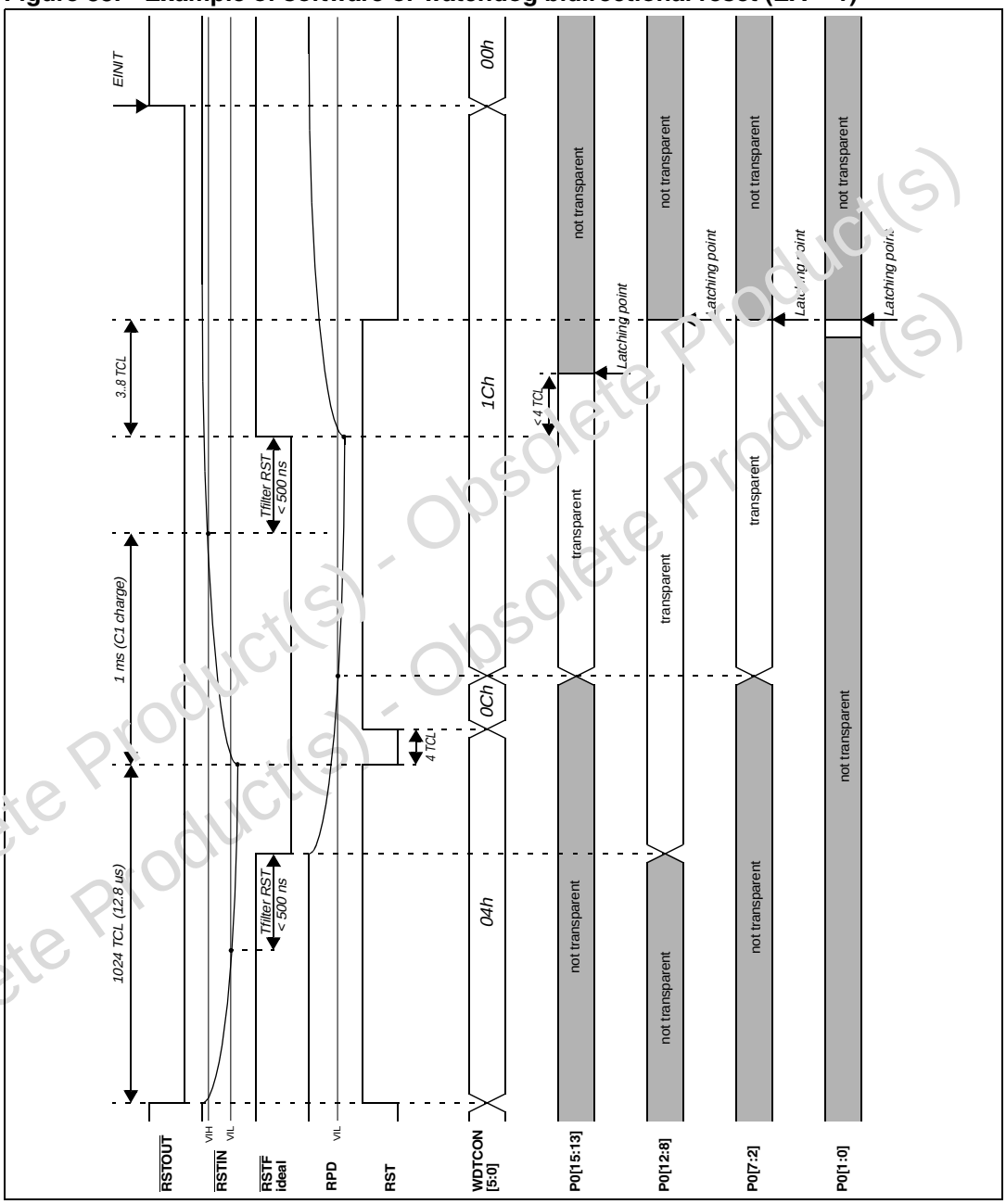
There is one basic structure for all port lines with only an alternate input function. Port lines with only an alternate output function, however, have different structures due to the way the direction of the pin is switched and depending on whether the pin is accessible by the user software or not in the alternate function mode.

All port lines that are not used for these alternate functions may be used as general purpose I/O lines.

20.8 Reset application examples

Next two timing diagrams (*Figure 33* and *Figure 34*) provides additional examples of bidirectional internal reset events (Software and Watchdog) including in particular the external capacitances charge and discharge transients (refer also to *Figure 31* for the external circuit scheme).

Figure 33. Example of software or watchdog bidirectional reset ($\overline{EA}$ = 1)



24.2 Recommended operating conditions

Table 60. Recommended operating conditions

Symbol	Parameter	Value		Unit
		Min	Max	
V_{DD}	Operating supply voltage	4.5	5.5	V
V_{STBY}	Operationg stand-by supply voltage (1)	4.5	5.5	V
V_{AREF}	Operating analog reference voltage (2)			
T_A	Ambient temperature under bias	-40	+125	°C
T_J	Junction temperature under bias	-40	+150	°C

1. The value of the V_{STBY} voltage is specified in the range 4.5 - 5.5 Volt. Nevertheless, it is acceptable to exceed the upper limit (up to 6.0 Volt) for a maximum of 100 hours over the global 300000 hours, representing the lifetime of the device (about 30 years). On the other hand, it is possible to exceed the lower limit (down to 4.0 Volt) whenever RTC and 32kHz on-chip oscillator amplifier are turned off (only Stand-by RAM powered through VSTBY pin in Stand by mode). When VSTBY voltage is lower than main VDD, the input section of VSTBY/EA pin can generate a spurious static consumption on VDD power supply (in the range of tenth of µA).
2. For details on operating conditions concerning the usage of A/D Converter refer to *Section 24.7*.

24.3 Power considerations

The average chip-junction temperature, T_J, in degrees Celsius, may be calculated using the following equation:

$T_J = T_A + (P_D \times \Theta_{JA})$ (1)

Where:

T_A is the Ambient Temperature in °C,

Θ_{JA} is the Package Junction-to-Ambient Thermal Resistance, in °C/W,

P_D is the sum of P_{INT} and $P_{I/O}$ ($P_D = P_{INT} + P_{I/O}$),

P_{INT} is the product of I_{DD} and V_{DD}, expressed in Watt. This is the Chip Internal Power,

$P_{I/O}$ represents the Power Dissipation on Input and Output Pins; User Determined.

Most of the time for the applications $P_{I/O} < P_{INT}$ and may be neglected. On the other hand, $P_{I/O}$ may be significant if the device is configured to drive continuously external modules and/or memories.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is given by:

$P_D = K / (T_J + 273°C)$ (2)

Therefore (solving equations 1 and 2):

$K = P_D \times (T_A + 273°C) + \Theta_{JA} \times P_D^2$ (3)

Where:

K is a constant for the particular part, which may be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J may be obtained by solving equations (1) and (2) iteratively for any value of T_A.

24.5 DC characteristics

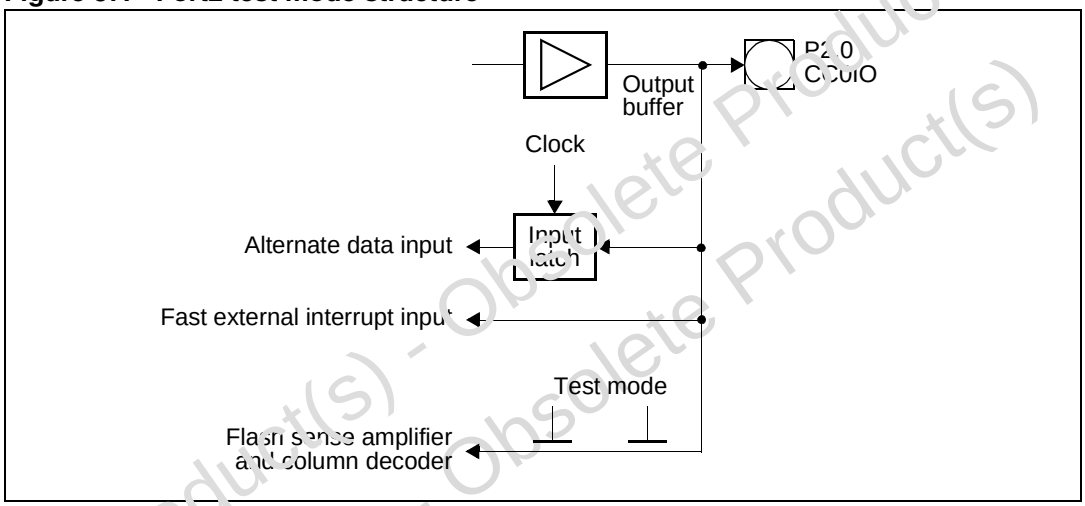
V_{DD} = 5 V ± 10%, V_{SS} = 0 V, T_A = –40 to +125°C

Table 63. DC characteristics

Parameter	Symbol	Limit values		Unit	Test Condition
		min.	max.		
Input low voltage (TTL mode) (except $\overline{RSTIN}$, $\overline{EA}$, $\overline{NMI}$, RPD, XTAL1, READY)	V_{IL} **SR**	– 0.3	0.8	V	–
Input low voltage (CMOS mode) (except $\overline{RSTIN}$, $\overline{EA}$, $\overline{NMI}$, RPD, XTAL1, READY)	V_{ILS} **SR**	– 0.3	0.3 V_{DD}	V	–
Input low voltage $\overline{RSTIN}$, $\overline{EA}$, $\overline{NMI}$, RPD	V_{IL1} **SR**	– 0.3	0.3 V_{DD}	V	–
Input low voltage XTAL1 (CMOS only)	V_{IL2} **SR**	– 0.3	0.3 V_{DD}	V	Direct Drive mode
Input low voltage READY (TTL only)	V_{IL3} **SR**	– 0.3	0.8	V	–
Input high voltage (TTL mode) (except $\overline{RSTIN}$, $\overline{EA}$, $\overline{NMI}$, RPD, XTAL1)	V_{IH} **SR**	2.0	V_{DD} + 0.3	V	–
Input high voltage (CMOS mode) (except $\overline{RSTIN}$, $\overline{EA}$, $\overline{NMI}$, RPD, XTAL1)	V_{IHS} **SR**	0.7 V_{DD}	V_{DD} + 0.3	V	–
Input high voltage $\overline{RSTIN}$, $\overline{EA}$, $\overline{NMI}$, RPD	V_{IH1} **SR**	0.7 V_{DD}	V_{DD} + 0.3	V	–
Input high voltage XTAL1 (CMOS only)	V_{IH2} **SR**	0.7 V_{DD}	V_{DD} + 0.3	V	Direct Drive mode
Input high voltage READY (TTL only)	V_{IH3} **SR**	2.0	V_{DD} + 0.3	V	–
Input Hysteresis (TTL mode) (except $\overline{RSTIN}$, $\overline{EA}$, $\overline{NMI}$, XTAL1, RPD)	V_{HYS} **CC**	400	700	mV	(1)
Input Hysteresis (CMOS mode) (except $\overline{RSTIN}$, $\overline{EA}$, $\overline{NMI}$, XTAL1, RPD)	V_{HYSS} **CC**	750	1400	mV	(1)
Input Hysteresis $\overline{RSTIN}$, $\overline{EA}$, $\overline{NMI}$	V_{HYS1} **CC**	750	1400	mV	(1)
Input Hysteresis XTAL1	V_{HYS2} **CC**	0	50	mV	(1)
Input Hysteresis READY (TTL only)	V_{HYS3} **CC**	400	700	mV	(1)
Input Hysteresis RPD	V_{HYS4} **CC**	500	1500	mV	(1)
Output low voltage (P6[7:0], ALE, $\overline{RD}$, $\overline{WR/WRL}$, $\overline{BHE/WRH}$, CLKOUT, $\overline{RSTIN}$, $\overline{RSTOUT}$)	V_{OL} **CC**	–	0.4 0.05	V	I_{OL} = 8 mA I_{OL} = 1 mA
Output low voltage (P0[15:0], P1[15:0], P2[15:0], P3[15,13:0], P4[7:0], P7[7:0], P8[7:0])	V_{OL1} **CC**	–	0.4 0.05	V	I_{OL1} = 4 mA I_{OL1} = 0.5 mA
Output low voltage RPD	V_{OL2} **CC**	–	V_{DD} 0.5 V_{DD} 0.3 V_{DD}	V	I_{OL2} = 85 µA I_{OL2} = 80 µA I_{OL2} = 60 µA

10. The power supply current is a function of the operating frequency (f_{CPU} is expressed in MHz). This dependency is illustrated in the *Figure 38* below. This parameter is tested at V_{DDmax} and at maximum CPU clock frequency with all outputs disconnected and all inputs at V_{IL} or V_{IH}, RSTIN pin at V_{IH1min}: **this implies I/O current is not considered**. The device is doing the following:
    - *Fetching code from all sectors of IFlash, accessing in read (few fetches) and write to XRAM*
    - *Watchdog Timer is enabled and regularly serviced*
    - *RTC is running with main oscillator clock as reference, generating a tick interrupts every 192 clock cycles*
    - *Four channel of XPWM are running (waves period: 2, 2.5, 3 and 4 CPU clock cycles): no output toggling*
    - *Five General Purpose Timers are running in timer mode with prescaler equal to 8 (T2, T3, T4, T5, T6)*
    - *ADC is in* **Auto Scan Continuous Conversion mode** *on all 16 channels of Port5*
    - *All interrupts generated by XPWM, RTC, Timers and ADC are not serviced*
11. The Idle mode supply current is a function of the operating frequency (f_{CPU} is expressed in MHz). This dependency is illustrated in the *Figure 37* below. These parameters are tested and at maximum CPU clock with all outputs disconnected and all inputs at V_{IL} or V_{IH}, RSTIN pin at V_{IH1min}.
12. This parameter is tested including leakage currents. All inputs (including pins configured as inputs) at 0 V to 0.1 V or at V_{DD} – 0.1 V to V_{DD}, V_{AREF} = 0 V, all outputs (including pins configured as outputs) disconnected. Besides, the Main Voltage Regulator is assumed off: in case it is not, additional 1mA shall be assumed.

Figure 37. Port2 test mode structure



24.6 Flash characteristics

V_{DD} = 5 V ± 10%, V_{SS} = 0 V

Table 64. Flash characteristics

Parameter	Typical	Maximum		Unit	Notes
	T_A = 25°C	T_A = 125°C			
	0 cycles(1)	0 cycles(1)	100k cycles		
Word Program (32-bit) (2)	35	80	290	µs	–
Double Word Program (64-bit)(2))	60	150	570	µs	–
Bank 0 Program (256K) (Double Word Program)	1.6	2.0	3.9	s	–
Sector Erase (8K)	0.6 0.5	0.9 0.8	1.0 0.9	s	not preprogrammed preprogrammed
Sector Erase (32K)	1.1 0.8	2.0 1.8	2.7 2.5	s	not preprogrammed preprogrammed
Sector Erase (64K)	1.7 1.3	3.7 3.3	5.1 4.7	s	not preprogrammed preprogrammed
Bank 0 Erase (256K) (3)	5.6 4.0	13.6 11.9	19.2 17.5	s	not preprogrammed preprogrammed
Recovery from Power-Down (t_{PD})	–	40	40	µs	(4)
Program Suspend Latency (4)	–	10	10	µs	
Erase Suspend Latency (4)	–	30	30	µs	
Erase Suspend Request Rate (4)	20	20	20	ms	Min delay between 2 requests
Set Protection (4)	40	90	300	µs	

1. The figures are given after about 100 cycles due to testing routines (0 cycles at the final customer).
2. Word and Double Word Programming times are provided as average values derived from a full sector programming time: absolute value of a Word or Double Word Programming time could be longer than the average value.
3. Bank Erase is obtained through a multiple Sector Erase operation (setting bits related to all sectors of the Bank). As ST10F271 implements only one bank, the Bank Erase operation is equivalent to Module and Chip Erase operations.
4. Not 100% tested, guaranteed by Design Characterization.

Table 65. Flash data retention characteristics

Number of program / erase cycles (-40°C ≤T_A ≤125°C)	Data retention time (average ambient temperature 60°C)	
	256Kbyte (code store)	64Kbyte (EEPROM emulation) (1)
0 - 100	> 20 years	> 20 years
1,000	-	> 20 years
10,000	-	10 years
100,000	-	1 year

1. Two 64Kbyte Flash Sectors may be typically used to emulate up to 4, 8 or 16Kbyte of EEPROM. Therefore, in case of an emulation of a 16Kbyte EEPROM, 100,000 Flash Program / Erase cycles are equivalent to 800,000 EEPROM Program/Erase cycles. For an efficient use of the EEPROM Emulation please refer to dedicated Application Note document (*AN2061 - "EEPROM Emulation with ST10F2xx"*). Contact your local field service, local sales person or STMicroelectronics representative to get copy of such a guideline document.

24.7 A/D converter characteristics

V_{DD} = 5V ± 10%, V_{SS} = 0V, T_A = –40 to +125°C, 4.5V ≤V_{AREF} ≤V_{DD}, V_{SS} ≤V_{AGND} ≤V_{SS} + 0.2V

Table 66. A/D converter characteristics

Parameter	Symbol		Limit Values		Unit	Test Condition
			min.	max.		
Analog Reference voltage 1)	V_{AREF}	SR	4.5	V_{DD}	V	
Analog Ground voltage	V_{AGND}	SR	V_{SS}	V_{SS} + 0.2	V	
Analog Input voltage 2)	V_{AIN}	SR	V_{AGND}	V_{AREF}	V	
Reference supply current	I_{AREF}	CC	– –	5 1	mA µA	Running mode 3) Power Down mode
Sample time	t_S	CC	1	–	µs	4)
Conversion time	t_C	CC	3	–	µs	5)
Differential Non Linearity 6)	DNL	CC	–1	+1	LSB	No overload
Integral Non Linearity 6)	INL	CC	–1.5	+1.5	LSB	No overload
Offset Error 6)	OFS	CC	–1.5	+1.5	LSB	No overload
Total unadjusted error 6)	TUE	CC	–2.0 –5.0 –7.0	+2.0 +5.0 +7.0	LSB	Port5 Port1 - No overload 3) Port1 - Overload 3)
Coupling Factor between inputs 3) 7)	K	CC	–	10^{-6}	–	On both Port5 and Port1
Input Pin Capacitance 3) 8)	C_{P1}	CC	–	3	pF	
	C_{P2}	CC	–	4 6	pF	Port5 Port1
Sampling Capacitance 3) 8)	C_S	CC	–	3.5	pF	

1. Supposing to design the filter with the pole exactly at the maximum frequency of the signal, the time constant of the filter is:

$$R_C C_F = \frac{1}{2\pi f_0} = 15.9\mu s$$

2. Using the relation between C_F and C_S and taking some margin (4000 instead of 2048), it is possible to define C_F:

$$C_F = 4000 \cdot C_S = 16nF$$

3. As a consequence of step 1 and 2, RC can be chosen:

$$R_F = \frac{1}{2\pi f_0 C_F} = 995\Omega \cong 1k\Omega$$

4. Considering the current injection limitation and supposing that the source can go up to 12V, the total series resistance can be defined as:

$$R_S + R_F + R_L = \frac{V_{AM}}{I_{INJ}} = 4k\Omega$$

from which is now simple to define the value of R_L:

$$R_L = \frac{V_{AM}}{I_{INJ}} - R_F - R_S = 2.9k\Omega$$

5. Now the three element of the external circuit R_F, C_F and R_L are defined. Some conditions discussed in the previous paragraphs have been used to size the component, the other must now be verified. The relation which allow to minimize the accuracy error introduced by the switched capacitance equivalent resistance is in this case:

$$R_{EQ} = \frac{1}{f_C C_S} = 10M\Omega$$

So the error due to the voltage partitioning between the real resistive path and C_S is less then half a count (considering the worst case when V_A = 5V):

$$V_A \cdot \frac{R_S + R_F + R_L + R_{SW} + R_{AD}}{R_{EQ}} = 2.35mV < \frac{1}{2}LSB$$

The other conditions to be verified is the time constants of the transients are really and significantly shorter than the sampling period duration T_S:

$$\tau_1 = (R_{SW} + R_{AD}) \cdot C_S = 2.8ns << T_S = 1\mu s$$

$$10 \cdot \tau_2 = 10 \cdot R_L \cdot (C_S + C_{P1} + C_{P2}) = 290ns < T_S = 1\mu s$$

For complete set of parameters characterizing the ST10F271 A/D Converter equivalent circuit, refer to *Section 24.7: A/D converter characteristics on page 136*.

Table 72. Main oscillator negative resistance (module)

	C_A = 15pF			C_A = 25pF			C_A = 35pF		
	min.	typ.	max.	min.	typ.	max.	min.	typ.	max.
4 MHz	545 Ω	1035 Ω	–	550 Ω	1050 Ω	–	430 Ω	850 Ω	–
8 MHz	240 Ω	450 Ω	–	170 Ω	350 Ω	–	120 Ω	250 Ω	–

The given values of C_A do not include the stray capacitance of the package and of the printed circuit board: the negative resistance values are calculated assuming additional 5pF to the values in the table. The crystal shunt capacitance (C_0) and the package capacitance between XTAL1 and XTAL2 pins is globally assumed equal to 10pF.

The external resistance between XTAL1 and XTAL2 is not necessary, since already present on the silicon.

24.8.12 32 kHz oscillator specifications

V_{DD} = 5V ± 10%, V_{SS} = 0V, T_A = –40 to +125°C

Table 73. 32kHz oscillator characteristics

Symbol	Parameter	Conditions	Value			Unit
			min.	typ.	max.	
g_{m32}	Oscillator Transconductance [1]	Start-up	20	31	50	µA/V
		Normal run	8	17	30	µA/V
V_{OSC32}	Oscillation Amplitude [2]	Peak to Peak	0.5	1.0	2.4	V
V_{AV32}	Oscillation Voltage level [2]	Sine wave middle	0.7	0.9	1.2	V
t_{STUP32}	Oscillator Start-up Time [2]	Stable V_{DD}	–	1	5	s

1. At power-on a high current biasing is applied for faster oscillation start-up. Once the oscillation is started, the current biasing is reduced to lower the power consumption of the system.
2. Not 100% tested, guaranteed by design characterization.

Figure 48. 32kHz crystal oscillator connection diagram

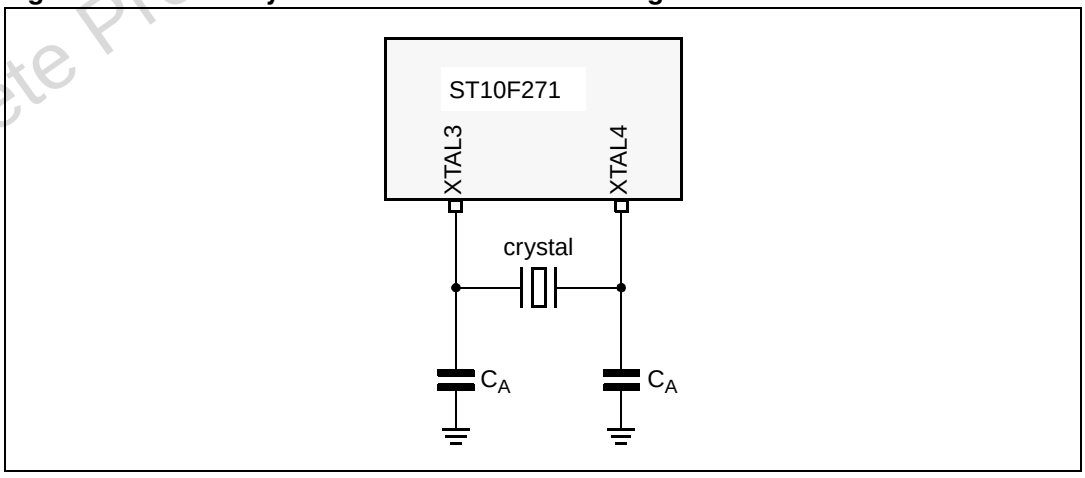


Figure 54. External memory cycle: Demultiplexed bus, with/without r/w delay, normal ALE

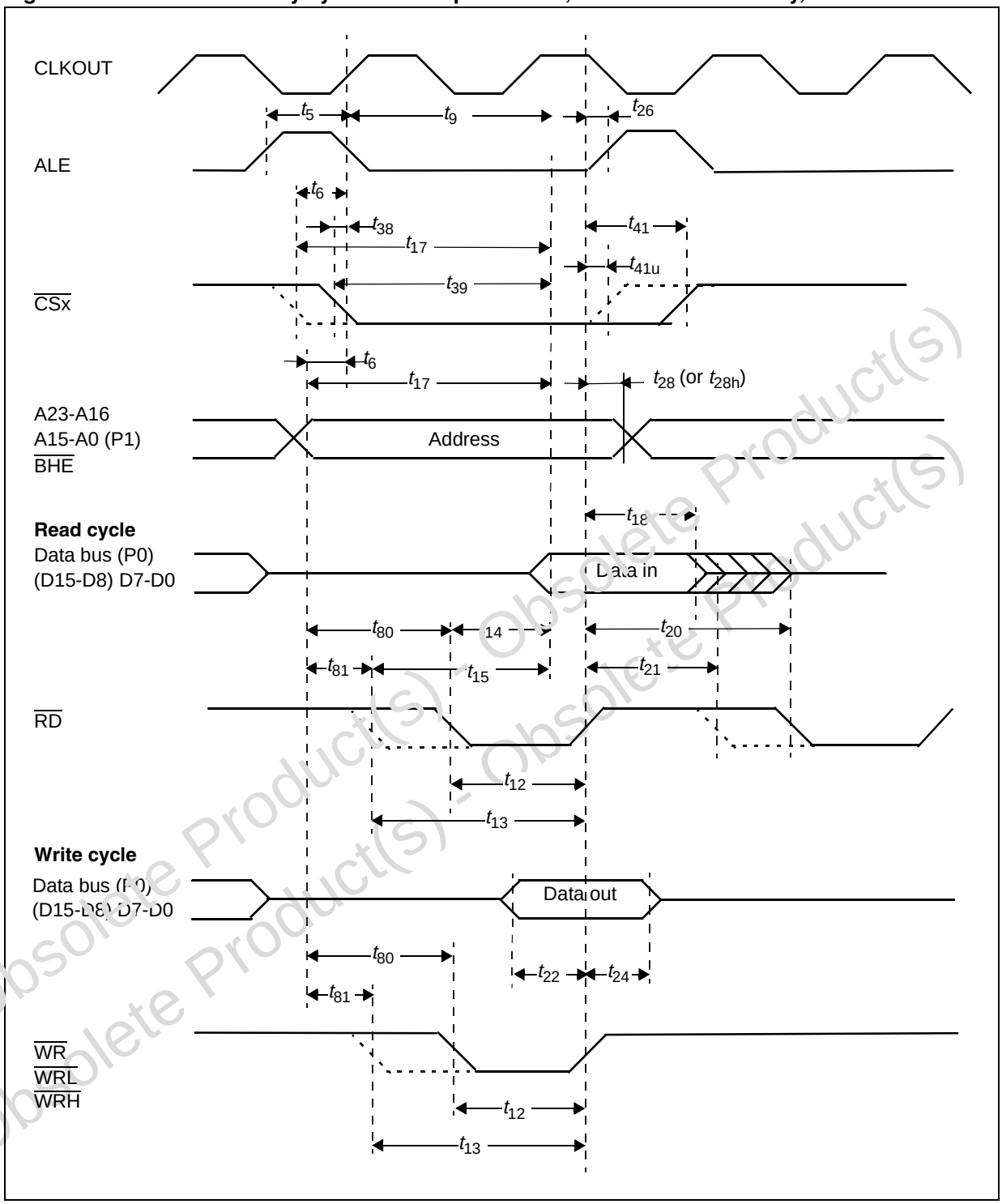


Figure 55. Exteral memory cycle: Demultiplexed bus, with/without r/w delay, extended ALE