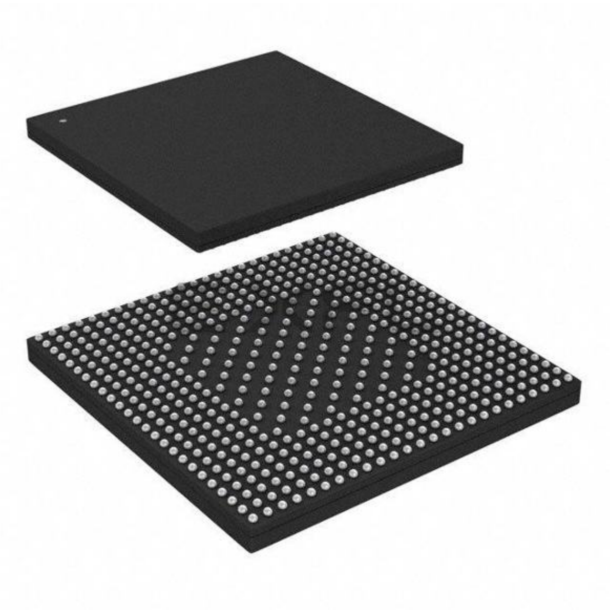

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## Understanding Embedded - Microprocessors

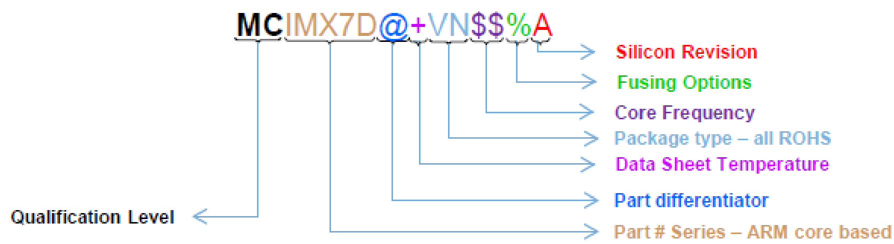
Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-A7, ARM® Cortex®-M4 |
| Number of Cores/Bus Width | 2 Core, 32-Bit |
| Speed | 1.2GHz |
| Co-Processors/DSP | Multimedia; NEON™ MPE |
| RAM Controllers | LPDDR2, LPDDR3, DDR3, DDR3L |
| Graphics Acceleration | No |
| Display & Interface Controllers | Keypad, LCD, MIPI |
| Ethernet | 10/100/1000Mbps (2) |
| SATA | - |
| USB | USB 2.0 + PHY (1), USB 2.0 OTG + PHY (2) |
| Voltage - I/O | 1.8V, 3.3V |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Security Features | A-HAB, ARM TZ, CAAM, CSU, SJC, SNVS |
| Package / Case | 488-TFBGA |
| Supplier Device Package | 488-TFBGA (12x12) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx7d2dvk12sc |

Figure 1 describes the part number nomenclature so that the users can identify the characteristics of the specific part number.




| Qualification Level | MC |
|---|---|
| Samples | PC |
| Mass | MC |
| Special | SC |

| Part # Series | |
|---|---|
| IMX7D | 2 x Cortex-A7<br>2 x USB2.0 OTG<br>(w/ PHY)<br>1 x PCIe<br>3 x SDIO/MMC, |
| IMX7S | 1 x Cortex-A7<br>1 x USB2.0 OTG<br>(w/ PHY)<br>3 x SDIO/MMC |

| Part differentiator | @ |
|---|---|
| Add 2x CAN and EPDC | 7 |
| Adds 2x CAN | 5 |
| Baseline Feature-set | 3 |
| Baseline Feature-set—Core up to 1.2GHz (restricted specifications) [1] | 2 |

| Temperature Tj | + |
|---|---|
| Consumer: 0 to + 95°C [1] | D |
| Extended Cons: -20 to + 105°C | E |

| Package Type | ROHS |
|---|---|
| MAPBGA 19x19 0.75mm | VM |
| MAPBGA 12 x12 0.4mm | VK |

| Frequency | $$ |
|---|---|
| 800 MHz | 08 |
| 1 GHz | 10 |
| 1.2 GHz | 12 |

| Fusing | % |
|---|---|
| Security Enabled | S |
| Security Disabled | A |

| Silicon Rev | A |
|---|---|
| Rev 1.0 | A |
| Rev 1.1 | B |
| Rev 1.2 | C |
| Rev. 1.3 | D |

1 Restricted electrical specifications for parts with CPU maximum frequency of 1.2 GHz:

- Temperature range 0 to 85 degrees C (see Table 1)
- VDD_ARM requirements (see Table 9)

**Figure 1. Part number nomenclature—i.MX 7Dual family of processors**

## 1.2 Features

The i.MX 7Dual family of processors is based on ARM Cortex-A7 MPCore™ Platform, which has the following features:

- Two ARM Cortex-A7 Cores (with TrustZone® technology)
- The core configuration is symmetric, where each core includes:
  - — 32 KByte L1 Instruction Cache
  - — 32 KByte L1 Data Cache
  - — Private Timer and Watchdog
  - — NEON MPE (media processing engine) coprocessor

The ARM Cortex-A7 Core complex shares:

- General interrupt controller (GIC) with 128 interrupt support
- Global timer
- Snoop control unit (SCU)
- 512 KB unified I/D L2 cache

The package contact assignments can be found in Section 6, "Package information and contact assignments." Signal descriptions are provided in the *i.MX 7Dual Application Processor Reference Manual* (IMX7DRM).

**Table 3. Special signal considerations**

| Signal Name | Remarks |
|---|---|
| CCM_CLK1_P/<br>CCM_CLK1_N<br>CCM_CLK2 | One general purpose differential high speed clock input/output and one single-ended clock input are provided.<br>Either or both of them can be used:<br>• To feed an external reference clock to the PLLs and to the modules inside the SoC, for example, as an alternate reference clock for PCIe, Video/Audio interfaces and so forth.<br>• To output the internal SoC clock to be used outside the SoC as either a reference clock or as a functional clock for peripherals; for example, it can be used as an output of the PCIe master clock (root complex use)<br>See the *i.MX 7Dual Application Processor Reference Manual* (IMX7DRM) for details on the respective clock trees.<br>The CCM_CLK1_* inputs/outputs are an LVDS differential pair.<br>Alternatively, a single-ended signal may be used to drive CCM_CLK1_P input. In this case corresponding CCM_CLK1_N input should be tied to the constant voltage level equal to 1/2 of the input signal swing.<br>Termination should be provided in case of high frequency signals.<br>See the LVDS pad electrical specification for further details. CCM_CLK2 is a single-ended input referenced to ground.<br>After initialization:<br>• The CCM_CLK1_* inputs/outputs can be disabled if not used. Any of the unused CCM_CLK1_* pins may be left floating.<br>• The CCM_CLK2 input should be grounded if not used. |
| RTC_XTALI/RTC_XTALO | If the user wishes to configure RTC_XTALI and RTC_XTALO as an RTC oscillator, a 32.768 kHz crystal, (100 k ESR, 10 pF load) should be connected between RTC_XTALI and RTC_XTALO. It is recommended to use the configurable load capacitors provided in the IP instead of adding them externally. To hit the exact oscillation frequency, the configurable capacitors need to be reduced to account for board and chip parasitics.<br>The integrated oscillation amplifier is self biasing, but relatively weak. Care must be taken to limit parasitic leakage from RTC_XTALI and RTC_XTALO to either power or ground (>100 M). This will debias the amplifier and cause a reduction of startup margin. Typically RTC_XTALI and RTC_XTALO should bias to approximately 0.5 V.<br>If it is desired to feed an external low frequency clock into RTC_XTALI, the RTC_XTALO pin should be left floating or driven with a complimentary signal. The logic level of this forcing clock should not exceed VDD_SNVS_CAP level.<br>In the case when a high-accuracy realtime clock is not required, the system may use internal low frequency oscillator. It is recommended to connect RTC_XTALI to ground and keep RTC_XTALO floating. This will however result in increased power consumption, because the internal oscillator uses higher power than the RTC oscillator. Thus for lowest power configuration it is recommended to always install a crystal. |
| XTALI/XTALO | A 24.0 MHz crystal should be connected between XTALI and XTALO. |

**Table 5. Recommended connections for unused analog interfaces(continued)**

| Module | Package Net Name | Recommendation if Unused |
|---|---|---|
| PCIe | PCIE_REFCLKIN_N, PCIE_REFCLKIN_P, PCIE_REFCLKOUT_N, PCIE_REFCLKOUT_P, PCIE_RX_N, PCIE_RX_P, PCIE_TX_N, PCIE_TX_P | Floating |
| | PCIE_VP,PCIE_VP_RX,PCIE_VP_TX, PCIE_VPH,PCIE_VPH_RX,PCIE_VPH_TX, PCIE_REXT | Tie to ground |
| SNVS | SNVS_TAMPER00, SNVS_TAMPER01, SNVS_TAMPER02, SNVS_TAMPER03, SNVS_TAMPER04, SNVS_TAMPER05, SNVS_TAMPER06, SNVS_TAMPER07, SNVS_TAMPER08, SNVS_TAMPER09 | Float—configure with software |
| Temperature sensor | TEMPSENSOR_REXT | Tie to ground or pulldown with 100 KΩ resistor |
| | TEMPSENSOR_RESERVE | Floating |
| | VDD_TEMPSENSOR_1P8 | 1.8 V |
| USB HSIC | VDD_USB_H_1P2 | Tie to ground |
| | USB_H_DATA, USB_H_STROBE | Floating |
| USB OTG1 | VDD_USB_OTG1_3P3_IN, VDD_USB_OTG1_1P0_CAP | Tie to ground |
| | USB_OTG1_VBUS, USB_OTG1_DP, USB_OTG1_DN, USB_OTG1_ID, USB_OTG1_REXT, USB_OTG1_CHD_B | Floating |
| USB OTG2 | VDD_USB_OTG2_3P3_IN, VDD_USB_OTG2_1P0_CAP | Tie to ground |
| | USB_OTG2_VBUS, USB_OTG2_DP, USB_OTG2_DN, USB_OTG2_ID, USB_OTG2_REXT | Floating |

# 4 Electrical characteristics

This section provides the device and module-level electrical characteristics for the i.MX 7Dual family of processors.

## 4.1 Chip-level conditions

This section provides the device-level electrical characteristics for the IC. See Table 6 for a quick reference to the individual tables and sections.

**Table 6. i.MX 7Dual Chip-level conditions**

| For these characteristics, … | Topic appears … |
|---|---|
| Absolute maximum ratings | on page 21 |
| FPBGA case “X” and case “Y” package thermal resistance | on page 22 |
| Operating ranges | on page 23 |
| External clock sources | on page 25 |

Table 10 shows on-chip LDO regulators that can supply on-chip loads.

**Table 10. On-chip LDOs[1] and their on-chip loads**

| Voltage Source | Load | Comment |
|---|---|---|
| VDDD_1P0_CAP | VDD_MIPI_1P0 | Connect directly (short) via board level |
| | PCIE_VP | |
| | PCIE_VP_RX | |
| | PCIE_VP_TX | |
| VDD_1P2_CAP | VDD_USB_H_1P2 | Connect directly (short) via board level |
| VDDA_PHY_1P8 | VDDA_MIPI_1P8 | Connect directly (short) via board level |
| | PCIE_VPH | |
| | PCIE_VPH_RX | |
| | PCIE_VPH_TX | |

1 On-chip LDOs are designed to supply i.MX 7Dual loads and must not be used to supply external loads.

### 4.1.4 External clock sources

Each i.MX 7Dual processor has two external input system clocks: a low frequency (RTC_XTALI) and a high frequency (XTALI).

The RTC_XTALI is used for low-frequency functions. It supplies the clock for wake-up circuit, power-down real time clock operation, and slow system and watch-dog counters. The clock input can be connected to either external oscillator or a crystal using internal oscillator amplifier. Additionally, there is an internal resistor-capacitor (RC) oscillator, which can be used instead of the RTC_XTALI if accuracy is not important.

The system clock input XTALI is used to generate the main system clock. It supplies the PLLs and other peripherals. The system clock input can be connected to either an external oscillator or a crystal using internal oscillator amplifier.

Table 11 shows the interface frequency requirements.

**Table 11. External input clock frequency**

| Parameter Description | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| RTC_XTALI Oscillator[1,2] | $f_{ckil}$ | — | 32.768[3] | — | kHz |
| XTALI Oscillator[2,4] | $f_{xtal}$ | | 24 | | MHz |

1 External oscillator or a crystal with internal oscillator amplifier.
2 The required frequency stability of this clock source is application dependent. See *Hardware Development Guide for i.MX7Dual and 7Solo Applications Processors.*
3 Recommended nominal frequency 32.768 kHz.
4 External oscillator or a fundamental frequency crystal appropriately coupled to the internal oscillator amplifier.

### 4.1.7.2 4.1.7.2 Power-Down modes

Table 17 shows the USB interface current consumption with only the OTG block powered down.

**Table 17. USB PHY current consumption with VBUS Valid Comparators disabled[1]**

| | VDD_USB_OTG1_3P3_IN | VDD_USB_OTG2_3P3_IN |
|---|---|---|
| **Current** | 730 uA | 730 uA |

[1] VBUS Valid comparators can be disabled through software by setting USBNC_OTG*_PHY_CFG2[OTGDISABLE0] to 1. This signal powers down only the VBUS Valid comparator, and does not control power to the Session Valid Comparator, ADP Probe and Sense comparators, or the ID detection circuitry.

In Power-Down mode, everything is powered down, including the USB_VBUS valid comparators and their associated bandgap circuity in typical condition. Table 18 shows the USB interface current consumption in Power-Down mode.

**Table 18. USB PHY current consumption in Power-Down mode[1]**

| | VDD_USB_OTG1_3P3_IN | VDD_USB_OTG2_3P3_IN |
|---|---|---|
| **Current** | 200 uA | 200 uA |

[1] The VBUS Valid Comparators and their associated bandgap circuits can be disabled through software by setting USBNC_OTG*_PHY_CFG2[OTGDISABLE0] to 1 and USBNC_OTG*_PHY_CFG2[DRVVBUS0] to 0, respectively.

## 4.1.8 PCIe phy 2.1 DC electrical characteristics

**Table 19. PCIe recommended operating conditions**

| Parameter | Description | | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Low Power Supply Voltage for PHY Core | 1 V | 0.95 | 1.05 | V |
| | High Power Supply Voltage for PHY Core | 1.8 V | 1.71 | 1.89 | |
| $T_A$ | Commercial Temperature Range | | 0 | 70 | °C |
| $T_J$ | Simulation Junction Temperature Range | | -40 | 125 | °C |

**Note:** $V_{DD}$ should have no more than 40 mVpp AC power supply noise superimposed on the high power supply voltage for the PHY core (1.8 V nominal DC value). At the same time, VDD should have no more than 20 mVpp AC power supply noise superimposed on the low power supply voltage for the PHY core.
The power supply voltage variation for the PHY core should have less than +/-5% including the board-level power supply variation and on-chip power supply variation due to the finite impedances in the package.

**Table 21. PCIe PHY high-speed characteristics(continued)**

| High Speed I/O Characteristics | | | | | | |
|---|---|---|---|---|---|---|
| **Description** | **Symbol** | **Speed** | **Min.** | **Typ.** | **Max.** | **Unit** |
| PCIe Tx deterministic jitter < 1.5 MHz | TRJ | 2.5 Gbps/ 5.0 Gbps | — | — | 3 ps | ps, rms |
| PCIe Tx deterministic jitter > 1.5 MHz | TDJ | 5.0 Gbps/ 2.5 Gbps | — | — | 30 ps/ 60 ps | ps, pk–pk |
| RX Serial data input voltage (Differential pk–pk) | $\Delta V_{RX}$ | 1.5 Gbps | 325 | — | 600 | mVp–p |
| | | 2.5 Gbps | 120 | — | 1200 | |
| | | 3.0 Gbps | 275 | — | 750 | |
| | | 5.0 Gbps | 120 | — | 1200 | |
| | | 6.0 Gbps | 240 | — | 1000 | |

**Table 22. PCIe PHY reference clock timing requirements**

| Description | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Frequency Tolerance | $F_{TOL}$ | –100 | — | 100 | ppm |
| Duty Cycle | $D_C$ | 40 | — | 60 | % |
| Rise and Fall Time | $T_R$,$T_F$ | — | — | 1.5 | ns |
| Peak to peak Jitter | Jitter | — | — | 40 | ps,pk–pk |
| RMS Jitter | | — | — | 2.5 | ps,rms |
| Period Jitter | | — | — | 25 | ps |
| External Clock source output impedence | $Z_{C,DC}$ | 40 | — | 60 | Ω |
| Differential input high voltage | $V_{IH}$ | 150 | — | | mV |
| Differential input low voltage | $V_{IL}$ | — | — | -150 | mV |
| Absolute maximum input voltage | $V_{MAX}$ | 33 | — | 1.15 | V |
| Absolute minimum input voltage | $V_{MIN}$ | 400 | — | -0.3 | V |
| Absolute crossing point voltage | $V_{CROSS}$ | 250 | — | 1550 | mV |

- Irreversible damage to the processor (worst-case scenario)

### 4.1.9 Power-up sequence

The i.MX7 processor has the following power-up sequence requirements:

- VDD_SNVS_IN to be turned on before any other power supply. If a coin cell is used to power VDD_SNVS_IN, then ensure that it is connected before any other supply is switched on.
- VDD_SOC to be turned on before NVCC_DRAM and NVCC_DRAM_CKE.
- VDD_ARM, VDD_SOC, VDDA_1P8_IN, VDD_LPSR_IN and all I/O power (NVCC_*) should be turned on after VDD_SVNS_IN is active. But there is no sequence requirement among these power rails other than the sequence requirement between VDD_SOC and NVCC_DRAM/NVCC_DRAM_CKE.
- There are no special timing requirements for VDD_USB_OTG1_3P3_IN and VDD_USB_OTG2_3P3_IN.

The POR_B input (if used) must be immediately asserted at power-up and remain asserted until the last power rail reaches its working voltage. In the absence of an external reset feeding the POR_B input, the internal POR module takes control.

The power-up sequence is shown in Figure 4 with the following timing parameters:

T1 Time from SVNS power stable to other power rails start to ramp, minimal delay is 2ms, no max delay requirement.

T2 Time from first power rails (except SNVS) ramp up to all the power rails get stable, minimal delay is 0ms, no max delay requirement.

T3 Time from all power rails get stable to power-on reset, minimal delay is 0ms, no max delay requirement.

T6 Time from VDD_SOC get stable to NVCC_DRAM/NVCC_DRAM_CKE start to ramp, minimal delay is 0ms, no max delay requirement.

The system crystal oscillator consists of a Pierce-type structure running off the digital supply. A straight forward biased-inverter implementation is used.

### 4.4.2 OSC32K

This block implements an internal amplifier, trimable load capacitors and a resistor that when combined with a suitable quartz crystal implements a low power oscillator.

In addition, if the clock monitor determines that the OSC32K is not present then the source of the 32 kHz clock will automatically switch to the internal relaxation oscillator of lesser frequency accuracy.

**CAUTION**

The internal RTC oscillator does not provide an accurate frequency and is affected by process, voltage and temperature variations. NXP strongly recommends using an external crystal as the RTC_XTALI reference. If the internal oscillator is used instead, careful consideration must be given to the timing implications on all of the SoC modules dependent on this clock.

The OSC32k runs from VDD_SNVS_1p8_CAP, which is regulated from VDD_SNVS. The target battery is an ~3 V coin cell for VDD_SNVS and the regulated output is ~1.75V.

**Table 28. OSC32K Main Characteristics**

| | Min | Typ | Max | Comments |
|---|---|---|---|---|
| Fosc | — | 32.768 KHz | — | This frequency is nominal and determined by the crystal selected. 32.0 K would work as well. |
| Current consumption | — | 350 nA | — | The typical value shown is only for the oscillator, driven by an external crystal. If the interrelaxation oscillator is used instead of an external crystal then approximately 250 nA should be added to this value. |
| Bias resistor | — | 200 MΩ | | This is the integrated bias resistor that sets the amplifier into a high gain state. Any leakage through the ESD network, external board leakage, or even a scope probe that is significant relative to this value will debias the amp. The debiasing will result in low gain and will impact the circuit's ability to start up and maintain oscillations. |
| **Target Crystal Properties** | | | | |
| Cload | — | 10 pF | — | Usually, crystals can be purchased tuned for different Cload. This Cload value is typically 1/2 of the capacitances realized on the PCB on either side of the quartz. A higher Cload will decrease oscillation margin but increases current oscillating through the crystal. The Cload is programmable in 2 pF steps. |
| ESR | — | 50 KΩ | — | Equivalent series resistance of the crystal. Choosing a crystal with a higher value will decrease oscillating margin. |

## 4.5 I/O DC parameters

This section includes the DC parameters of the following I/O types:

DDRMC operation with the standards stated above is contingent upon the board DDR design adherence to the DDR design and layout requirements stated in the hardware development guide for the i.MX 7 application processor.

**Table 30. DC input logic level**

| Characteristics | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC input logic high[1] | $V_{IH(DC)}$ | $V_{REF}$ +100 | — | mV |
| DC input logic low[1] | $V_{IL(DC)}$ | — | $V_{REF}$ –100 | |

[1] It is the relationship of the $V_{DDQ}$ of the driving device and the $V_{REF}$ of the receiving device that determines noise margins. However, in the case of $V_{IH}$(DC) max (that is, input overdrive), it is the $V_{DDQ}$ of the receiving device that is referenced.

**Table 31. Output DC current drive**

| Characteristics | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Output minimum source DC current[1] | $I_{OH}$(DC) | –4 | — | mA |
| Output minimum sink DC current[1] | $I_{OL}$(DC) | 4 | — | mA |
| DC output high voltage($I_{OH}$ = –0.1mA)[1,2] | $V_{OH}$ | $0.9 \times V_{DDQ}$ | — | V |
| DC output low voltage($I_{OL}$ = 0.1mA)[1,2] | $V_{OL}$ | — | $0.1 \times V_{DDQ}$ | V |

[1] When DDS=[111] and without ZQ calibration.
[2] The values of $V_{OH}$ and $V_{OL}$ are valid only for 1.2 V range.

**Table 32. Input DC current**

| Characteristics | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| High level input current[1,2] | $I_{IH}$ | –25 | 25 | μA |
| Low level input current[1,2] | $I_{IL}$ | –25 | 25 | μA |

[1] The values of $V_{OH}$ and $V_{OL}$ are valid only for 1.2 V range.
[2] Driver Hi-Z and input power-down (PD=High)

#### 4.5.2.1 LPDDR3 mode I/O DC parameters

**Table 33. LPDDR3 I/O DC electrical parameters**

| Parameters | Symbol | Test Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| High-level output voltage | VOH | Ioh= -0.1mA | 0.9 × OVDD | — | V |
| Low-level output voltage | VOL | Iol= 0.1mA | — | 0.1 × OVDD | V |
| Input Reference Voltage | Vref | — | 0.49 × OVDD | 0.51 × OVDD | V |

**Table 33. LPDDR3 I/O DC electrical parameters(continued)**

| Parameters | Symbol | Test Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| DC High-Level input voltage | Vih_DC | — | VRef + 0.100 | OVDD | V |
| DC Low-Level input voltage | Vil_DC | — | OVSS | VRef – 0.100 | V |
| Differential Input Logic High | Vih_diff | — | 0.26 | See note[1] | — |
| Differential Input Logic Low | Vil_diff | — | See note[1] | -0.26 | — |
| Pull-up/Pull-down Impedance Mismatch | Mmpupd | — | –15 | 15 | % |
| 240 ?unit calibration resolution | Rres | — | — | 10 | ? |
| Keeper Circuit Resistance | Rkeep | — | 110 | 175 | k? |
| Input current (no pull-up/down) | Iin | VI = 0, VI = OVDD | -2.5 | 2.5 | µA |

[1] The single-ended signals need to be within the respective limits (Vih(dc) max, Vil(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot.

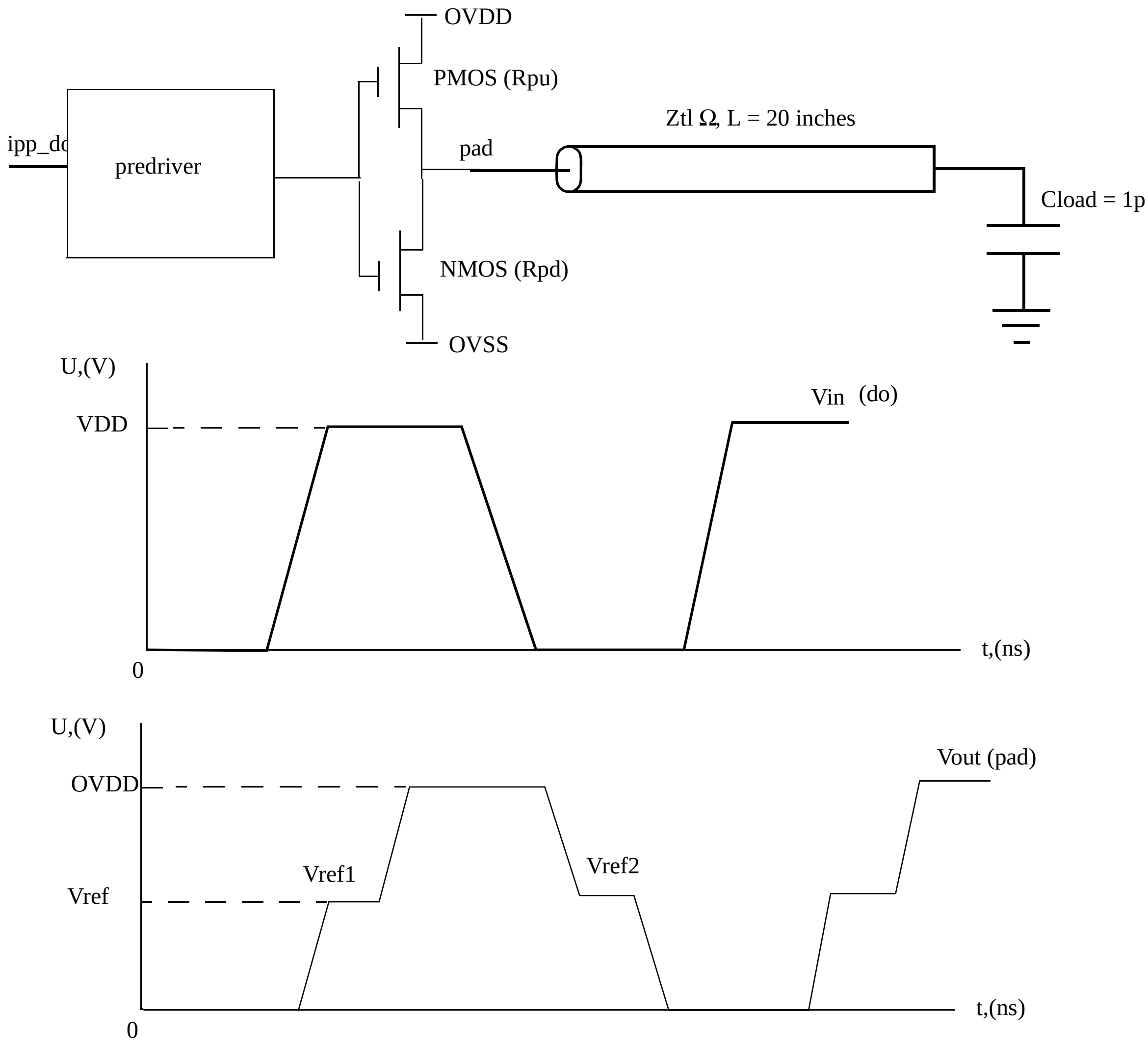
## 4.5.3 Differential I/O port (CCM_CLK1P/N)

The clock I/O interface is designed to be compatible with TIA/EIA 644-A standard. See TIA/EIA STANDARD 644-A, *Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits* (2001), for details.

Table 34 shows the clock I/O DC parameters.

**Table 34. Differential clock I/O DC electrical characteristics**

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|---|
| Vod | Output Differential Voltage | Rload=100 Ω between padp and padn | 250 | 350 | 450 | mV | Vpadp–Vpadn |
| Voh | High-level output voltage | | 1.025 | 1.175 | 1.325 | V | [1] |
| Vol | Low-level output voltage | | 0.675 | 0.825 | 0.975 | | [2] |
| Vocm | Output common mode voltage | | 0.9 | 1 | 1.1 | | Core supply is used |
| Vid | Input Differential Voltage | | 100 | | 600 | mV | Vpadp–Vpadn |
| Vicm | Input common mode voltage | | 50m | | 1.57 | V | Vicm(max)=ovdd(min)–Vid(min)/2 |
| Icc-ovdd | Tri-state I/O supply current | ipp_ibe=ipp_obe=0 irefin disabled (0uA) | | | 0.46 | uA | |




$$Rpu = \frac{Vovdd - Vref1}{Vref1} \times Ztl$$

$$Rpd = \frac{Vref2}{Vovdd - Vref2} \times Ztl$$

**Figure 9. Impedance matching load for measurement**

## 4.7.1 DDR I/O output buffer impedance

The LPDDR2 interface is designed to be fully compatible with JESD209-2B LPDDR2 JEDEC standard release June, 2009. The LPDDR3 interface mode is designed to be compatible with JESD209-3B JEDEC standard released August, 2013. The DDR3 interface is designed to be fully compatible with JESD79-3F DDR3 JEDEC standard release July, 2012.

1 t is the maximum EIM logic (axi_clk) cycle time. The maximum allowed axi_clk frequency depends on the fixed/non-fixed latency configuration, whereas the maximum allowed EIM_BCLK frequency is:

—Fixed latency for both read and write is 132 MHz.

—Variable latency for read only is 132 MHz.

—Variable latency for write only is 52 MHz.

In variable latency configuration for write, if BCD = 0 & WBCDD = 1 or BCD = 1, axi_clk must be 104 MHz. Write BCD = 1 and 104 MHz axi_clk, will result in a EIM_BCLK of 52 MHz. When the clock branch to EIM is decreased to 104 MHz, other buses are impacted which are clocked from this source. See the CCM chapter of the *i.MX 7Dual Application Processor Reference Manual* (IMX7DRM) for a detailed clock tree description.

2 EIM_BCLK parameters are being measured from the 50% point, that is, high is defined as 50% of signal value and low is defined as 50% as signal value.

3 For signal measurements, “High” is defined as 80% of signal value and “Low” is defined as 20% of signal value.

Figure 14 to Figure 17 provide few examples of basic EIM accesses to external memory devices with the timing parameters mentioned previously for specific control parameters settings.

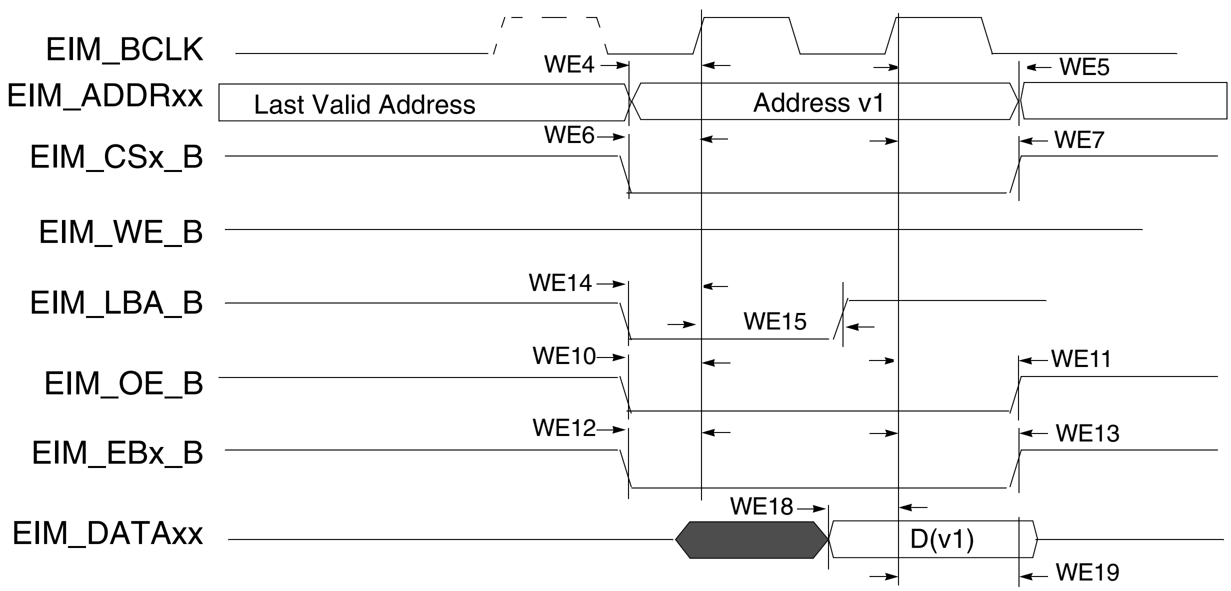



**Figure 14. Synchronous memory read access, WSC=1**

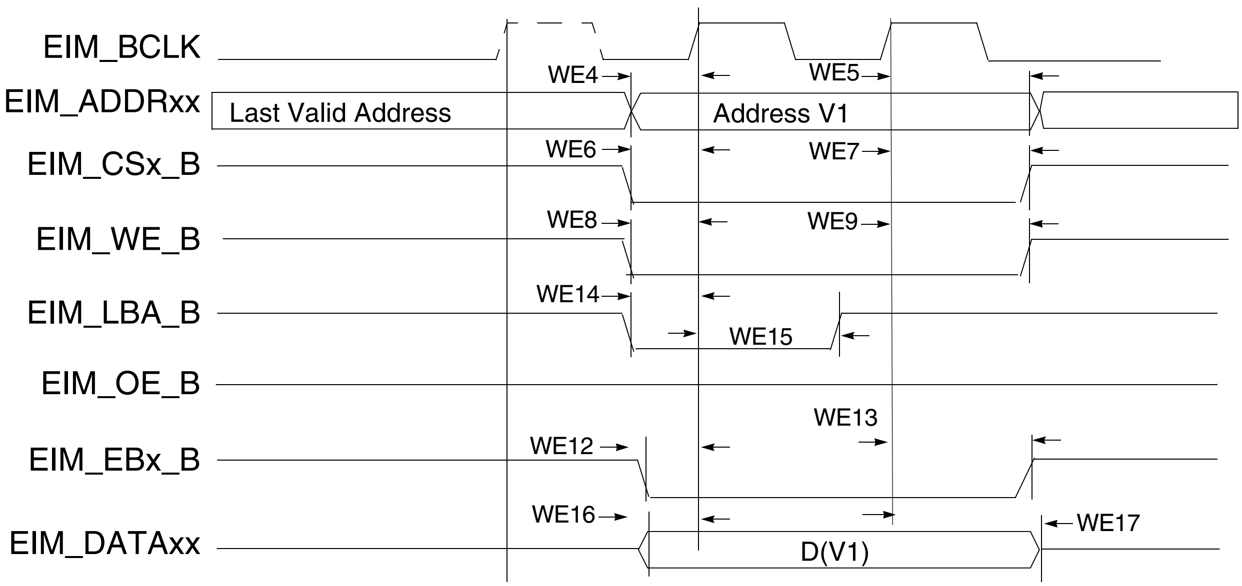



**Figure 15. Synchronous memory, write access, WSC=1, WBEA=0 and WADVN=0**

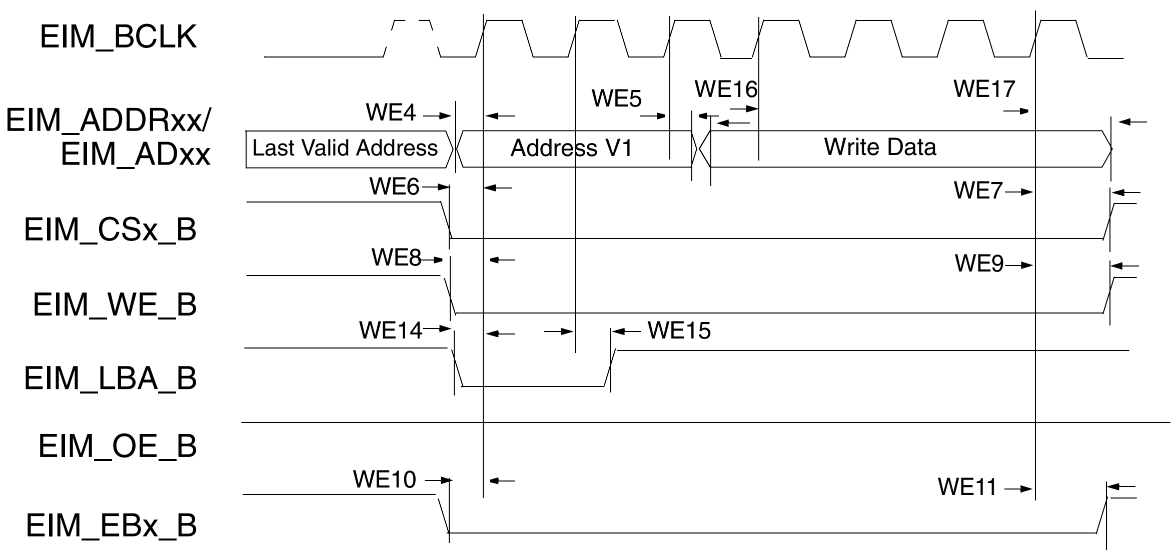



**Figure 16. Muxed Address/Data (A/D) mode, synchronous write access, WSC=6, ADVA=0, ADVN=1, and ADH=1**

## NOTE

In 32-bit Muxed Address/Data (A/D) mode the 16 MSBs are driven on the data bus.

Figure 31 shows the LPDDR2 write timing diagram. The timing parameters for this diagram appear in Table 54.

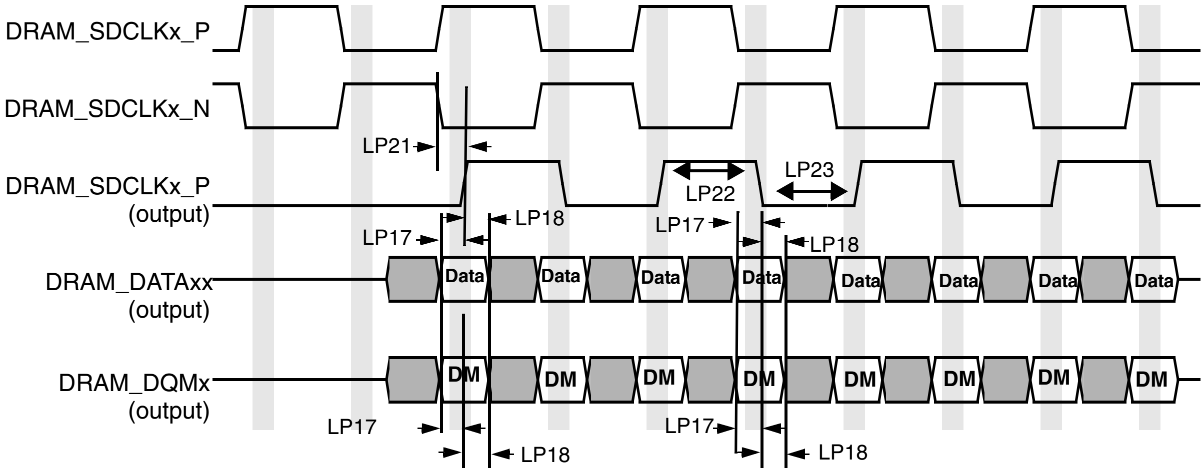



**Figure 31. LPDDR2 write cycle**

**Table 54. LPDDR2 write cycle**

| ID | Parameter | Symbol | CK = 533 MHz | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| LP17 | DRAM_DATAxx and DRAM_DQMx setup time to DRAM_SDQSx_P (differential strobe) | tDS | 360 | — | ps |
| LP18 | DRAM_DATAxx and DRAM_DQMx hold time to DRAM_SDQSx_P (differential strobe) | tDH | 360 | — | ps |
| LP21 | DRAM_SDQSx_P latching rising transitions to associated clock edges | tDQSS | -0.25 | +0.25 | tCK |
| LP22 | DRAM_SDQSx_P high level width | tDQSH | 0.4 | — | tCK |
| LP23 | DRAM_SDQSx_P low level width | tDQSL | 0.4 | — | tCK |

1 To receive the reported setup and hold values, write calibration should be performed in order to locate the DRAM_SDQS in the middle of DRAM_DATAxx window.

2 All measurements are in reference to Vref level.

3 Measurements were done using balanced load and 25 Ω resistor from outputs to DDR_VREF.

### 4.10.11.2 DDR Mode

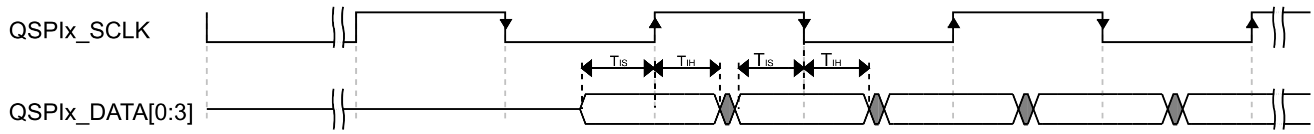



**Figure 74. QuadSPI Input/Read Timing (DDR mode with internal sampling)**

**Table 82. QuadSPI Input/Read Timing (DDR mode with internal sampling)**

| Symbol | Parameter | Value | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| $T_{IS}$ | Setup time for incoming data | 8.67 | — | ns |
| $T_{IH}$ | Hold time requirement for incoming data | 0 | — | ns |

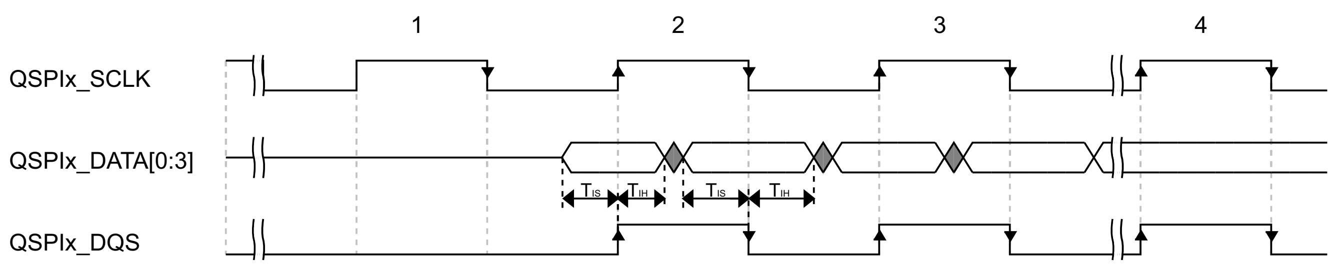



**Figure 75. QuadSPI Input/Read Timing (DDR mode with loopback DQS sampling)**

**Table 83. QuadSPI Input/Read Timing (DDR mode with loopback DQS sampling)**

| Symbol | Parameter | Value | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| $T_{IS}$ | Setup time for incoming data | 2 | — | ns |
| $T_{IH}$ | Hold time requirement for incoming data | 1 | — | ns |

**NOTE**

- For internal sampling, the timing values assumes using sample point 0, that is QuadSPIx_SMPR[SDRSMP] = 0.

#### 4.10.14.2.1 UART transmitter

Figure 83 depicts the transmit timing of UART in the RS-232 Serial mode, with 8 data bit/1 stop bit format. Table 89 lists the UART RS-232 Serial mode transmit timing characteristics.

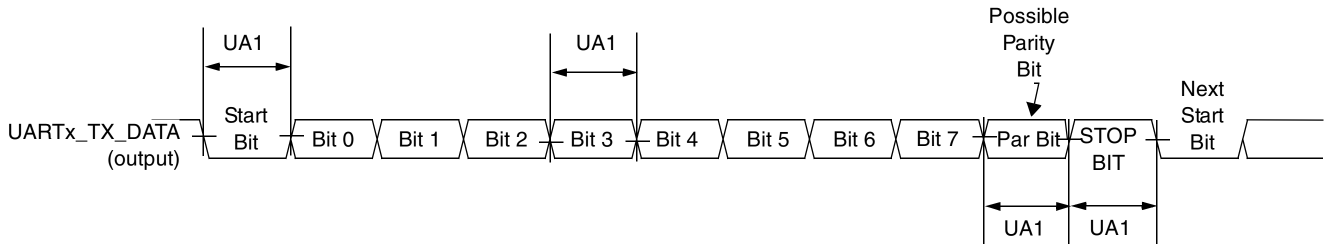



**Figure 83. UART RS-232 Serial mode transmit timing diagram**

**Table 89. RS-232 Serial mode transmit timing parameters**

| ID | Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| UA1 | Transmit Bit Time | $t_{Tbit}$ | $1/F_{baud\_rate}$[1] - $T_{ref\_clk}$[2] | $1/F_{baud\_rate} + T_{ref\_clk}$ | — |

[1] $F_{baud\_rate}$: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

[2] $T_{ref\_clk}$: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

#### 4.10.14.2.2 UART receiver

Figure 84 depicts the RS-232 Serial mode receive timing with 8 data bit/1 stop bit format. Table 90 lists Serial mode receive timing characteristics.

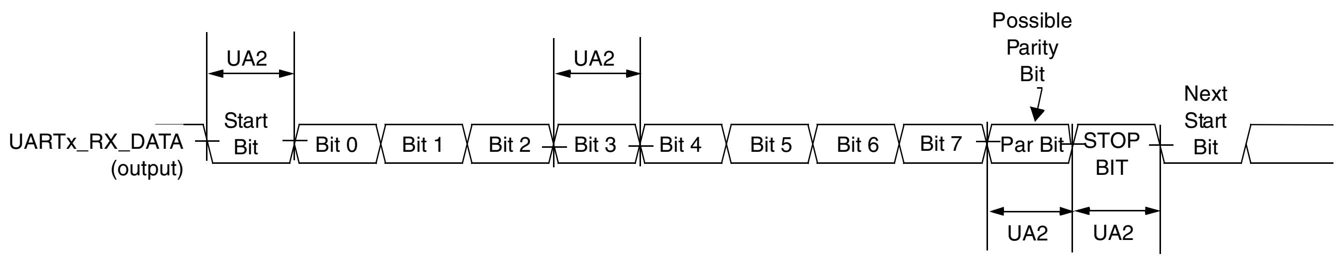



**Figure 84. UART RS-232 Serial mode receive timing diagram**

**Table 90. RS-232 Serial mode receive timing parameters**

| ID | Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| UA2 | Receive Bit Time[1] | $t_{Rbit}$ | $1/F_{baud\_rate}$[2] - $1/(16 \times F_{baud\_rate})$ | $1/F_{baud\_rate} + 1/(16 \times F_{baud\_rate})$ | — |

[1] The UART receiver can tolerate $1/(16 \times F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud\_rate})$.

[2] $F_{baud\_rate}$: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

## 4.10.15 USB HSIC timing

This section describes the electrical information of the USB HSIC port.

**Table 97. Interface allocation during boot(continued)**

| Interface | IP Instance | Allocated Pads During Boot | Comment |
|---|---|---|---|
| SPI | ECSPI-2 | ECSPI2_SCLK, ECSPI2_MOSI, ECSPI2_MISO, ECSPI2_SS0, ENET1_RX_CTL, ENET1_RXC, ENET1_TD0 | The chip-select pin used depends on the fuse "CS select (SPI only)" |
| SPI | ECSPI-3 | SAI2_TXFS, SAI2_TXC, SAI2_RXD, SAI2_TXD, SD1_DATA3, SD2_CD_B, SD2_WP | The chip-select pin used depends on the fuse "CS select (SPI only)" |
| SPI | ECSPI-4 | SD1_CD_B, SD1_WP, SD1_RESET_B, SD1_CLK, SD1_CMD, SD1_DATA0, SD1_DATA1 | The chip-select pin used depends on the fuse "CS select (SPI only)" |
| EIM | EIM | EPDC_SDCE2, EPDC_SDCE3, EPDC_GDCLK, EPDC_GDOE, EPDC_GDRL, EPDC_GDSP, EPDC_BDR0, LCD_DAT20, LCD_DAT21, LCD_DAT22, LCD_DAT23, EPDC_D8, EPDC_D9, EPDC_D10, EPDC_D12, EPDC_D14, EPDC_PWRSTAT | Used for NOR, OneNAND boot Only CS0 is supported. Allocated pads may differ depending on mux mode. See the “System Boot, Fusemap, and eFuse” chapter of the *i.MX 7Dual Application Processor Reference Manual* (IMX7DRM) for details. |
| NAND Flash | GPMI | SD3_CLK, SD3_CMD, SD3_DATA0, SD3_DATA1, SD3_DATA2, SD3_DATA3, SD3_DATA4, SD3_DATA5, SD3_DATA6, SD3_DATA7, SD3_STROBE, SD3_RESET_B, SAI1_TXC, SAI1_TXFS, SAI1_TXD | 8 bit<br>Only CS0 is supported |
| SD/MMC | USDHC-1 | SD1_CD_B, SD1_RESET_B, SD1_CLK, SD1_CMD, SD1_DATA0, SD1_DATA1, SD1_DATA2, SD1_DATA3, GPIO1_IO08, ECSPI2_SCLK, ECSPI2_MOSI, ECSPI2_MISO, ECSPI2_SS0 | 1, 4, or 8 bit |
| SD/MMC | USDHC-2 | SD2_RESET_B, SD2_CLK, SD2_CMD, SD2_DATA0, SD2_DATA1, SD2_DATA2, SD2_DATA3, GPIO1_IO12, ECSPI1_SCLK, ECSPI1_MOSI, ECSPI1_MISO, ECSPI1_SS0 | 1, 4, or 8 bit |
| SD/MMC | USDHC-3 | SD3_CLK, SD3_CMD, SD3_DAT0, SD3_DAT1, SD3_DAT2, SD3_DAT3, SD3_DAT4, SD3_DAT5, SD3_DAT6, SD3_DAT7, SD3_RESET_B | 1, 4, or 8 bit |
| USB | USB-OTG PHY | | — |

**Table 98. i.MX 7Dual 12 x 12 mm supplies contact assignments(continued)**

| Rail | Ball | Comments |
|---|---|---|
| VDD_XTAL_1P8 | AH02 | |
| VDDA_1P0_CAP | AH07 | Secondary supply for 1.0V. Requires external capacitor |
| VDDA_1P8_IN | AF04,AG03,AG04 | Supply for 1.8V |
| VDDA_ADC1_1P8 | AH04 | Supply for ADC |
| VDDA_MIPI_1P8 | J15 | Supply for MIPI |
| VDDA_PHY_1P8 | Y14 | |
| VDDD_1P0_CAP | AC13,AE12,AF12 | Secondary supply for 1.0V. Requires external capacitor |

Table 99 shows an alpha-sorted list of functional contact assignments for the 12 x 12 mm package.

**Table 99. i.MX 7Dual 12 x 12 mm functional contact assignments**

| Ball | Ball Name | Power Group | Ball type[1] | Default Mode[1] | Default Function[1] | PD/PU |
|---|---|---|---|---|---|---|
| AB07 | ADC1_IN0 | ADC1_VDDA_1P8 | | | ADC1_IN0 | |
| AC07 | ADC1_IN1 | ADC1_VDDA_1P8 | | | ADC1_IN1 | |
| AD07 | ADC1_IN2 | ADC1_VDDA_1P8 | | | ADC1_IN2 | |
| AD09 | ADC1_IN3 | ADC1_VDDA_1P8 | | | ADC1_IN3 | |
| Y01 | BOOT_MODE0 | NVCC_GPIO1 | GPIO | ALT0 | BOOT_MODE0 | 100K PD |
| Y02 | BOOT_MODE1 | NVCC_GPIO1 | GPIO | ALT0 | BOOT_MODE1 | 100K PD |
| AE04 | CCM_CLK1_N | VDDA_1P8 | | | CCM_CLK1_N | |
| AE03 | CCM_CLK1_P | VDDA_1P8 | | | CCM_CLK1_P | |
| AE02 | CCM_CLK2 | VDDA_1P8 | | | CCM_CLK2 | |
| AC24 | DRAM_ADDR00 | NVCC_DRAM | DDR | | DRAM_ADDR00 | |
| AC25 | DRAM_ADDR01 | NVCC_DRAM | DDR | | DRAM_ADDR01 | |
| AC26 | DRAM_ADDR02 | NVCC_DRAM | DDR | | DRAM_ADDR02 | |
| AB25 | DRAM_ADDR03 | NVCC_DRAM | DDR | | DRAM_ADDR03 | |
| AB24 | DRAM_ADDR04 | NVCC_DRAM | DDR | | DRAM_ADDR04 | |
| AE23 | DRAM_ADDR05 | NVCC_DRAM | DDR | | DRAM_ADDR05 | |
| AF23 | DRAM_ADDR06 | NVCC_DRAM | DDR | | DRAM_ADDR06 | |
| AE22 | DRAM_ADDR07 | NVCC_DRAM | DDR | | DRAM_ADDR07 | |
| AD22 | DRAM_ADDR08 | NVCC_DRAM | DDR | | DRAM_ADDR08 | |
| AC22 | DRAM_ADDR09 | NVCC_DRAM | DDR | | DRAM_ADDR09 | |

**Table 102. i.MX 7Dual 19 x 19 mm functional contact assignments(continued)**

| Ball | Ball Name | Power Group | Ball type[1] | Default Mode[1] | Default Function[1] | PD/PU |
|---|---|---|---|---|---|---|
| D21 | LCD_DATA00 | NVCC_LCD | GPIO | ALT5 | GPIO3_IO[5] | 100K PD |
| A22 | LCD_DATA01 | NVCC_LCD | GPIO | ALT5 | GPIO3_IO[6] | 100K PD |
| B22 | LCD_DATA02 | NVCC_LCD | GPIO | ALT5 | GPIO3_IO[7] | 100K PD |
| A23 | LCD_DATA03 | NVCC_LCD | GPIO | ALT5 | GPIO3_IO[8] | 100K PD |
| C22 | LCD_DATA04 | NVCC_LCD | GPIO | ALT5 | GPIO3_IO[9] | 100K PD |
| B23 | LCD_DATA05 | NVCC_LCD | GPIO | ALT5 | GPIO3_IO[10] | 100K PD |
| A24 | LCD_DATA06 | NVCC_LCD | GPIO | ALT5 | GPIO3_IO[11] | 100K PD |
| F20 | LCD_DATA07 | NVCC_LCD | GPIO | ALT5 | GPIO3_IO[12] | 100K PD |
| E21 | LCD_DATA08 | NVCC_LCD | GPIO | ALT5 | GPIO3_IO[13] | 100K PD |
| C23 | LCD_DATA09 | NVCC_LCD | GPIO | ALT5 | GPIO3_IO[14] | 100K PD |
| B24 | LCD_DATA10 | NVCC_LCD | GPIO | ALT5 | GPIO3_IO[15] | 100K PD |
| G20 | LCD_DATA11 | NVCC_LCD | GPIO | ALT5 | GPIO3_IO[16] | 100K PD |
| F21 | LCD_DATA12 | NVCC_LCD | GPIO | ALT5 | GPIO3_IO[17] | 100K PD |
| E22 | LCD_DATA13 | NVCC_LCD | GPIO | ALT5 | GPIO3_IO[18] | 100K PD |
| D23 | LCD_DATA14 | NVCC_LCD | GPIO | ALT5 | GPIO3_IO[19] | 100K PD |
| C24 | LCD_DATA15 | NVCC_LCD | GPIO | ALT5 | GPIO3_IO[20] | 100K PD |
| B25 | LCD_DATA16 | NVCC_LCD | GPIO | ALT5 | GPIO3_IO[21] | 100K PD |
| G21 | LCD_DATA17 | NVCC_LCD | GPIO | ALT5 | GPIO3_IO[22] | 100K PD |
| E23 | LCD_DATA18 | NVCC_LCD | GPIO | ALT5 | GPIO3_IO[23] | 100K PD |
| D24 | LCD_DATA19 | NVCC_LCD | GPIO | ALT5 | GPIO3_IO[24] | 100K PD |
| C25 | LCD_DATA20 | NVCC_LCD | GPIO | ALT5 | GPIO3_IO[25] | 100K PD |
| E24 | LCD_DATA21 | NVCC_LCD | GPIO | ALT5 | GPIO3_IO[26] | 100K PD |
| D25 | LCD_DATA22 | NVCC_LCD | GPIO | ALT5 | GPIO3_IO[27] | 100K PD |
| G23 | LCD_DATA23 | NVCC_LCD | GPIO | ALT5 | GPIO3_IO[28] | 100K PD |
| F25 | LCD_ENABLE | NVCC_LCD | GPIO | ALT5 | GPIO3_IO[1] | 100K PD |
| E25 | LCD_HSYNC | NVCC_LCD | GPIO | ALT5 | GPIO3_IO[2] | 100K PD |
| C21 | LCD_RESET | NVCC_LCD | GPIO | ALT5 | GPIO3_IO[4] | 100K PD |
| F24 | LCD_VSYNC | NVCC_LCD | GPIO | ALT5 | GPIO3_IO[3] | 100K PD |
| A15 | MIPI_CSI_CLK_N | MIPI_VDDA_1P8 | | | MIPI_CSI_CLK_N | |
| B15 | MIPI_CSI_CLK_P | MIPI_VDDA_1P8 | | | MIPI_CSI_CLK_P | |
| A16 | MIPI_CSI_D0_N | MIPI_VDDA_1P8 | | | MIPI_CSI_D0_N | |
| B16 | MIPI_CSI_D0_P | MIPI_VDDA_1P8 | | | MIPI_CSI_D0_P | |

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