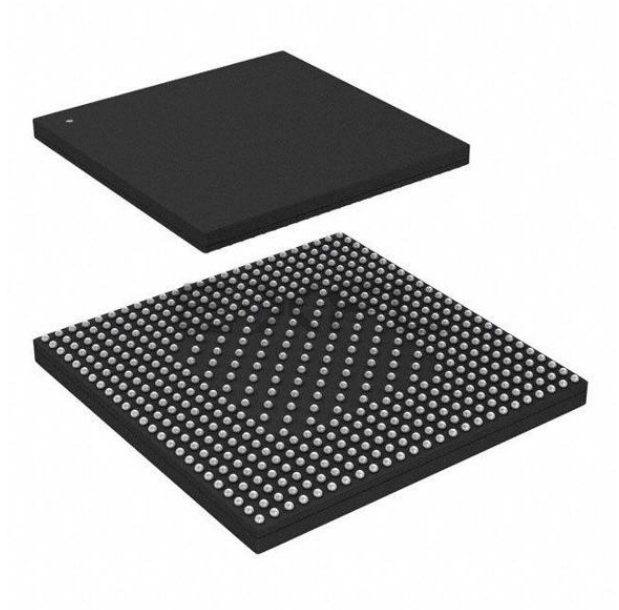

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Understanding Embedded - Microprocessors

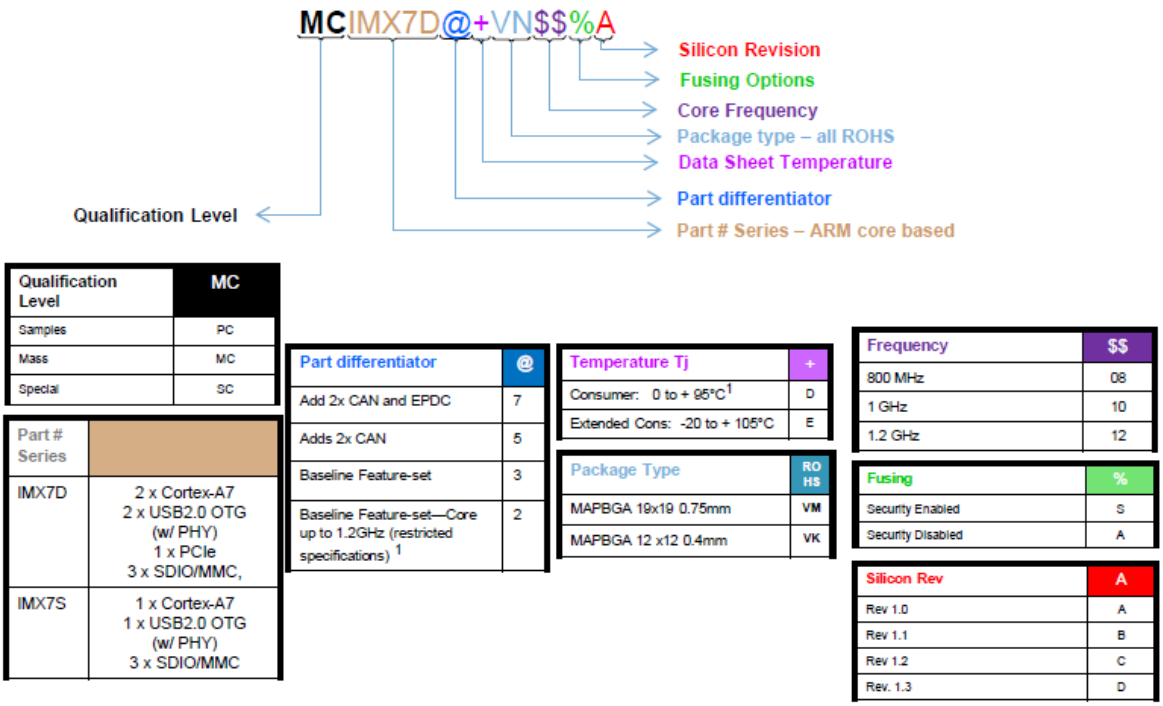
Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A7, ARM® Cortex®-M4
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.2GHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR2, LPDDR3, DDR3, DDR3L
Graphics Acceleration	No
Display & Interface Controllers	Keypad, LCD, MIPI
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (1), USB 2.0 OTG + PHY (2)
Voltage - I/O	1.8V, 3.3V
Operating Temperature	0°C ~ 85°C (TJ)
Security Features	A-HAB, ARM TZ, CAAM, CSU, SJC, SNVS
Package / Case	541-LFBGA
Supplier Device Package	541-MAPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx7d2dvm12sc

Figure 1 describes the part number nomenclature so that the users can identify the characteristics of the specific part number.



1 Restricted electrical specifications for parts with CPU maximum frequency of 1.2 GHz:

- Temperature range 0 to 85 degrees C (see Table 1)
- VDD_ARM requirements (see Table 9)

Figure 1. Part number nomenclature—i.MX 7Dual family of processors

1.2 Features

The i.MX 7Dual family of processors is based on ARM Cortex-A7 MPCore™ Platform, which has the following features:

- Two ARM Cortex-A7 Cores (with TrustZone® technology)
- The core configuration is symmetric, where each core includes:
  - 32 KByte L1 Instruction Cache
  - 32 KByte L1 Data Cache
  - Private Timer and Watchdog
  - NEON MPE (media processing engine) coprocessor

The ARM Cortex-A7 Core complex shares:

- General interrupt controller (GIC) with 128 interrupt support
- Global timer
- Snoop control unit (SCU)
- 512 KB unified I/D L2 cache

Table 3. Special signal considerations(continued)

Signal Name	Remarks
DRAM_VREF	When using DDR_VREF with DDR I/O, the nominal reference voltage must be half of the NVCC_DRAM supply. The user must tie DDR_VREF to a precision external resistor divider. Use a 1 kΩ 0.5% resistor to GND and a 1 kΩ 0.5% resistor to NVCC_DRAM. Shunt each resistor with a closely-mounted 0.1 µF capacitor. To reduce supply current, a pair of 1.5 kΩ 0.1% resistors can be used. Using resistors with recommended tolerances ensures the ± 2% DDR_VREF tolerance (per the DDR3 specification) is maintained when four DDR3 ICs plus the i.MX 7Dual are drawing current on the resistor divider. It is recommended to use regulated power supply for “big” memory configurations (more than eight devices)
ZQPAD	DRAM calibration resistor 240 Ω 1% used as reference during DRAM output buffer driver calibration should be connected between this pad and GND.
PCIE_VPH/PCIE_VPH_TX/ PCIE_VPH_RX	Short these pins to VDDA_PHY1P8 if using PCIe. User can tie these pins to ground if not using PCIe.
PCIE_VP/PCIE_VP_TX/PC IE_VP_RX	Short these pins to VDDD_1P0CAP if using PCIe. User can tie these pins to ground with a 10 KΩ resistor if not using PCIe.
VDDA_MIPI_1P8	Short these pins to VDDA_PHY_1P8 if using MIPI. User can leave these pins floating or grounded if not using MIPI.
VDD_MIPI_1P0	Short these pins to VDDD_1P0_CAP if using MIPI. User can leave these pins floating or grounded if not using MIPI.
GPANAIO	This signal is reserved for manufacturing use only. User must leave this connection floating.
JTAG_*nnnn*	The JTAG interface is summarized in Table 4. Use of external resistors is unnecessary. However, if external resistors are used, the user must ensure that the on-chip pull-up/down configuration is followed. For example, do not use an external pull down on an input that has on-chip pull-up.
	JTAG_TDO is configured with a keeper circuit such that the floating condition is eliminated if an external pull resistor is not present. An external pull resistor on JTAG_TDO is detrimental and should be avoided.
	JTAG_MOD is referenced as SJC_MOD in the *i.MX 7Dual Application Processor Reference Manual* (IMX7DRM). Both names refer to the same signal. JTAG_MOD must be externally connected to GND for normal operation. Termination to GND through an external pull-down resistor (such as 1 kΩ) is allowed. JTAG_MOD set to high configures the JTAG interface to a mode compatible with the IEEE 1149.1 standard. JTAG_MOD set to low configures the JTAG interface for common SW debug adding all the system TAPs to the chain.
NC	Do not connect. These signals are reserved and should be floated by the user.
POR_B	This cold reset negative logic input resets all modules and logic in the IC. May be used in addition to internally generated power on reset signal (logical AND, both internal and external signals are considered active low).
ONOFF	In Normal mode, may be connected to ON/OFF button (De-bouncing provided at this input). Internally this pad is pulled up. Short connection to GND in OFF mode causes internal power management state machine to change state to ON. In ON mode short connection to GND generates interrupt (intended to SW controllable power down). Long above ~5s connection to GND causes “forced” OFF.
TEST_MODE	TEST_MODE is for factory use. This signal is internally connected to an on-chip pull-down device. The user must tie this signal to GND.

Table 5. Recommended connections for unused analog interfaces(continued)

Module	Package Net Name	Recommendation if Unused
PCIe	PCIE_REFCLKIN_N, PCIE_REFCLKIN_P, PCIE_REFCLKOUT_N, PCIE_REFCLKOUT_P, PCIE_RX_N, PCIE_RX_P, PCIE_TX_N, PCIE_TX_P	Floating
	PCIE_VP,PCIE_VP_RX,PCIE_VP_TX, PCIE_VPH,PCIE_VPH_RX,PCIE_VPH_TX, PCIE_REXT	Tie to ground
SNVS	SNVS_TAMPER00, SNVS_TAMPER01, SNVS_TAMPER02, SNVS_TAMPER03, SNVS_TAMPER04, SNVS_TAMPER05, SNVS_TAMPER06, SNVS_TAMPER07, SNVS_TAMPER08, SNVS_TAMPER09	Float—configure with software
Temperature sensor	TEMPSENSOR_REXT	Tie to ground or pulldown with 100 KΩ resistor
	TEMPSENSOR_RESERVE	Floating
	VDD_TEMPSENSOR_1P8	1.8 V
USB HSIC	VDD_USB_H_1P2	Tie to ground
	USB_H_DATA, USB_H_STROBE	Floating
USB OTG1	VDD_USB_OTG1_3P3_IN, VDD_USB_OTG1_1P0_CAP	Tie to ground
	USB_OTG1_VBUS, USB_OTG1_DP, USB_OTG1_DN, USB_OTG1_ID, USB_OTG1_REXT, USB_OTG1_CHD_B	Floating
USB OTG2	VDD_USB_OTG2_3P3_IN, VDD_USB_OTG2_1P0_CAP	Tie to ground
	USB_OTG2_VBUS, USB_OTG2_DP, USB_OTG2_DN, USB_OTG2_ID, USB_OTG2_REXT	Floating

4 Electrical characteristics

This section provides the device and module-level electrical characteristics for the i.MX 7Dual family of processors.

4.1 Chip-level conditions

This section provides the device-level electrical characteristics for the IC. See Table 6 for a quick reference to the individual tables and sections.

Table 6. i.MX 7Dual Chip-level conditions

For these characteristics, …	Topic appears …
Absolute maximum ratings	on page 21
FPBGA case “X” and case “Y” package thermal resistance	on page 22
Operating ranges	on page 23
External clock sources	on page 25

The typical values shown in Table 11 are required for use with NXP BSPs to ensure precise time keeping and USB operation. For RTC_XTALI operation, two clock sources are available. If there is not an externally applied oscillator to RTC_XTALI, the internal oscillator takes over.

- On-chip 32 kHz RC oscillator—this clock source has the following characteristics:
  - Approximately 25 µA more I_{DD} than crystal oscillator
  - Approximately ±10% tolerance
  - No external component required
  - Starts up faster than 32 kHz crystal oscillator
  - Three configurations for this input:
    - External oscillator
    - External crystal coupled to RTC_XTALI and RTC_XTALO
    - Internal oscillator

External crystal oscillator with on-chip support circuit:

- At power up, RC oscillator is utilized. After crystal oscillator is stable, the clock circuit switches over to the crystal oscillator automatically.
- Higher accuracy than RC oscillator
- If no external crystal is present, then the RC oscillator is utilized

The decision of choosing a clock source should be taken based on real-time clock use and precision timeout.

4.1.5 Maximum supply currents

The Power Virus numbers shown in Table 12 represent a use case designed specifically to show the maximum current consumption possible. All cores are running at the defined maximum frequency and are limited to L1 cache accesses only to ensure no pipeline stalls. Although a valid condition, it would have a very limited practical use case, if at all, and be limited to an extremely low duty cycle unless the intention was to specifically show the worst case power consumption.

The MC3xPF3000xxxx, NXP's power management IC targeted for the i.MX 7Dual family of processors, supports the Power Virus mode operating at 1% duty cycle. Higher duty cycles are allowed, but a robust thermal design is required for the increased system power dissipation.

Table 12 represents the maximum momentary current transients on power lines, and should be used for power supply selection. Maximum currents are higher by far than the average power consumption of typical use cases. For typical power consumption information, see the application note, *i.MX 7DS Power Consumption Measurement* (AN5383).

Table 12. Maximum supply currents

Power Rail	Source	Conditions	Max Current	Unit
VDD_ARM	From PMIC	—	500	mA
VDD_SOC	From PMIC	—	1000	mA

Table 12. Maximum supply currents(continued)

Power Rail	Source	Conditions	Max Current	Unit
DRAM_VREF	From PMIC	—	30	mA
NVCC_DRAM_CKE	From PMIC	—	30	mA
NVCC_DRAM	From PMIC	—	—[3]	mA

1 The actual maximum current drawn from VDDA_1P8_IN is as shown plus any additional current drawn from the VDDD_1P0_CAP, VDD_1P2_CAP, VDDA_PHY_1P8 outputs, depending on actual application configuration (for example, VDD_MIPI_1P0, VDD_USB_H_1P2 and PCIE_VP/VPH supplies).

2 General equation for estimated, maximal power consumption of an I/O power supply:

$I_{max} = N \times C \times V \times (0.5 \times F)$

where:

N = Number of I/O pins supplied by the power line
C = Equivalent external capacitive load
V = IO voltage
$(0.5 \times F)$ = Data change rate, up to 0.5 of the clock rate (F)
In this equation, I_{max} is in amps, C in farads, V in volts, and F in hertz.

3 The DRAM power consumption is dependent on several factors, such as external signal termination. DRAM power calculators are typically available from the memory vendors. They take into account factors such as signal termination. See the application note, *i.MX 7DS Power Consumption Measurement* (AN5383) for examples of DRAM power consumption during specific use case scenarios.

4.1.6 Power modes

The i.MX 7Dual has the following power modes:

- OFF mode: all power rails are off
- SNVS mode: only RTC and tamper detection logic is active
- LPSR mode: an extension of SNVS mode, with 16 GPIOs in low power state retention mode
- RUN Mode: all external power rails are on, CPU is active and running, other internal module can be on/off based on application;
- Low Power mode (System Idle, Low Power Idle, and Deep Sleep): most external power rails are still on, CPU is in WFI state or power gated, most of the internal modules are clock gated or power gated

When LPSR mode is not needed for the application, the VDD_LPSR can be connected to VDDA_1P8 and NVCC_GPIO1/2 can be connected to the same power supply as NVCC_XXX for other GPIO banks.

In LPSR mode, the supported wakeup source are RTC alarm, ONOFF event, security/tamper and also the 16 GPIO pads.

4.1.6.4 RUN Mode

In RUN mode, the CPU is active and running, and the analog / digital peripheral modules inside the processor will be enabled. In this mode, all the external power rails to the processor have to be ON and the SoC will be able to draw as many current as listed in the Table 5 Maximum Power Requirement.

In this mode, the PMIC should allow SoC to change the voltage of power rails through I2C/SPI interface. Typically, when the CPU is doing DVFS, it switches the VDD_ARM voltage according to Table 9 when the CPU's frequency is switching between 1 GHz and 800 MHz (or below).

4.1.6.5 Low Power Mode

When the CPU is not running, the processor can enter low power mode. i.MX 7Dual processor supports a very flexible set of power mode configurations in low power mode.

Typically there are 3 low power modes used, System IDLE, Low Power IDLE and SUSPEND:

- System IDLE—This is a mode that the CPU can automatically enter when there is no thread running. All the peripherals can keep working and the CPU's state is retained so the interrupt response can be very short. The cores are able to individually enter the WAIT state.
- Low Power IDLE—This mode is for the case when the system needs to have lower power but still keep some of the peripherals alive. Most of the peripherals, analog modules, and PHYs are shut off; see Table 5-5, "Low Power Mode Definition," in the *i.MX 7Dual Application Processor Reference Manual* (IMX7DRM) for details. The interrupt response in this mode is expected to be longer than the System IDLE, but its power is much lower.
- Suspend—This mode has the greatest power savings; all clocks, unused analog/PHYs, and peripherals are off. The external DRAM stays in Self-Refresh mode. The exit time from this mode is much longer.

In System IDLE and Low Power IDLE mode, the voltage on external power supplies remains the same as in RUN mode, so the external PMIC is not aware of the state of the processor. If any low-power setting needs to be applied to PMIC, it is done through the I2C/SPI interface before the processor enters a low-power mode.

When the processor enters SUSPEND mode, it will assert the PMIC_STBY_REQ signal to PMIC. When this signal is asserted, the processor allows the PMIC to shut off VDD_ARM externally. However, in some application scenario, SW want to keep the data in L2 Cache to avoid performance impact on cache miss. In this case, the VDD_ARM cannot be shut off. To support both scenarios, the PMIC should have an option to shut off or keep VDD_ARM when it receives the PMIC_STBY_REQ. This should be configured through I2C/SPI interface before the processor enters SUSPEND mode.

Except the VDD_ARM, the other power rails have to keep active in SUSPEND mode. Since the current on each power rail is greatly reduced in this mode, PMIC can enter its own low power mode to get extra

Table 20. PCIe DC electrical characteristics

Parameter	Description		Min	Typ	Max	Unit
V_{DD}	Power Supply Voltage (VDD of 1.0 V nominal gate oxide /1.8 V for thick gate oxide)		1.0 - 5%	1.0	1.0 + 5%	V
			1.8 - 5%	1.8	1.8 + 5%	V
PD	Power Consumption	Normal	—	130	—	mW
		Partial Mode	—	108	—	mW
		Slumber Mode	—	7	—	mW
		Full Powerdown	—	0.2	—	mW

Table 21. PCIe PHY high-speed characteristics

High Speed I/O Characteristics						
Description	**Symbol**	**Speed**	**Min.**	**Typ.**	**Max.**	**Unit**
Unit Interval	UI	1.5 Gbps	—	666.67	—	ps
		2.5 Gbps	—	400	—	
		3.0 Gbps	—	333.33	—	
		5.0 Gbps	—	200	—	
		6.0 Gbps	—	166.67	—	
TX Serial output rise time (20% to 80%)	T_{TXRISE}	1.5 Gbps	50	—	273	ps
		2.5 Gbps	50	—	—	
		3.0 Gbps	50	—	136	
		5.0 Gbps	30	—	—	
		6.0 Gbps	33	—	80	
TX Serial output fall time (80% to 20%)	T_{TXFALL}	1.5 Gbps	50	—	273	ps
		2.5 Gbps	50	—	—	
		3.0 Gbps	50	—	136	
		5.0 Gbps	30	—	—	
		6.0 Gbps	33	—	80	
TX Serial data output voltage (Differential, pk–pk)	ΔV_{TX}	1.5 Gbps	400	—	600	mVp–p
		2.5 Gbps	400	—	1200	
		3.0 Gbps	400	—	700	
		5.0 Gbps	400	—	1200	
		6.0 Gbps	240	—	900	

DDRMC operation with the standards stated above is contingent upon the board DDR design adherence to the DDR design and layout requirements stated in the hardware development guide for the i.MX 7 application processor.

Table 30. DC input logic level

Characteristics	Symbol	Min	Max	Unit
DC input logic high[1]	$V_{IH(DC)}$	V_{REF} +100	—	mV
DC input logic low[1]	$V_{IL(DC)}$	—	V_{REF} –100	

1 It is the relationship of the V_{DDQ} of the driving device and the V_{REF} of the receiving device that determines noise margins. However, in the case of V_{IH}(DC) max (that is, input overdrive), it is the V_{DDQ} of the receiving device that is referenced.

Table 31. Output DC current drive

Characteristics	Symbol	Min	Max	Unit
Output minimum source DC current[1]	I_{OH}(DC)	–4	—	mA
Output minimum sink DC current[1]	I_{OL}(DC)	4	—	mA
DC output high voltage(I_{OH} = –0.1mA)[1,2]	V_{OH}	0.9 × V_{DDQ}	—	V
DC output low voltage(I_{OL} = 0.1mA)[1,2]	V_{OL}	—	0.1 × V_{DDQ}	V

1 When DDS=[111] and without ZQ calibration.

2 The values of V_{OH} and V_{OL} are valid only for 1.2 V range.

Table 32. Input DC current

Characteristics	Symbol	Min	Max	Unit
High level input current[1,2]	I_{IH}	–25	25	μA
Low level input current[1,2]	I_{IL}	–25	25	μA

1 The values of V_{OH} and V_{OL} are valid only for 1.2 V range.

2 Driver Hi-Z and input power-down (PD=High)

4.5.2.1 LPDDR3 mode I/O DC parameters

Table 33. LPDDR3 I/O DC electrical parameters

Parameters	Symbol	Test Conditions	Min	Max	Unit
High-level output voltage	VOH	Ioh= -0.1mA	0.9 × OVDD	—	V
Low-level output voltage	VOL	Iol= 0.1mA	—	0.1 × OVDD	V
Input Reference Voltage	Vref	—	0.49 × OVDD	0.51 × OVDD	V

Table 35. Maximum input cell delay time

Cell name	Max Delay PAD → Y (ns)		
	VDD=1.65 V T=125°C Process=Slow	VDD=2.3 V T=125°C Process=Slow	VDD=3.0 V T=125°C Process=Slow
PBIDIRPUD_E33_33_NT_DR	0.9	1.5	1.4

Table 36. Output cell delay time for fixed load

Parameter				Simulated Cell Delay A → PAD (ns)								
				VDD = 1.65 V, T = 125°C			VDD = 2.3 V, T = 125°C			VDD = 3.0 V, T = 125°C		
DS0	DS1	SR	Driver Type	CL= 5 pF	CL= 10 pF	CL= 40 pF	CL= 5 pF	CL= 10 pF	CL= 40 pF	CL= 5 pF	CL= 10 pF	CL= 40 pF
0	0	1	1× Slow Slew	4.9	6.0	12.5	4.8	6.1	11.9	5.4	6.7	14.6
0	0	0	1× Fast Slew	3.8	4.7	11.2	3.8	5.1	12.8	4.2	5.3	13.5
0	1	1	2× Slow Slew	4.1	4.8	8.2	4.2	4.9	8.8	4.5	5.3	9.1
0	1	0	2× Fast Slew	2.8	3.3	6.4	2.9	3.4	7.2	3.1	3.7	7.2
1	0	1	4× Slow Slew	3.6	4.1	6.0	3.7	4.1	6.4	3.9	4.4	6.6
1	0	0	4× Fast Slew	2.2	2.5	4.1	2.3	2.6	4.6	2.4	2.8	4.8
1	1	1	6× Slow Slew	3.6	4.0	5.5	3.6	4.0	5.9	3.8	4.3	6.2
1	1	0	6× Fast Slew	2.0	2.3	3.4	2.1	2.3	3.8	2.2	2.5	3.9

Table 37. Maximum frequency of operation for input

Maximum frequency (MHz)		
VDD = 1.8 V, CL = 50 fF	VDD=2.5 V, CL =5 0 fF	VDD = 3.3 V, CL = 50 fF
550	400	430

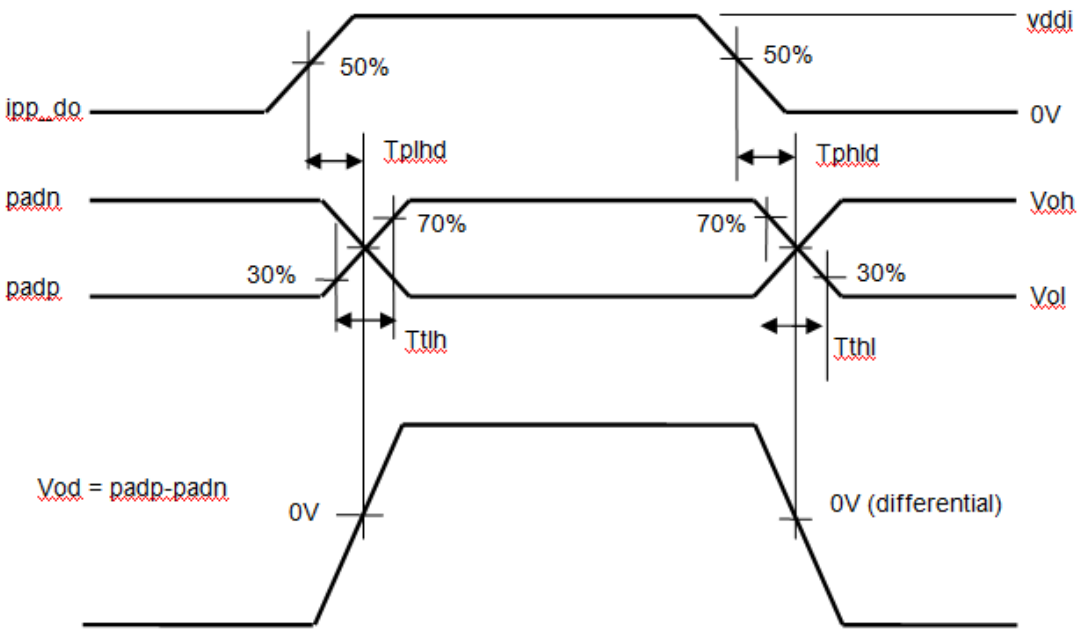


Figure 8. Differential LVDS driver transition time waveform

Table 39 shows the AC parameters for clock I/O.

Table 39. I/O AC Parameters of LVDS Pad

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit	Notes
Tphld	Output Differential propagation delay high to low	Rload=100 Ω between padp and padn, Cload = 2pF	—	—	0.61	ns	1
Tplhd	Output Differential propagation delay low to high		—	—	0.61		
Ttlh	Output Transition time low to high		—	—	0.17		2
Tthl	Output Transition time high to low		—	—	0.17		
Tphlr	Input Differential propagation delay high to low	Rload=100 Ω between padp and padn, Cload on ipp_ind=0.1 pF	—	—	0.33	ns	3
Tplhr	Input Differential propagation delay low to high		—	—	0.33		
Ttx	Transmitter startup time (ipp-obe low to high)	—	—	—	40	ns	4
F	Operating frequency	—	—	500	1000	MHz	—

1 At WCS, 125C, 1.62 V ovdd, 0.9 V vddi. Measurement levels are 50-50%. Output differential signal measured.

2 WCS, 125C, 1.62 V ovdd, 0.9 V vddi. Measurement levels are 20-80%. Output differential signal measured

3 At WCS, 125C, 1.62 V ovdd, 0.9 V vddi. Measurement levels are 50-50%.

4 TX startup time is defined as the time taken by transmitter for settling after its ipp_obe has been asserted. It is to stabilize the current reference. Functionality is guaranteed only after the startup time

4.7 Output buffer impedance parameters

This section defines the I/O impedance parameters of the i.MX 7Dual family of processors for the following I/O types:

- Double Data Rate I/O (DDR) for LPDDR2, LPDDR3, and DDR3/DDR3L modes
- Differential I/O (CCM_CLK1)
- USB battery charger detection open-drain output (USB_OTG1_CHD_B)

NOTE

DDR I/O output driver impedance is measured with “long” transmission line of impedance Ztl attached to I/O pad and incident wave launched into transmission line. Rpu/Rpd and Ztl form a voltage divider that defines specific voltage of incident wave relative to OVDD. Output driver impedance is calculated from this voltage divider (see Figure 9).

[1] t is the maximum EIM logic (axi_clk) cycle time. The maximum allowed axi_clk frequency depends on the fixed/non-fixed latency configuration, whereas the maximum allowed EIM_BCLK frequency is:

—Fixed latency for both read and write is 132 MHz.

—Variable latency for read only is 132 MHz.

—Variable latency for write only is 52 MHz.

In variable latency configuration for write, if BCD = 0 & WBCDD = 1 or BCD = 1, axi_clk must be 104 MHz. Write BCD = 1 and 104 MHz axi_clk, will result in a EIM_BCLK of 52 MHz. When the clock branch to EIM is decreased to 104 MHz, other buses are impacted which are clocked from this source. See the CCM chapter of the *i.MX 7Dual Application Processor Reference Manual* (IMX7DRM) for a detailed clock tree description.

[2] EIM_BCLK parameters are being measured from the 50% point, that is, high is defined as 50% of signal value and low is defined as 50% as signal value.

[3] For signal measurements, “High” is defined as 80% of signal value and “Low” is defined as 20% of signal value.

Figure 14 to Figure 17 provide few examples of basic EIM accesses to external memory devices with the timing parameters mentioned previously for specific control parameters settings.

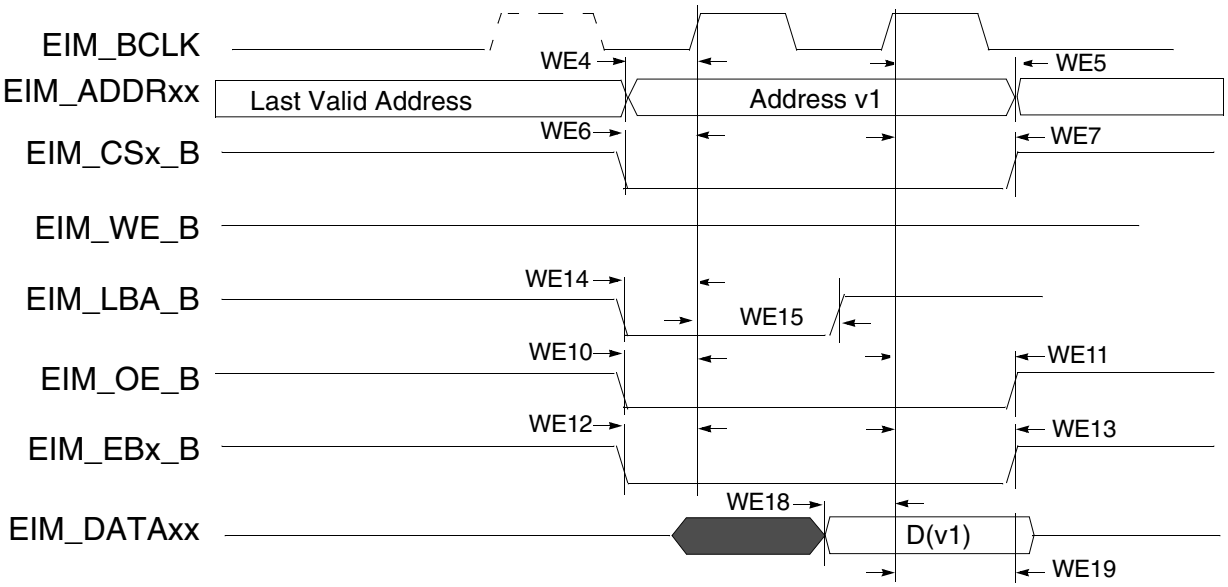


Figure 14. Synchronous memory read access, WSC=1

Table 46. EIM asynchronous timing parameters table relative chip to select(continued)

Ref No.	Parameter	Determination by Synchronous measured parameters[1]	Min	Max	Unit
WE38	EIM_EBx_B Invalid to EIM_CSx_B Invalid (Read access)	WE7 – WE13 + (RBEN – RCSN)	—	3 – (RBEN– RCSN)	ns
WE39	EIM_CSx_B Valid to EIM_LBA_B Valid	WE14 – WE6 + (ADVA – CSA)	—	3 + (ADVA – CSA)	ns
WE40	EIM_LBA_B Invalid to EIM_CSx_B Invalid (ADVL is asserted)	WE7 – WE15 – CSN	—	3 – CSN	ns
WE40A (muxed A/D)	EIM_CSx_B Valid to EIM_LBA_B Invalid	WE14 – WE6 + (ADVN + ADVA + 1 – CSA)	–3 + (ADVN + ADVA + 1 – CSA)	3 + (ADVN + ADVA + 1 – CSA)	ns
WE41	EIM_CSx_B Valid to Output Data Valid	WE16 – WE6 – WCSA	—	3 – WCSA	ns
WE41A (muxed A/D)	EIM_CSx_B Valid to Output Data Valid	WE16 – WE6 + (WADVN + WADVA + ADH + 1 – WCSA)	—	3 + (WADVN + WADVA + ADH + 1 – WCSA)	ns
WE42	Output Data Invalid to EIM_CSx_B Invalid	WE17 – WE7 – CSN	—	3 – CSN	ns
MAXCO	Output maximum delay from internal driving EIM_ADDRxx/control FFs to chip outputs	10	—	—	ns
MAXCSO	Output maximum delay from CSx internal driving FFs to CSx out	10	—	—	ns
MAXDI	EIM_DATAxx maximum delay from chip input data to its internal FF	5	—	—	ns
WE43	Input Data Valid to EIM_CSx_B Invalid	MAXCO – MAXCSO + MAXDI	MAXCO – MAXCSO + MAXDI	—	ns
WE44	EIM_CSx_B Invalid to Input Data invalid	0	0	—	ns
WE45	EIM_CSx_B Valid to EIM_EBx_B Valid (Write access)	WE12 – WE6 + (WBEA – WCSA)	—	3 + (WBEA – WCSA)	ns
WE46	EIM_EBx_B Invalid to EIM_CSx_B Invalid (Write access)	WE7 – WE13 + (WBEN – WCSN)	—	–3 + (WBEN – WCSN)	ns

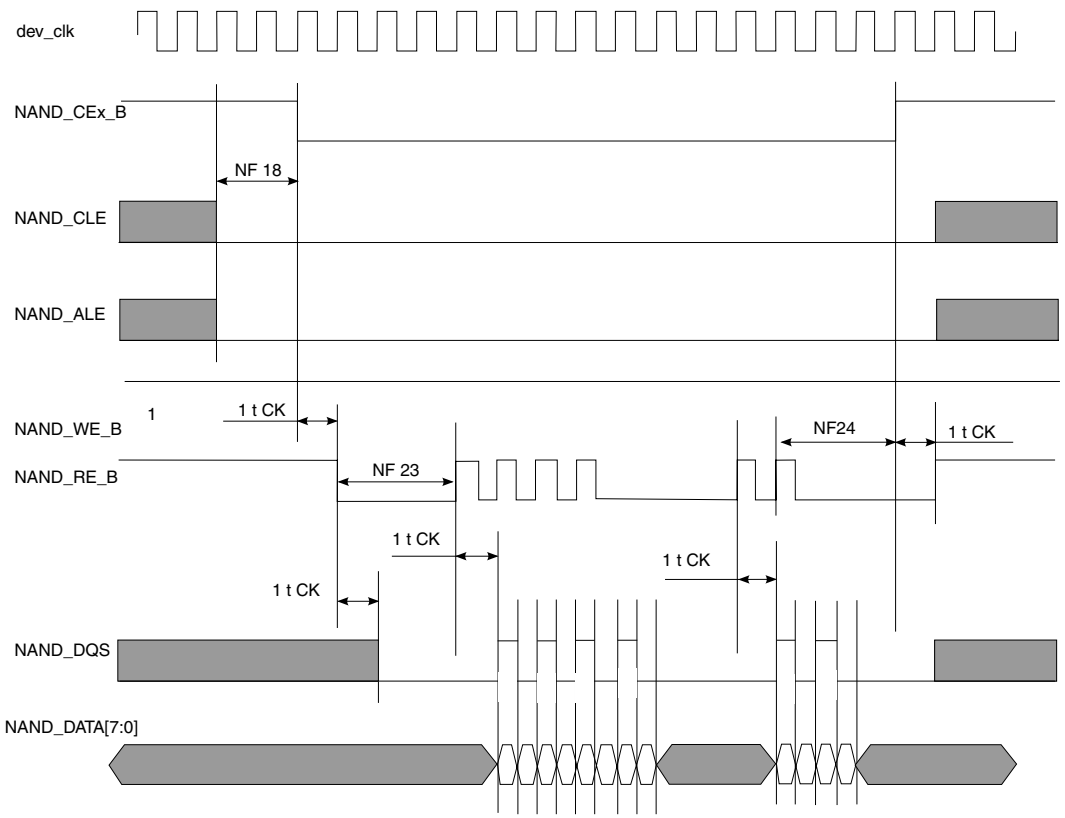


Figure 43. Toggle mode data read timing

Table 58. Toggle mode timing parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF1	NAND_CLE setup time	tCLS	(AS + DS) × T - 0.12 [see note[2]s,[3]]		
NF2	NAND_CLE hold time	tCLH	DH × T - 0.72 [see note[2]]		
NF3	NAND_CE0_B setup time	tCS	(AS + DS) × T - 0.58 [see notes,[2]]		
NF4	NAND_CE0_B hold time	tCH	DH × T - 1 [see note[2]]		
NF5	NAND_WE_B pulse width	tWP	DS × T [see note[2]]		
NF6	NAND_ALE setup time	tALS	(AS + DS) × T - 0.49 [see notes,[2]]		
NF7	NAND_ALE hold time	tALH	DH × T - 0.42 [see note[2]]		
NF8	Command/address NAND_DATAxx setup time	tCAS	DS × T - 0.26 [see note[2]]		
NF9	Command/address NAND_DATAxx hold time	tCAH	DH × T - 1.37 [see note[2]]		
NF18	NAND_CEx_B access time	tCE	CE_DELAY × T [see notes[4,2]]	—	ns
NF22	clock period	tCK	—	—	ns
NF23	preamble delay	tPRE	PRE_DELAY × T [see notes[5,2]]	—	ns
NF24	postamble delay	tPOST	POST_DELAY × T +0.43 [see note[2]]	—	ns

4.10.2.5 SDR50/SDR104 AC timing

Figure 50 depicts the timing of SDR50/SDR104, and Table 65 lists the SDR50/SDR104 timing characteristics.

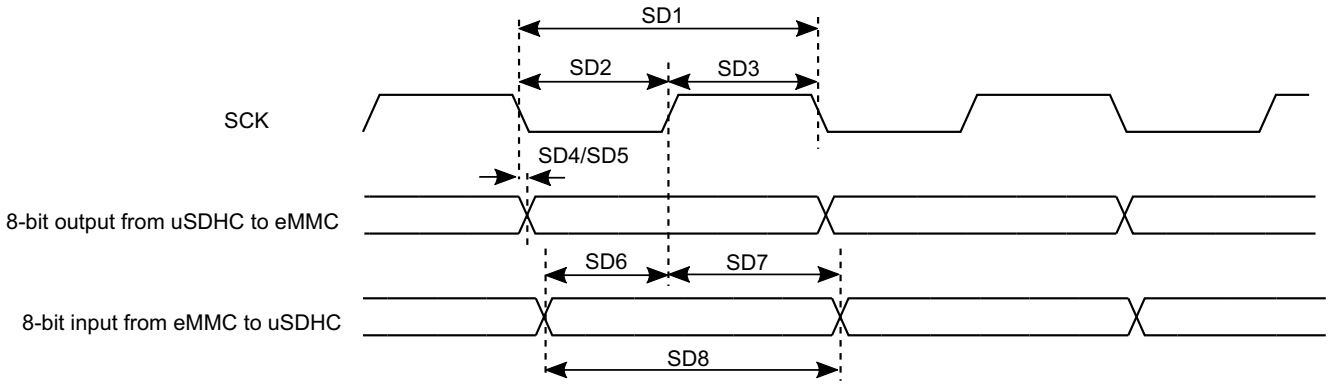


Figure 50. SDR50/SDR104 timing

Table 65. SDR50/SDR104 interface timing specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency Period	t_{CLK}	5	—	ns
SD2	Clock Low Time	t_{CL}	$0.46 \times t_{CLK}$	$0.54 \times t_{CLK}$	ns
SD3	Clock High Time	t_{CH}	$0.46 \times t_{CLK}$	$0.54 \times t_{CLK}$	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR50 (Reference to CLK)					
SD4	uSDHC Output Delay	t_{OD}	–3	1	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR104 (Reference to CLK)					
SD5	uSDHC Output Delay	t_{OD}	–1.6	1	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR50 (Reference to CLK)					
SD6	uSDHC Input Setup Time	t_{ISU}	2.4	—	ns
SD7	uSDHC Input Hold Time	t_{IH}	1.4	—	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR104 (Reference to CLK)[1]					
SD8	Card Output Data Window	t_{ODW}	$0.5*t_{CLK}$	—	ns

[1]Data window in SDR100 mode is variable.

Table 66. MII receive signal timing

ID	Characteristic[1]	Min.	Max.	Unit
M1	ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER to ENET_RX_CLK setup	5	—	ns
M2	ENET_RX_CLK to ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER hold	5	—	ns
M3	ENET_RX_CLK pulse width high	35%	65%	ENET_RX_CLK period
M4	ENET_RX_CLK pulse width low	35%	65%	ENET_RX_CLK period

[1] ENET_RX_EN, ENET_RX_CLK, and ENET0_RXD0 have the same timing in 10 Mbps 7-wire interface mode.

4.10.3.1.2 MII transmit signal timing (ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER, and ENET_TX_CLK)

The transmitter functions correctly up to an ENET_TX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the ENET_TX_CLK frequency.

Figure 52 shows MII transmit signal timings. Table 67 describes the timing parameters (M5–M8) shown in the figure.

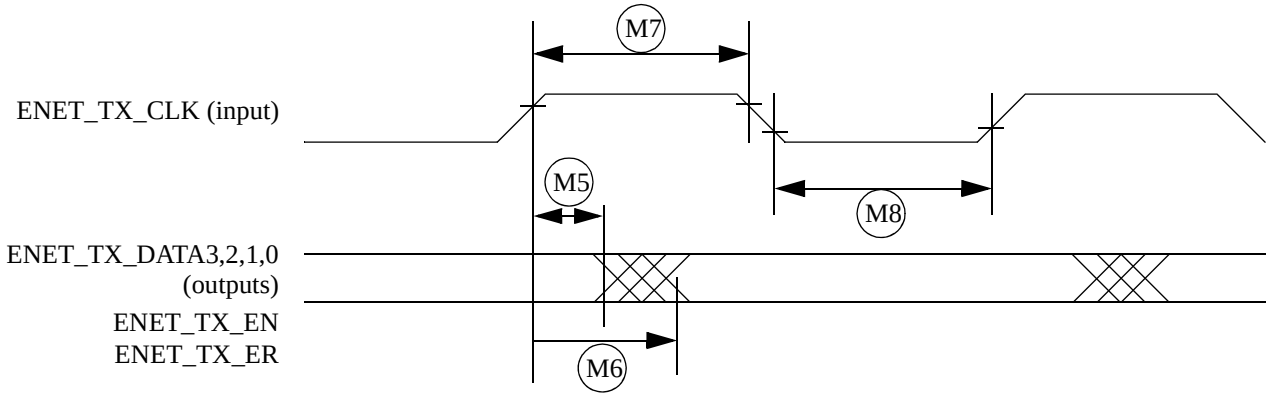


Figure 52. MII transmit signal timing diagram

Table 67. MII transmit signal timing

ID	Characteristic[1]	Min.	Max.	Unit
M5	ENET_TX_CLK to ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER invalid	5	—	ns
M6	ENET_TX_CLK to ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER valid	—	20	ns
M7	ENET_TX_CLK pulse width high	35%	65%	ENET_TX_CLK period
M8	ENET_TX_CLK pulse width low	35%	65%	ENET_TX_CLK period

[1] ENET_TX_EN, ENET_TX_CLK, and ENET0_TXD0 have the same timing in 10-Mbps 7-wire interface mode.

Table 70. RMII signal timing

ID	Characteristic	Min.	Max.	Unit
M16	ENET_CLK pulse width high	35%	65%	ENET_CLK period
M17	ENET_CLK pulse width low	35%	65%	ENET_CLK period
M18	ENET_CLK to ENET0_TXD[1:0], ENET_TX_DATA invalid	4	—	ns
M19	ENET_CLK to ENET0_TXD[1:0], ENET_TX_DATA valid	—	15	ns
M20	ENET_RX_DATAD[1:0], ENET_RX_EN(ENET_RX_EN), ENET_RX_ER to ENET_CLK setup	4	—	ns
M21	ENET_CLK to ENET_RX_DATAD[1:0], ENET_RX_EN, ENET_RX_ER hold	2	—	ns

4.10.3.3 Signal switching specifications

The following timing specifications meet the requirements for RGMII interfaces for a range of transceiver devices.

Table 71. RGMII signal switching specifications[1]

Symbol	Description	Min.	Max.	Unit
T_{cyc}[2]	Clock cycle duration	7.2	8.8	ns
T_{skewT}[3]	Data to clock output skew at transmitter	-500	500	ps
T_{skewR}[3]	Data to clock input skew at receiver	1	2.6	ns
Duty_G[4]	Duty cycle for Gigabit	45	55	%
Duty_T[4]	Duty cycle for 10/100T	40	60	%
Tr/Tf	Rise/fall time (20–80%)	—	0.75	ns

1 The timings assume the following configuration:
DDR_SEL = (11)b
DSE (drive-strength) = (111)b

2 For 10 Mbps and 100 Mbps, T_{cyc} will scale to 400 ns ±40 ns and 40 ns ±4 ns respectively.

3 For all versions of RGMII prior to 2.0; This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns and less than 2.0 ns will be added to the associated clock signal. For 10/100, the Max value is unspecified.

4 Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.

4.10.16 USB PHY parameters

This section describes the USB-OTG PHY parameters.

The USB PHY meets the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 OTG, USB Host with the amendments below (On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification is not applicable to Host port):

- USB ENGINEERING CHANGE NOTICE
  - Title: 5V Short Circuit Withstand Requirement Change
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- Errata for USB Revision 2.0 April 27, 2000 as of 12/7/2000
- USB ENGINEERING CHANGE NOTICE
  - Title: Pull-up/Pull-down resistors
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: Suspend Current Limit Changes
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: USB 2.0 Phase Locked SOFs
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification
  - Revision 2.0, version 1.1a, July 27, 2010
- Battery Charging Specification (available from USB-IF)
  - Revision 1.2, December 7, 2010

4.10.16.1 USB_OTG*_REXT reference resistor connection

The bias generation and impedance calibration process for the USB OTG PHYs requires connection of reference resistors 200 Ω 1% precision on each of USB_OTG1_REXT and USB_OTG2_REXT pads to ground.

4.10.16.2 USB_OTG_CHD_B USB battery charger detection external pullup resistor connection

The usage and external resistor connection for the USB_OTG_CHD_B pin are described in Table 3, Table 7, and Section 4.7.3, “USB battery charger detection driver impedance.”

Table 99. i.MX 7Dual 12 x 12 mm functional contact assignments(continued)

Ball	Ball Name	Power Group	Ball type[1]	Default Mode[1]	Default Function[1]	PD/PU
AD13	ONOFF	VDD_SNVS_IN			ONOFF	
AG13	PCIE_REFCLKIN_N	PCIE_VPH			PCIE_REFCLKIN_N	
AH13	PCIE_REFCLKIN_P	PCIE_VPH			PCIE_REFCLKIN_P	
AG11	PCIE_REFCLKOUT_N	PCIE_VPH			PCIE_REFCLKOUT_N	
AH11	PCIE_REFCLKOUT_P	PCIE_VPH			PCIE_REFCLKOUT_P	
Y16	PCIE_REXT	PCIE_VPH			PCIE_REXT	
AG16	PCIE_RX_N	PCIE_VPH_RX			PCIE_RX_N	
AH16	PCIE_RX_P	PCIE_VPH_RX			PCIE_RX_P	
AG14	PCIE_TX_N	PCIE_VPH_TX			PCIE_TX_N	
AG15	PCIE_TX_P	PCIE_VPH_TX			PCIE_TX_P	
AD11	CCM_PMIC_STBY_REQ	VDD_SNVS_IN	GPIO		CCM_PMIC_STBY_REQ	
Y03	POR_B	NVCC_GPIO1	GPIO	ALT0	POR_B	100K PU
AG09	RTC_XTALI	VDD_SNVS_1P8_CAP			RTC_XTALI	
AH09	RTC_XTALO	VDD_SNVS_1P8_CAP			RTC_XTALO	
D03	SAI1_MCLK	NVCC_SAI	GPIO	ALT5	GPIO6_IO[18]	100K PD
G04	SAI1_RXC	NVCC_SAI	GPIO	ALT5	GPIO6_IO[17]	100K PD
F03	SAI1_RXD	NVCC_SAI	GPIO	ALT5	GPIO6_IO[12]	100K PD
C04	SAI1_RXFS	NVCC_SAI	GPIO	ALT5	GPIO6_IO[16]	100K PD
F04	SAI1_TXC	NVCC_SAI	GPIO	ALT5	GPIO6_IO[13]	100K PD
G05	SAI1_TXD	NVCC_SAI	GPIO	ALT5	GPIO6_IO[15]	100K PD
F05	SAI1_TXFS	NVCC_SAI	GPIO	ALT5	GPIO6_IO[14]	100K PD
E06	SAI2_RXD	NVCC_SAI	GPIO	ALT5	GPIO6_IO[21]	100K PD
D04	SAI2_TXC	NVCC_SAI	GPIO	ALT5	GPIO6_IO[20]	100K PD
D06	SAI2_TXD	NVCC_SAI	GPIO	ALT5	GPIO6_IO[22]	100K PD
F06	SAI2_TXFS	NVCC_SAI	GPIO	ALT5	GPIO6_IO[19]	100K PD
A05	SD1_CD_B	NVCC_SD1	GPIO	ALT5	GPIO5_IO[0]	100K PD
B03	SD1_CLK	NVCC_SD1	GPIO	ALT5	GPIO5_IO[3]	100K PD
A02	SD1_CMD	NVCC_SD1	GPIO	ALT5	GPIO5_IO[4]	100K PD
B04	SD1_DATA0	NVCC_SD1	GPIO	ALT5	GPIO5_IO[5]	100K PD
A04	SD1_DATA1	NVCC_SD1	GPIO	ALT5	GPIO5_IO[6]	100K PD
B02	SD1_DATA2	NVCC_SD1	GPIO	ALT5	GPIO5_IO[7]	100K PD
B01	SD1_DATA3	NVCC_SD1	GPIO	ALT5	GPIO5_IO[8]	100K PD

Table 102. i.MX 7Dual 19 x 19 mm functional contact assignments(continued)

Ball	Ball Name	Power Group	Ball type[1]	Default Mode[1]	Default Function[1]	PD/PU
A14	MIPI_CSI_D1_N	MIPI_VDDA_1P8			MIPI_CSI_D1_N	
B14	MIPI_CSI_D1_P	MIPI_VDDA_1P8			MIPI_CSI_D1_P	
A19	MIPI_DSI_CLK_N	MIPI_VDDA_1P8			MIPI_DSI_CLK_N	
B19	MIPI_DSI_CLK_P	MIPI_VDDA_1P8			MIPI_DSI_CLK_P	
A20	MIPI_DSI_D0_N	MIPI_VDDA_1P8			MIPI_DSI_D0_N	
B20	MIPI_DSI_D0_P	MIPI_VDDA_1P8			MIPI_DSI_D0_P	
A18	MIPI_DSI_D1_N	MIPI_VDDA_1P8			MIPI_DSI_D1_N	
B18	MIPI_DSI_D1_P	MIPI_VDDA_1P8			MIPI_DSI_D1_P	
J13	MIPI_VDDA_1P8	MIPI_VDDA_1P8			MIPI_VDDA_1P8	
J15	MIPI_VDDD_1P0	MIPI_VDDD_1P0			MIPI_VDDD_1P0	
J17	MIPI_VDDD_1P0	MIPI_VDDD_1P0			MIPI_VDDD_1P0	
AC08	ONOFF	VDD_SNVS_IN			ONOFF	
AE10	PCIE_REFCLKIN_N	PCIE_VPH			PCIE_REFCLKIN_N	
AD10	PCIE_REFCLKIN_P	PCIE_VPH			PCIE_REFCLKIN_P	
AC10	PCIE_REFCLKOUT_N	PCIE_VPH			PCIE_REFCLKOUT_N	
AB10	PCIE_REFCLKOUT_P	PCIE_VPH			PCIE_REFCLKOUT_P	
AA13	PCIE_REXT	PCIE_VPH			PCIE_REXT	
AE11	PCIE_RX_N	PCIE_VPH_RX			PCIE_RX_N	
AD11	PCIE_RX_P	PCIE_VPH_RX			PCIE_RX_P	
AC11	PCIE_TX_N	PCIE_VPH_TX			PCIE_TX_N	
AB11	PCIE_TX_P	PCIE_VPH_TX			PCIE_TX_P	
AA10	PCIE_VP	PCIE_VP			PCIE_VP	
AA12	PCIE_VP_RX	PCIE_VP_RX			PCIE_VP_RX	
AA11	PCIE_VP_TX	PCIE_VP_TX			PCIE_VP_TX	
Y10	PCIE_VPH	PCIE_VPH			PCIE_VPH	
Y12	PCIE_VPH_RX	PCIE_VPH_RX			PCIE_VPH_RX	
Y11	PCIE_VPH_TX	PCIE_VPH_TX			PCIE_VPH_TX	
R06	POR_B	NVCC_GPIO1	GPIO	ALT0	POR_B	100K PU
AE06	RTC_XTALI	VDD_SNVS_1P8_CAP			RTC_XTALI	
AD06	RTC_XTALO	VDD_SNVS_1P8_CAP			RTC_XTALO	
E10	SAI1_MCLK	NVCC_SAI	GPIO	ALT5	GPIO6_IO[18]	100K PD
D12	SAI1_RXC	NVCC_SAI	GPIO	ALT5	GPIO6_IO[17]	100K PD