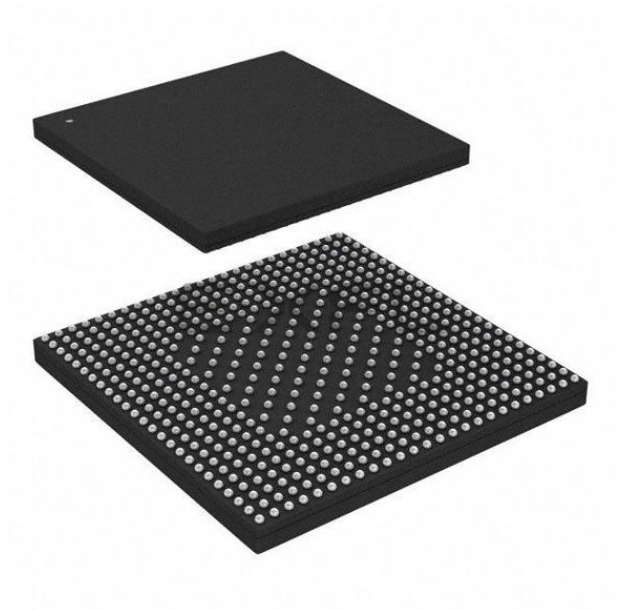

Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A7, ARM® Cortex®-M4
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR2, LPDDR3, DDR3, DDR3L
Graphics Acceleration	No
Display & Interface Controllers	Keypad, LCD, MIPI
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (1), USB 2.0 OTG + PHY (2)
Voltage - I/O	1.8V, 3.3V
Operating Temperature	0°C ~ 95°C (TJ)
Security Features	A-HAB, ARM TZ, CAAM, CSU, SJC, SNVS
Package / Case	488-TFBGA
Supplier Device Package	488-TFBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx7d7dvk10sc

- Advanced security—The processors deliver hardware-enabled security features that enable secure e-commerce, digital rights management (DRM), information encryption, secure boot, and secure software downloads. The security features are discussed in detail in the i.MX 7Dual security reference manual.
- Integrated power management—The processors integrate linear regulators and internally generate voltage levels for different power domains. This significantly simplifies system power management structure.

For a comprehensive list of the i.MX 7Dual features, see Section 1.2, "Features."

1.1 Ordering information

Table 1 provides examples of orderable sample part numbers covered by this data sheet.

Table 1. Orderable parts

Part Number	Options	Cortex-A7 CPU Speed Grade	Qualification Tier	Temperature (T_j)	Package
MCIMX7D7DVK10SD	EPDC, CAN 2 x Gigabit Ethernet 4 tamper pins 1 x ADC	1 GHz	Consumer[1]	0 to +95°C	12x12 mm 0.4 mm pitch BGA
MCIMX7D7DVM10SD	EPDC, CAN 2 x Gigabit Ethernet 10 tamper pins 2 x ADC	1 GHz	Consumer[1]	0 to +95°C	19x19 mm 0.75 mm pitch BGA
MCIMX7D5EVM10SD	No EPDC, CAN 2 x Gigabit Ethernet 10 tamper pins 2 x ADC	1 GHz	Industrial[2]	-20 to 105°C	19x19 mm 0.75 mm pitch BGA
MCIMX7D3DVK10SD	No EPDC, No CAN 2 x Gigabit Ethernet 4 tamper pins 1 x ADC	1 GHz	Consumer[1]	0 to +95°C	12x12 mm 0.4 mm pitch BGA
MCIMX7D3EVK10SD	No EPDC, No CAN 2 x Gigabit Ethernet 4 tamper pins 1 x ADC	1 GHz	Industrial[2]	–20 to +105°C	12x12 mm 0.4 mm pitch BGA
MCIMX7D2DVK12SD	No EPDC, No CAN 2 x Gigabit Ethernet 4 tamper pins 1x ADC	1.2 GHz	Consumer	0 to 85°C	12x12 mm 0.4 mm pitch BGA
MCIMX7D2DVM12SD	No EPDC, No CAN 2x Gigabit Ethernet 10 tamper pins 2x ADC	1.2 GHz	Consumer	0 to 85°C	19x19mm 0.75 mm pitch BGA

1 Consumer qualification grade assumes 5-year lifetime with 50% duty cycle.

2 Industrial qualification grade assumes 10-year lifetime with 100% duty cycle.

Table 2. i.MX 7Dual modules list(continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
eCSPI1 eCSPI2 eCSPI3 eCSPI4	Configurable SPI	Connectivity Peripherals	Full-duplex enhanced Synchronous Serial Interface, with data rate up to 52 Mbit/s. It is configurable to support Master/Slave modes, four chip selects to support multiple peripherals.
EIM	NOR-Flash /PSRAM interface	Connectivity Peripherals	The EIM NOR-FLASH / PSRAM provides: • Support for 16-bit (in Muxed I/O mode only) PSRAM memories (sync and async operating modes), at slow frequency • Support for 16-bit (in muxed and non-muxed I/O modes) NOR-Flash memories, at slow frequency • Multiple chip selects
ENET1 ENET2	Ethernet Controller	Connectivity peripherals	The Ethernet Media Access Controller (MAC) is designed to support 10/100/1000 Mbps Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The module has dedicated hardware to support the IEEE 1588 standard. See the ENET chapter of the *i.MX 7Dual Application Processor Reference Manual* (IMX7DRM) for details.
EPDC	Electrophoretic Display Controller	Connectivity peripherals	The EPDC is a feature-rich, low power, and high-performance direct-drive, active matrix EPD controller. It is specifically designed to drive E Ink™ EPD panels, supporting a wide variety of TFT backplanes. Various levels of flexibility and programmability have been introduced, as well as hardware support for different E Ink image enhancing algorithms, such as Regal D waveform support.
FLEXCAN1 FLEXCAN2	Flexible Controller Area Network	Connectivity peripherals	The CAN protocol was primarily, but not only, designed to be used as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the Electromagnetic interference (EMI) environment of a vehicle, cost-effectiveness and required bandwidth. The FlexCAN module is a full implementation of the CAN protocol specification, Version 2.0 B, which supports both standard and extended message frames.
FLEXTIMER1 FLEXTIMER2	Flexible Timer Module	Timer Peripherals	Provide input signal capture and PWM support
GPIO1 GPIO2 GPIO3 GPIO4 GPIO5 GPIO6 GPIO7	General Purpose I/O Modules	System control peripherals	Used for general purpose input/output to external ICs. Each GPIO module supports up to 32 bits of I/O.
GPMI	General Purpose Memory Interface	Connectivity peripherals	The GPMI module supports up to 8x NAND devices and 62-bit ECC encryption/decryption for NAND Flash Controller (GPMI2). GPMI supports separate DMA channels for each NAND device.

The package contact assignments can be found in Section 6, "Package information and contact assignments." Signal descriptions are provided in the *i.MX 7Dual Application Processor Reference Manual* (IMX7DRM).

Table 3. Special signal considerations

Signal Name	Remarks
CCM_CLK1_P/ CCM_CLK1_N CCM_CLK2	One general purpose differential high speed clock input/output and one single-ended clock input are provided. Either or both of them can be used: • To feed an external reference clock to the PLLs and to the modules inside the SoC, for example, as an alternate reference clock for PCIe, Video/Audio interfaces and so forth. • To output the internal SoC clock to be used outside the SoC as either a reference clock or as a functional clock for peripherals; for example, it can be used as an output of the PCIe master clock (root complex use) See the *i.MX 7Dual Application Processor Reference Manual* (IMX7DRM) for details on the respective clock trees. The CCM_CLK1_* inputs/outputs are an LVDS differential pair. Alternatively, a single-ended signal may be used to drive CCM_CLK1_P input. In this case corresponding CCM_CLK1_N input should be tied to the constant voltage level equal to 1/2 of the input signal swing. Termination should be provided in case of high frequency signals. See the LVDS pad electrical specification for further details. CCM_CLK2 is a single-ended input referenced to ground. After initialization: • The CCM_CLK1_* inputs/outputs can be disabled if not used. Any of the unused CCM_CLK1_* pins may be left floating. • The CCM_CLK2 input should be grounded if not used.
RTC_XTALI/RTC_XTALO	If the user wishes to configure RTC_XTALI and RTC_XTALO as an RTC oscillator, a 32.768 kHz crystal, (100 k ESR, 10 pF load) should be connected between RTC_XTALI and RTC_XTALO. It is recommended to use the configurable load capacitors provided in the IP instead of adding them externally. To hit the exact oscillation frequency, the configurable capacitors need to be reduced to account for board and chip parasitics. The integrated oscillation amplifier is self biasing, but relatively weak. Care must be taken to limit parasitic leakage from RTC_XTALI and RTC_XTALO to either power or ground (>100 M). This will debias the amplifier and cause a reduction of startup margin. Typically RTC_XTALI and RTC_XTALO should bias to approximately 0.5 V. If it is desired to feed an external low frequency clock into RTC_XTALI, the RTC_XTALO pin should be left floating or driven with a complimentary signal. The logic level of this forcing clock should not exceed VDD_SNVS_CAP level. In the case when a high-accuracy realtime clock is not required, the system may use internal low frequency oscillator. It is recommended to connect RTC_XTALI to ground and keep RTC_XTALO floating. This will however result in increased power consumption, because the internal oscillator uses higher power than the RTC oscillator. Thus for lowest power configuration it is recommended to always install a crystal.
XTALI/XTALO	A 24.0 MHz crystal should be connected between XTALI and XTALO.

Table 3. Special signal considerations(continued)

Signal Name	Remarks
DRAM_VREF	When using DDR_VREF with DDR I/O, the nominal reference voltage must be half of the NVCC_DRAM supply. The user must tie DDR_VREF to a precision external resistor divider. Use a 1 kΩ 0.5% resistor to GND and a 1 kΩ 0.5% resistor to NVCC_DRAM. Shunt each resistor with a closely-mounted 0.1 µF capacitor. To reduce supply current, a pair of 1.5 kΩ 0.1% resistors can be used. Using resistors with recommended tolerances ensures the ± 2% DDR_VREF tolerance (per the DDR3 specification) is maintained when four DDR3 ICs plus the i.MX 7Dual are drawing current on the resistor divider. It is recommended to use regulated power supply for “big” memory configurations (more than eight devices)
ZQPAD	DRAM calibration resistor 240 Ω 1% used as reference during DRAM output buffer driver calibration should be connected between this pad and GND.
PCIE_VPH/PCIE_VPH_TX/ PCIE_VPH_RX	Short these pins to VDDA_PHY1P8 if using PCIe. User can tie these pins to ground if not using PCIe.
PCIE_VP/PCIE_VP_TX/PC IE_VP_RX	Short these pins to VDDD_1P0CAP if using PCIe. User can tie these pins to ground with a 10 KΩ resistor if not using PCIe.
VDDA_MIPI_1P8	Short these pins to VDDA_PHY_1P8 if using MIPI. User can leave these pins floating or grounded if not using MIPI.
VDD_MIPI_1P0	Short these pins to VDDD_1P0_CAP if using MIPI. User can leave these pins floating or grounded if not using MIPI.
GPANAIO	This signal is reserved for manufacturing use only. User must leave this connection floating.
JTAG_*nnnn*	The JTAG interface is summarized in Table 4. Use of external resistors is unnecessary. However, if external resistors are used, the user must ensure that the on-chip pull-up/down configuration is followed. For example, do not use an external pull down on an input that has on-chip pull-up.
	JTAG_TDO is configured with a keeper circuit such that the floating condition is eliminated if an external pull resistor is not present. An external pull resistor on JTAG_TDO is detrimental and should be avoided.
	JTAG_MOD is referenced as SJC_MOD in the *i.MX 7Dual Application Processor Reference Manual* (IMX7DRM). Both names refer to the same signal. JTAG_MOD must be externally connected to GND for normal operation. Termination to GND through an external pull-down resistor (such as 1 kΩ) is allowed. JTAG_MOD set to high configures the JTAG interface to a mode compatible with the IEEE 1149.1 standard. JTAG_MOD set to low configures the JTAG interface for common SW debug adding all the system TAPs to the chain.
NC	Do not connect. These signals are reserved and should be floated by the user.
POR_B	This cold reset negative logic input resets all modules and logic in the IC. May be used in addition to internally generated power on reset signal (logical AND, both internal and external signals are considered active low).
ONOFF	In Normal mode, may be connected to ON/OFF button (De-bouncing provided at this input). Internally this pad is pulled up. Short connection to GND in OFF mode causes internal power management state machine to change state to ON. In ON mode short connection to GND generates interrupt (intended to SW controllable power down). Long above ~5s connection to GND causes “forced” OFF.
TEST_MODE	TEST_MODE is for factory use. This signal is internally connected to an on-chip pull-down device. The user must tie this signal to GND.

The typical values shown in Table 11 are required for use with NXP BSPs to ensure precise time keeping and USB operation. For RTC_XTALI operation, two clock sources are available. If there is not an externally applied oscillator to RTC_XTALI, the internal oscillator takes over.

- On-chip 32 kHz RC oscillator—this clock source has the following characteristics:
  - Approximately 25 µA more I_{DD} than crystal oscillator
  - Approximately ±10% tolerance
  - No external component required
  - Starts up faster than 32 kHz crystal oscillator
  - Three configurations for this input:
    - External oscillator
    - External crystal coupled to RTC_XTALI and RTC_XTALO
    - Internal oscillator

External crystal oscillator with on-chip support circuit:

- At power up, RC oscillator is utilized. After crystal oscillator is stable, the clock circuit switches over to the crystal oscillator automatically.
- Higher accuracy than RC oscillator
- If no external crystal is present, then the RC oscillator is utilized

The decision of choosing a clock source should be taken based on real-time clock use and precision timeout.

4.1.5 Maximum supply currents

The Power Virus numbers shown in Table 12 represent a use case designed specifically to show the maximum current consumption possible. All cores are running at the defined maximum frequency and are limited to L1 cache accesses only to ensure no pipeline stalls. Although a valid condition, it would have a very limited practical use case, if at all, and be limited to an extremely low duty cycle unless the intention was to specifically show the worst case power consumption.

The MC3xPF3000xxxx, NXP's power management IC targeted for the i.MX 7Dual family of processors, supports the Power Virus mode operating at 1% duty cycle. Higher duty cycles are allowed, but a robust thermal design is required for the increased system power dissipation.

Table 12 represents the maximum momentary current transients on power lines, and should be used for power supply selection. Maximum currents are higher by far than the average power consumption of typical use cases. For typical power consumption information, see the application note, *i.MX 7DS Power Consumption Measurement* (AN5383).

Table 12. Maximum supply currents

Power Rail	Source	Conditions	Max Current	Unit
VDD_ARM	From PMIC	—	500	mA
VDD_SOC	From PMIC	—	1000	mA

4.1.7.2 4.1.7.2 Power-Down modes

Table 17 shows the USB interface current consumption with only the OTG block powered down.

Table 17. USB PHY current consumption with VBUS Valid Comparators disabled[1]

	VDD_USB_OTG1_3P3_IN	VDD_USB_OTG2_3P3_IN
Current	730 uA	730 uA

1 VBUS Valid comparators can be disabled through software by setting USBNC_OTG*_PHY_CFG2[OTGDISABLE0] to 1. This signal powers down only the VBUS Valid comparator, and does not control power to the Session Valid Comparator, ADP Probe and Sense comparators, or the ID detection circuitry.

In Power-Down mode, everything is powered down, including the USB_VBUS valid comparators and their associated bandgap circuity in typical condition. Table 18 shows the USB interface current consumption in Power-Down mode.

Table 18. USB PHY current consumption in Power-Down mode[1]

	VDD_USB_OTG1_3P3_IN	VDD_USB_OTG2_3P3_IN
Current	200 uA	200 uA

1 The VBUS Valid Comparators and their associated bandgap circuits can be disabled through software by setting USBNC_OTG*_PHY_CFG2[OTGDISABLE0] to 1 and USBNC_OTG*_PHY_CFG2[DRVVBUS0] to 0, respectively.

4.1.8 PCIe phy 2.1 DC electrical characteristics

Table 19. PCIe recommended operating conditions

Parameter	Description		Min	Max	Unit
V_{DD}	Low Power Supply Voltage for PHY Core	1 V	0.95	1.05	V
	High Power Supply Voltage for PHY Core	1.8 V	1.71	1.89	
T_A	Commercial Temperature Range		0	70	°C
T_J	Simulation Junction Temperature Range		-40	125	°C

Note: V_{DD} should have no more than 40 mVpp AC power supply noise superimposed on the high power supply voltage for the PHY core (1.8 V nominal DC value). At the same time, VDD should have no more than 20 mVpp AC power supply noise superimposed on the low power supply voltage for the PHY core.
The power supply voltage variation for the PHY core should have less than +/-5% including the board-level power supply variation and on-chip power supply variation due to the finite impedances in the package.

Table 21. PCIe PHY high-speed characteristics(continued)

High Speed I/O Characteristics						
Description	**Symbol**	**Speed**	**Min.**	**Typ.**	**Max.**	**Unit**
PCIe Tx deterministic jitter < 1.5 MHz	TRJ	2.5 Gbps/ 5.0 Gbps	—	—	3 ps	ps, rms
PCIe Tx deterministic jitter > 1.5 MHz	TDJ	5.0 Gbps/ 2.5 Gbps	—	—	30 ps/ 60 ps	ps, pk–pk
RX Serial data input voltage (Differential pk–pk)	ΔV_{RX}	1.5 Gbps	325	—	600	mVp–p
		2.5 Gbps	120	—	1200	
		3.0 Gbps	275	—	750	
		5.0 Gbps	120	—	1200	
		6.0 Gbps	240	—	1000	

Table 22. PCIe PHY reference clock timing requirements

Description	Symbol	Min.	Typ.	Max.	Unit
Frequency Tolerance	F_{TOL}	–100	—	100	ppm
Duty Cycle	D_C	40	—	60	%
Rise and Fall Time	T_R,T_F	—	—	1.5	ns
Peak to peak Jitter	Jitter	—	—	40	ps,pk–pk
RMS Jitter		—	—	2.5	ps,rms
Period Jitter		—	—	25	ps
External Clock source output impedence	$Z_{C,DC}$	40	—	60	Ω
Differential input high voltage	V_{IH}	150	—		mV
Differential input low voltage	V_{IL}	—	—	-150	mV
Absolute maximum input voltage	V_{MAX}	33	—	1.15	V
Absolute minimum input voltage	V_{MIN}	400	—	-0.3	V
Absolute crossing point voltage	V_{CROSS}	250	—	1550	mV

Table 35. Maximum input cell delay time

Cell name	Max Delay PAD → Y (ns)		
	VDD=1.65 V T=125°C Process=Slow	VDD=2.3 V T=125°C Process=Slow	VDD=3.0 V T=125°C Process=Slow
PBIDIRPUD_E33_33_NT_DR	0.9	1.5	1.4

Table 36. Output cell delay time for fixed load

Parameter				Simulated Cell Delay A → PAD (ns)								
				VDD = 1.65 V, T = 125°C			VDD = 2.3 V, T = 125°C			VDD = 3.0 V, T = 125°C		
DS0	DS1	SR	Driver Type	CL= 5 pF	CL= 10 pF	CL= 40 pF	CL= 5 pF	CL= 10 pF	CL= 40 pF	CL= 5 pF	CL= 10 pF	CL= 40 pF
0	0	1	1× Slow Slew	4.9	6.0	12.5	4.8	6.1	11.9	5.4	6.7	14.6
0	0	0	1× Fast Slew	3.8	4.7	11.2	3.8	5.1	12.8	4.2	5.3	13.5
0	1	1	2× Slow Slew	4.1	4.8	8.2	4.2	4.9	8.8	4.5	5.3	9.1
0	1	0	2× Fast Slew	2.8	3.3	6.4	2.9	3.4	7.2	3.1	3.7	7.2
1	0	1	4× Slow Slew	3.6	4.1	6.0	3.7	4.1	6.4	3.9	4.4	6.6
1	0	0	4× Fast Slew	2.2	2.5	4.1	2.3	2.6	4.6	2.4	2.8	4.8
1	1	1	6× Slow Slew	3.6	4.0	5.5	3.6	4.0	5.9	3.8	4.3	6.2
1	1	0	6× Fast Slew	2.0	2.3	3.4	2.1	2.3	3.8	2.2	2.5	3.9

Table 37. Maximum frequency of operation for input

Maximum frequency (MHz)		
VDD = 1.8 V, CL = 50 fF	VDD=2.5 V, CL =5 0 fF	VDD = 3.3 V, CL = 50 fF
550	400	430

4.8.4.3 LPDDR2 parameters

Figure 30 shows the LPDDR2 basic timing diagram. The timing parameters for this diagram appear in Table 53.

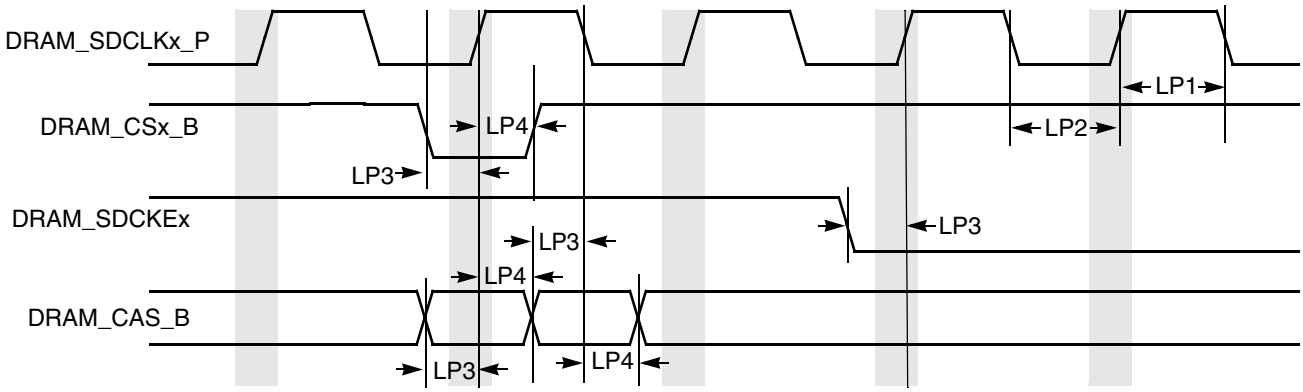

Figure 30. LPDDR2 command and address timing diagram

Table 53. LPDDR2 timing parameters[1,2]

ID	Parameter	Symbol	CK = 533 MHz		Unit
			Min	Max	
LP1	SDRAM clock high-level width	t_{CH}	0.45	0.55	t_{CK}
LP2	SDRAM clock low-level width	t_{CL}	0.45	0.55	t_{CK}
LP3	DRAM_CSx_B, DRAM_SDCKEx setup time	t_{IS}	370	—	ps
LP4	DRAM_CSx_B, DRAM_SDCKEx hold time	t_{IH}	370	—	ps
LP3	DRAM_CAS_B setup time	t_{IS}	770	—	ps
LP4	DRAM_CAS_B hold time	t_{IH}	770	—	ps

1 All measurements are in reference to Vref level.

2 Measurements were done using balanced load and 25 Ω resistor from outputs to DDR_VREF

In EDO mode (Figure 36), NF16/NF17 are different from the definition in non-EDO mode (Figure 35). They are called tREA/tRHOH (RE# access time/RE# HIGH to output hold). The typical value for them are 16 ns (max for tREA)/15 ns (min for tRHOH) at 50 MB/s EDO mode. In EDO mode, GPMI will sample NAND_DATAxx at rising edge of delayed NAND_RE_B provided by an internal DPLL. The delay value can be controlled by GPMI_CTRL1.RDN_DELAY (see the GPMI chapter of the *i.MX 7Dual Application Processor Reference Manual* [IMX7DRM]). The typical value of this control register is 0x8 at 50 MT/s EDO mode. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

4.9.2 Source Synchronous mode AC timing (ONFI 2.x compatible)

Figure 38 to Figure 40 show the write and read timing of Source Synchronous mode.

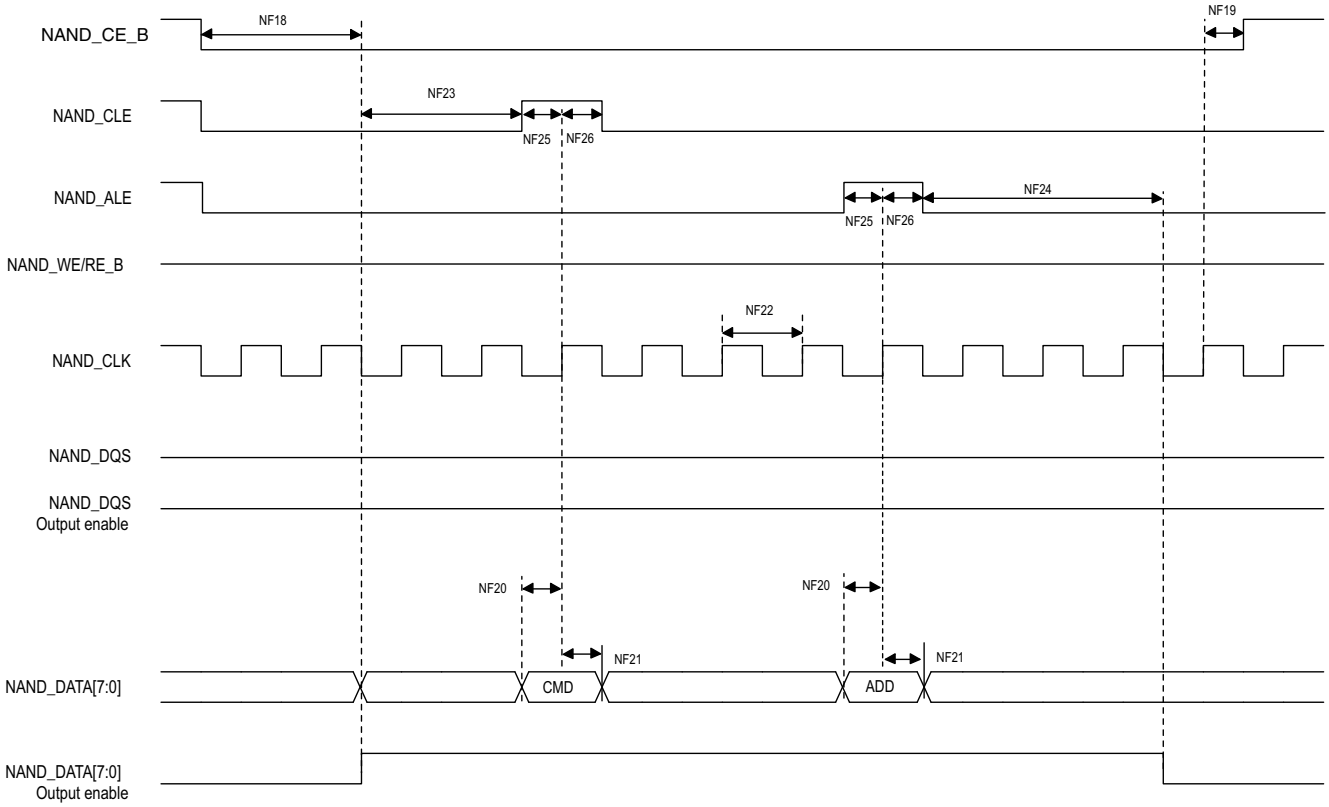

Figure 38. Source Synchronous mode command and address timing diagram

Table 62. eMMC4.4/4.41 interface timing specification(continued)

ID	Parameter	Symbols	Min	Max	Unit
SD3	uSDHC Input Setup Time	t_{ISU}	2.4	—	ns
SD4	uSDHC Input Hold Time	t_{IH}	1.3	—	ns

4.10.2.3 HS400 AC timing—eMMC5.0 only

Figure 48 depicts the timing of HS400. Table 63 lists the HS400 timing characteristics. Be aware that only data is sampled on both edges of the clock (not applicable to CMD). The CMD input/output timing for HS400 mode is the same as CMD input/output timing for SDR104 mode. Check SD5, SD6 and SD7 parameters in Table 65 SDR50/SDR104 Interface Timing Specification for CMD input/output timing for HS400 mode.

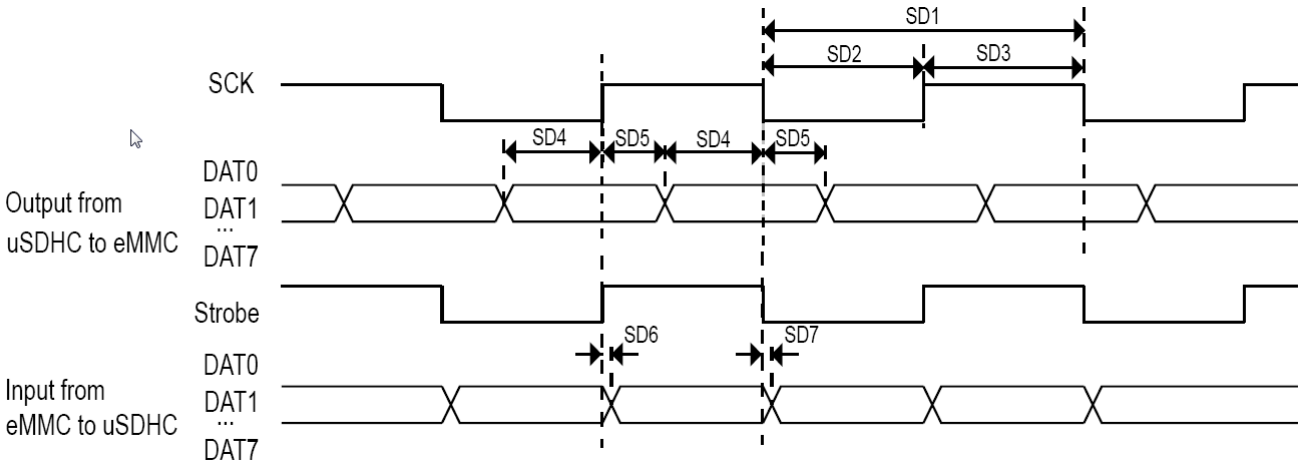

Figure 48. HS400 timing

Table 63. HS400 interface timing specifications

ID	Parameter	Symbols	Min	Max	Unit
Card Input clock					
SD1	Clock Frequency	fPP	0	200	Mhz
SD2	Clock Low Time	t_{CL}	$0.46 \times t_{CLK}$	$0.54 \times t_{CLK}$	ns
SD3	Clock High Time	t_{CH}	$0.46 \times t_{CLK}$	$0.54 \times t_{CLK}$	ns
uSDHC Output/Card inputs DAT (Reference to SCK)					
SD4	Output Skew from Data of Edge of SCK	t_{OSkew1}	0.45	—	ns
SD5	Output Skew from Edge of SCK to Data	t_{OSkew2}	0.45	—	ns

4.10.2.5 SDR50/SDR104 AC timing

Figure 50 depicts the timing of SDR50/SDR104, and Table 65 lists the SDR50/SDR104 timing characteristics.

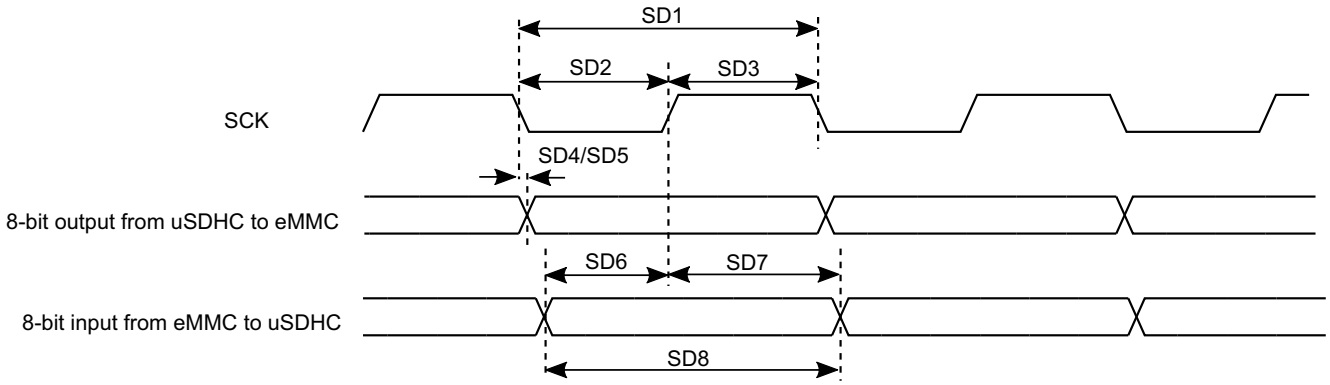

Figure 50. SDR50/SDR104 timing

Table 65. SDR50/SDR104 interface timing specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency Period	t_{CLK}	5	—	ns
SD2	Clock Low Time	t_{CL}	$0.46 \times t_{CLK}$	$0.54 \times t_{CLK}$	ns
SD3	Clock High Time	t_{CH}	$0.46 \times t_{CLK}$	$0.54 \times t_{CLK}$	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR50 (Reference to CLK)					
SD4	uSDHC Output Delay	t_{OD}	–3	1	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR104 (Reference to CLK)					
SD5	uSDHC Output Delay	t_{OD}	–1.6	1	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR50 (Reference to CLK)					
SD6	uSDHC Input Setup Time	t_{ISU}	2.4	—	ns
SD7	uSDHC Input Hold Time	t_{IH}	1.4	—	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR104 (Reference to CLK)[1]					
SD8	Card Output Data Window	t_{ODW}	$0.5*t_{CLK}$	—	ns

[1]Data window in SDR100 mode is variable.

Table 69. MII serial management channel timing

ID	Characteristic	Min.	Max.	Unit
M10	ENET_MDC falling edge to ENET_MDIO output invalid (min. propagation delay)	0	—	ns
M11	ENET_MDC falling edge to ENET_MDIO output valid (max. propagation delay)	—	5	ns
M12	ENET_MDIO (input) to ENET_MDC rising edge setup	18	—	ns
M13	ENET_MDIO (input) to ENET_MDC rising edge hold	0	—	ns
M14	ENET_MDC pulse width high	40%	60%	ENET_MDC period
M15	ENET_MDC pulse width low	40%	60%	ENET_MDC period

4.10.3.2 RMII mode timing

In RMII mode, ENET_CLK is used as the REF_CLK, which is a 50 MHz ± 50 ppm continuous reference clock. ENET_RX_EN is used as the ENET_RX_EN in RMII. Other signals under RMII mode include ENET_TX_EN, ENET_TX_DATA[1:0], ENET_RX_DATA[1:0] and ENET_RX_ER.

Figure 55 shows RMII mode timings. Table 70 describes the timing parameters (M16–M21) shown in the figure.

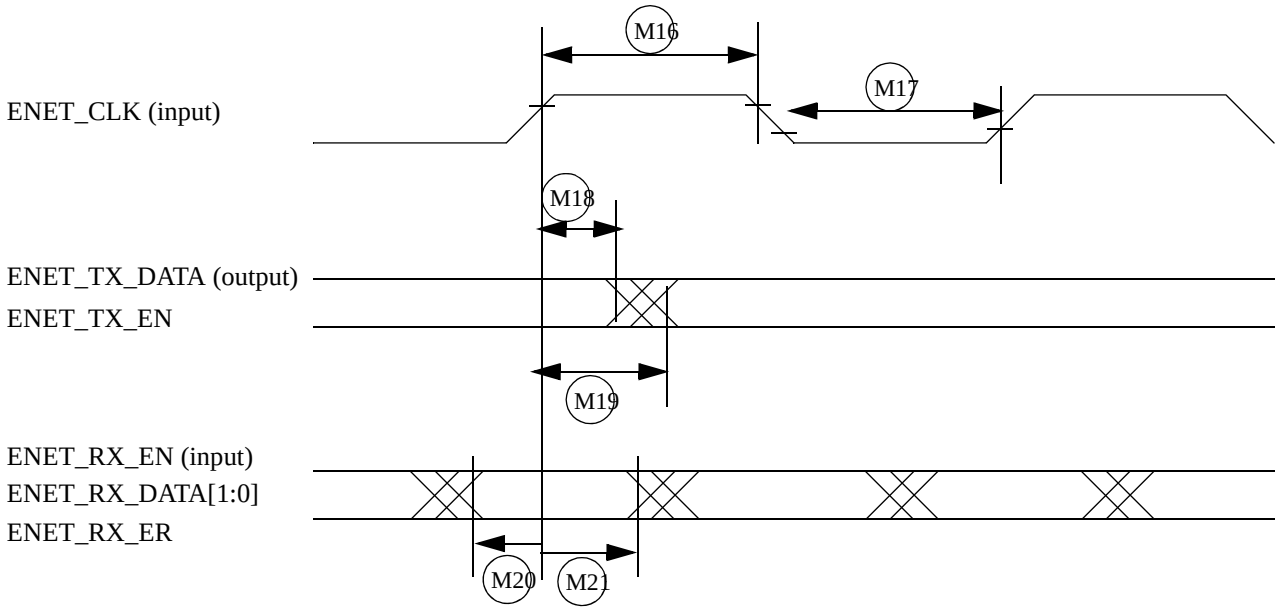

Figure 55. RMII mode signal timing diagram

4.10.8.6 High-speed clock timing

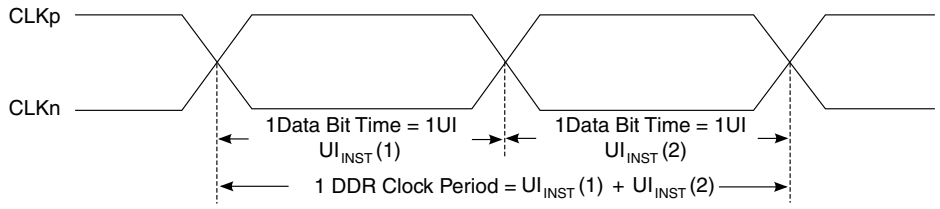

Figure 67. DDR Clock Definition

4.10.8.7 Forward high-speed data transmission timing

The timing relationship of the DDR Clock differential signal to the Data differential signal is shown in Figure 68:

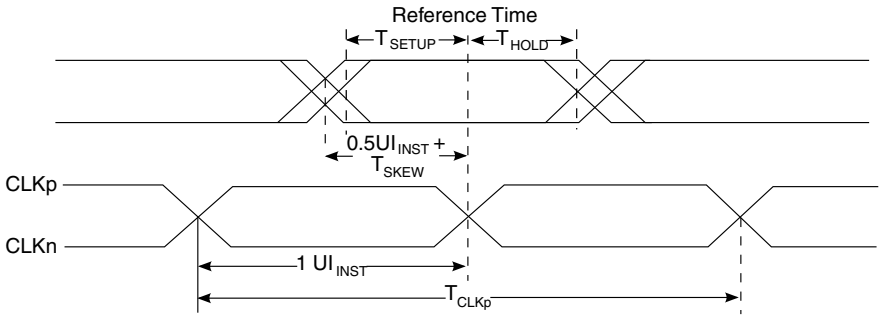

Figure 68. Data to Clock Timing Definitions

4.10.8.8 Reverse high-speed data transmission timing

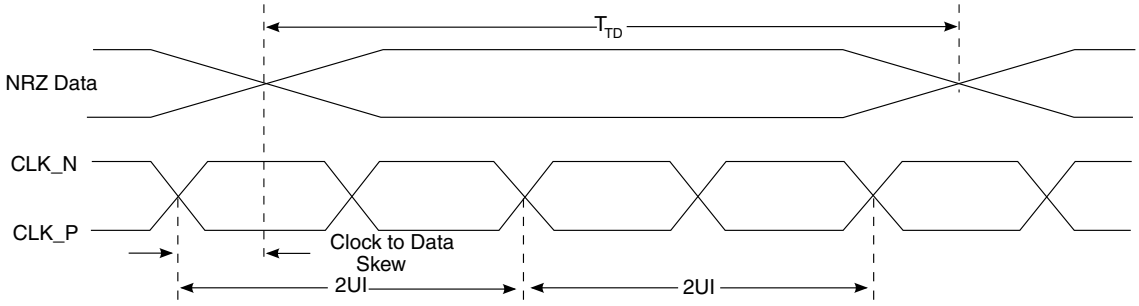

Figure 69. Reverse High-Speed Data Transmission Timing at Slave Side

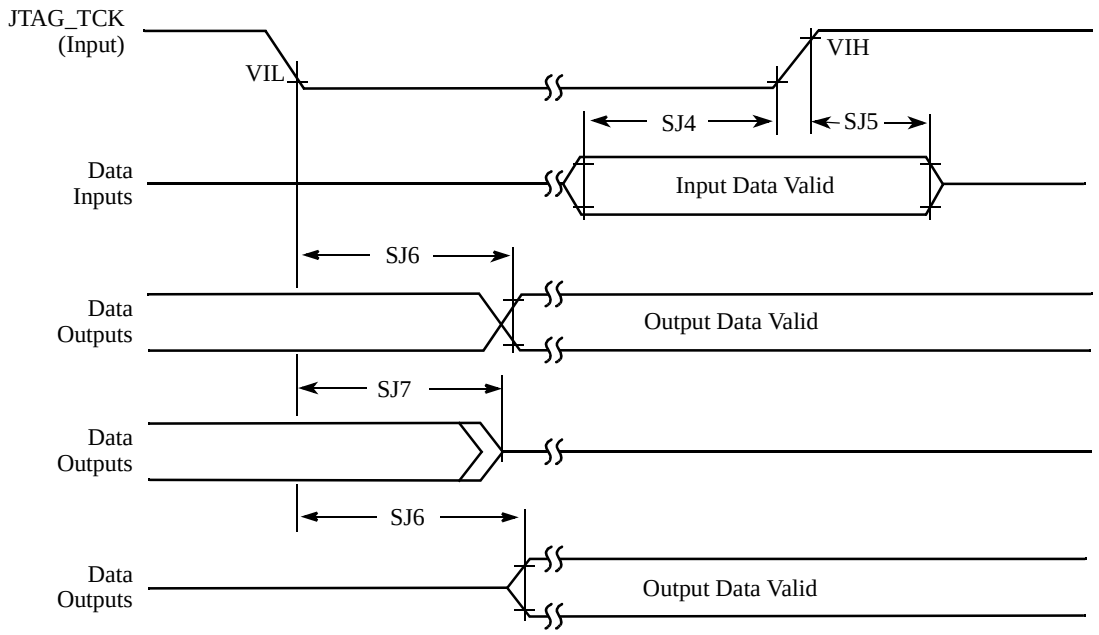

Figure 80. Boundary scan (JTAG) timing diagram

Table 98. i.MX 7Dual 12 x 12 mm supplies contact assignments(continued)

Rail	Ball	Comments
NVCC_UART	T09	Supply for UART
PCIE_VP	AB13	Supply input for the PCIe PHY
PCIE_VPH	Y15	Supply input for the PCIe PHY
PVCC_ENET_CAP	G16	Secondary supply for ENET. Requires external capacitor
PVCC_EPDC_LCD_CAP	R20	Secondary supply for EPDC, LCD. Requires external capacitor
PVCC_GPIO_CAP	AB11	Secondary supply for GPIO. Requires external capacitor
PVCC_I2C_SPI_UART_CAP	W08	Secondary supply for I2C, SPI, UART. Requires external capacitor
PVCC_SAI_SD_CAP	J14	Secondary supply for SAI, SD. Requires external capacitor
USB_OTG1_VBUS	C09	VBUS input for USB_OTG1
USB_OTG2_VBUS	C11	VBUS input for USB_OTG2
VDD_1P2_CAP	AA10	Supply for HSIC
VDD_ARM	A20,B20,C16,C17,C18,C19,C20,C21,C22,F19,H19,J20,K21,K23,K26,L27,L28	Supply voltage for ARM
VDD_LPSR_1P0_CAP	AG06	Secondary supply for LPSR. Requires external capacitor
VDD_LPSR_IN	AG05	Supply to LPSR
VDD_MIPI_1P0	J16	Supply for MIPI
VDD_SNVS_1P8_CAP	AG07	Secondary supply for SNVS. Requires external capacitor
VDD_SNVS_IN	Y13	Supply for SNVS
VDD_SOC	H10,J09,K03,K06,K08,L01,L02,L11,L18,N13,N16,P03,P06,P23,P26,R26,T13,T16,V11,V18,R03,R06,R23	Supply for SOC
VDD_TEMPSENSOR_1P8	AH05	Supply for temp sensor
VDD_USB_H_1P2	C12,G13	Supply input for the USB HSIC interface
VDD_USB_OTG1_1P0_CAP	E09	Secondary supply for OTG1. Requires external capacitor
VDD_USB_OTG1_3P3_IN	D09	Secondary supply for OTG1. Requires external capacitor
VDD_USB_OTG2_1P0_CAP	F09	Secondary supply for OTG2. Requires external capacitor
VDD_USB_OTG2_3P3_IN	D11	Secondary supply for OTG2. Requires external capacitor

Table 99. i.MX 7Dual 12 x 12 mm functional contact assignments(continued)

Ball	Ball Name	Power Group	Ball type[1]	Default Mode[1]	Default Function[1]	PD/PU
AB28	DRAM_DATA23	NVCC_DRAM	DDR		DRAM_DATA23	
V23	DRAM_DATA24	NVCC_DRAM	DDR		DRAM_DATA24	
V22	DRAM_DATA25	NVCC_DRAM	DDR		DRAM_DATA25	
T23	DRAM_DATA26	NVCC_DRAM	DDR		DRAM_DATA26	
T22	DRAM_DATA27	NVCC_DRAM	DDR		DRAM_DATA27	
V24	DRAM_DATA28	NVCC_DRAM	DDR		DRAM_DATA28	
V25	DRAM_DATA29	NVCC_DRAM	DDR		DRAM_DATA29	
T25	DRAM_DATA30	NVCC_DRAM	DDR		DRAM_DATA30	
T24	DRAM_DATA31	NVCC_DRAM	DDR		DRAM_DATA31	
AH24	DRAM_DQM0	NVCC_DRAM	DDR		DRAM_DQM0	
AD20	DRAM_DQM1	NVCC_DRAM	DDR		DRAM_DQM1	
AD28	DRAM_DQM2	NVCC_DRAM	DDR		DRAM_DQM2	
Y25	DRAM_DQM3	NVCC_DRAM	DDR		DRAM_DQM3	
AF16	DRAM_ODT0	NVCC_DRAM	DDR		DRAM_ODT0	
AH25	DRAM_RAS_B	NVCC_DRAM	DDR		DRAM_RAS_B	
V26	DRAM_RESET	NVCC_DRAM_CKE	DDR		DRAM_RESET	
AE28	DRAM_SDBA0	NVCC_DRAM	DDR		DRAM_SDBA0	
AB22	DRAM_SDBA1	NVCC_DRAM	DDR		DRAM_SDBA1	
AF27	DRAM_SDBA2	NVCC_DRAM	DDR		DRAM_SDBA2	
Y22	DRAM_SDCKE0	NVCC_DRAM_CKE	DDR		DRAM_SDCKE0	
AB23	DRAM_SDCKE1	NVCC_DRAM_CKE	DDR		DRAM_SDCKE1	
AF25	DRAM_SDCLK0_N	NVCC_DRAM	DDRCLK		DRAM_SDCLK0_N	
AE25	DRAM_SDCLK0_P	NVCC_DRAM	DDRCLK		DRAM_SDCLK0_P	
AG23	DRAM_SDQS0_N	NVCC_DRAM	DDRCLK		DRAM_SDQS0_N	
AG24	DRAM_SDQS0_P	NVCC_DRAM	DDRCLK		DRAM_SDQS0_P	
AC20	DRAM_SDQS1_N	NVCC_DRAM	DDRCLK		DRAM_SDQS1_N	
AB20	DRAM_SDQS1_P	NVCC_DRAM	DDRCLK		DRAM_SDQS1_P	
AD27	DRAM_SDQS2_N	NVCC_DRAM	DDRCLK		DRAM_SDQS2_N	
AC27	DRAM_SDQS2_P	NVCC_DRAM	DDRCLK		DRAM_SDQS2_P	
Y24	DRAM_SDQS3_N	NVCC_DRAM	DDRCLK		DRAM_SDQS3_N	
Y23	DRAM_SDQS3_P	NVCC_DRAM	DDRCLK		DRAM_SDQS3_P	
AH27	DRAM_SDWE_B	NVCC_DRAM	DDR		DRAM_SDWE_B	

Table 99. i.MX 7Dual 12 x 12 mm functional contact assignments(continued)

Ball	Ball Name	Power Group	Ball type[1]	Default Mode[1]	Default Function[1]	PD/PU
M03	ECSPI1_MISO	NVCC_SPI	GPIO	ALT5	GPIO4_IO[18]	100K PD
L03	ECSPI1_MOSI	NVCC_SPI	GPIO	ALT5	GPIO4_IO[17]	100K PD
K02	ECSPI1_SCLK	NVCC_SPI	GPIO	ALT5	GPIO4_IO[16]	100K PD
N03	ECSPI1_SS0	NVCC_SPI	GPIO	ALT5	GPIO4_IO[19]	100K PD
P02	ECSPI2_MISO	NVCC_SPI	GPIO	ALT5	GPIO4_IO[22]	100K PD
N02	ECSPI2_MOSI	NVCC_SPI	GPIO	ALT5	GPIO4_IO[21]	100K PD
N01	ECSPI2_SCLK	NVCC_SPI	GPIO	ALT5	GPIO4_IO[20]	100K PD
R02	ECSPI2_SS0	NVCC_SPI	GPIO	ALT5	GPIO4_IO[23]	100K PD
G18	ENET1_COL	NVCC_ENET1	GPIO	ALT5	GPIO7_IO[15]	100K PD
F18	ENET1_CRS	NVCC_ENET1	GPIO	ALT5	GPIO7_IO[14]	100K PD
F07	ENET1_RD0	NVCC_ENET1	GPIO	ALT5	GPIO7_IO[0]	100K PD
E07	ENET1_RD1	NVCC_ENET1	GPIO	ALT5	GPIO7_IO[1]	100K PD
D07	ENET1_RD2	NVCC_ENET1	GPIO	ALT5	GPIO_IO[2]	100K PD
D16	ENET1_RD3	NVCC_ENET1	GPIO	ALT5	GPIO7_IO[3]	100K PD
C06	ENET1_RX_CLK	NVCC_ENET1	GPIO	ALT5	GPIO7_IO[13]	100K PD
E11	ENET1_RX_CTL	NVCC_ENET1	GPIO	ALT5	GPIO7_IO[4]	100K PD
F11	ENET1_RXC	NVCC_ENET1	GPIO	ALT5	GPIO7_IO[5]	100K PD
E13	ENET1_TD0	NVCC_ENET1	GPIO	ALT5	GPIO7_IO[6]	100K PD
D13	ENET1_TD1	NVCC_ENET1	GPIO	ALT5	GPIO_IO[7]	100K PD
E16	ENET1_TD2	NVCC_ENET1	GPIO	ALT5	GPIO7_IO[8]	100K PD
F16	ENET1_TD3	NVCC_ENET1	GPIO	ALT5	GPIO7_IO[9]	100K PD
F13	ENET1_TX_CLK	NVCC_ENET1	GPIO	ALT5	GPIO7_IO[12]	100K PD
G11	ENET1_TX_CTL	NVCC_ENET1	GPIO	ALT5	GPIO7_IO[10]	100K PD
G09	ENET1_TXC	NVCC_ENET1	GPIO	ALT5	GPIO7_IO[11]	100K PD
L23	EPDC_BDR0	NVCC_EPDC2	GPIO	ALT5	GPIO2_IO[28]	100K PD
L22	EPDC_BDR1	NVCC_EPDC2	GPIO	ALT5	GPIO2_IO[29]	100K PD
T27	EPDC_D00	NVCC_EPDC1	GPIO	ALT5	GPIO2_IO[0]	100K PD
U26	EPDC_D01	NVCC_EPDC1	GPIO	ALT5	GPIO2_IO[1]	100K PD
T26	EPDC_D02	NVCC_EPDC1	GPIO	ALT5	GPIO2_IO[2]	100K PD
R27	EPDC_D03	NVCC_EPDC1	GPIO	ALT5	GPIO2_IO[3]	100K PD
N23	EPDC_D04	NVCC_EPDC1	GPIO	ALT5	GPIO2_IO[4]	100K PD
T28	EPDC_D05	NVCC_EPDC1	GPIO	ALT5	GPIO2_IO[5]	100K PD

Table 102. i.MX 7Dual 19 x 19 mm functional contact assignments(continued)

Ball	Ball Name	Power Group	Ball type[1]	Default Mode[1]	Default Function[1]	PD/PU
E12	SAI1_RXD	NVCC_SAI	GPIO	ALT5	GPIO6_IO[12]	100K PD
C12	SAI1_RXFS	NVCC_SAI	GPIO	ALT5	GPIO6_IO[16]	100K PD
C11	SAI1_TXC	NVCC_SAI	GPIO	ALT5	GPIO6_IO[13]	100K PD
E11	SAI1_TXD	NVCC_SAI	GPIO	ALT5	GPIO6_IO[15]	100K PD
D11	SAI1_TXFS	NVCC_SAI	GPIO	ALT5	GPIO6_IO[14]	100K PD
E09	SAI2_RXD	NVCC_SAI	GPIO	ALT5	GPIO6_IO[21]	100K PD
D08	SAI2_TXC	NVCC_SAI	GPIO	ALT5	GPIO6_IO[20]	100K PD
E08	SAI2_TXD	NVCC_SAI	GPIO	ALT5	GPIO6_IO[22]	100K PD
D09	SAI2_TXFS	NVCC_SAI	GPIO	ALT5	GPIO6_IO[19]	100K PD
C06	SD1_CD_B	NVCC_SD1	GPIO	ALT5	GPIO5_IO[0]	100K PD
B05	SD1_CLK	NVCC_SD1	GPIO	ALT5	GPIO5_IO[3]	100K PD
C05	SD1_CMD	NVCC_SD1	GPIO	ALT5	GPIO5_IO[4]	100K PD
A05	SD1_DATA0	NVCC_SD1	GPIO	ALT5	GPIO5_IO[5]	100K PD
D06	SD1_DATA1	NVCC_SD1	GPIO	ALT5	GPIO5_IO[6]	100K PD
A04	SD1_DATA2	NVCC_SD1	GPIO	ALT5	GPIO5_IO[7]	100K PD
D05	SD1_DATA3	NVCC_SD1	GPIO	ALT5	GPIO5_IO[8]	100K PD
B04	SD1_RESET_B	NVCC_SD1	GPIO	ALT5	GPIO5_IO[2]	100K PD
C04	SD1_WP	NVCC_SD1	GPIO	ALT5	GPIO5_IO[1]	100K PD
D03	SD2_CD_B	NVCC_SD2	GPIO	ALT5	GPIO5_IO[9]	100K PD
E03	SD2_CLK	NVCC_SD2	GPIO	ALT5	GPIO5_IO[12]	100K PD
F06	SD2_CMD	NVCC_SD2	GPIO	ALT5	GPIO5_IO[13]	100K PD
E04	SD2_DATA0	NVCC_SD2	GPIO	ALT5	GPIO5_IO[14]	100K PD
E05	SD2_DATA1	NVCC_SD2	GPIO	ALT5	GPIO5_IO[15]	100K PD
F05	SD2_DATA2	NVCC_SD2	GPIO	ALT5	GPIO5_IO[16]	100K PD
E06	SD2_DATA3	NVCC_SD2	GPIO	ALT5	GPIO5_IO[17]	100K PD
G03	SD2_RESET_B	NVCC_SD2	GPIO	ALT5	GPIO5_IO[11]	100K PD
C03	SD2_WP	NVCC_SD2	GPIO	ALT5	GPIO5_IO[10]	100K PD
C01	SD3_CLK	NVCC_SD3	GPIO	ALT5	GPIO6_IO[0]	100K PD
E01	SD3_CMD	NVCC_SD3	GPIO	ALT5	GPIO6_IO[1]	100K PD
B02	SD3_DATA0	NVCC_SD3	GPIO	ALT5	GPIO6_IO[2]	100K PD
A02	SD3_DATA1	NVCC_SD3	GPIO	ALT5	GPIO6_IO[3]	100K PD
G02	SD3_DATA2	NVCC_SD3	GPIO	ALT5	GPIO6_IO[4]	100K PD

Table 103. i.MX 7Dual 19 × 19 mm 0.75 mm pitch ball map (continued)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	
L	I2C4_SCL	I2C4_SDA	UART1_RXD	UART1_TXD	UART2_RXD	UART2_TXD	VSS		NVCC_SPI		VSS		VSS		VSS		NVCC_EPDC2		VSS	EPDC1_DATA14	EPDC1_DATA13	EPDC1_DATA12	EPDC1_DATA11	EPDC1_DATA10	EPDC1_DATA09	**L**
M	UART3_RXD	UART3_TXD	VDD_SOC	VDD_SOC	UART3_RTS	UART3_CTS		NVCC_I2C		VSS		VSS		VSS		VSS		NVCC_EPDC1		EPDC1_DATA05	EPDC1_DATA06	EPDC1_DATA07	EPDC1_DATA08	VSS	VSS	**M**
N	GPIO1_IO00	GPIO1_IO01	GPIO1_IO02	VSS	GPIO1_IO03	GPIO1_IO04	VSS		NVCC_UART		VSS		VSS		VSS		PVCC_EPDC_LCD_CAP		VSS	EPDC1_DATA02	EPDC1_DATA03	EPDC1_DATA04	DRAM_SDBA2	DRAM_DATA25	DRAM_DATA27	**N**
P	GPIO1_IO05	GPIO1_IO06	GPIO1_IO07	BOOT_MODE0	BOOT_MODE1	TEST_MODE		NVCC_GPIO1		VSS		VSS		VSS		VSS		VDD_SOC		EPDC_D00	EPDC1_DATA01	DRAM_SDBA1	DRAM_ADDR13	DRAM_DQM3	DRAM_DATA26	**P**
R	GPIO1_IO08	GPIO1_IO09	VDD_SOC	VDD_SOC	GPIO1_IO10	POR_B	VSS		PVCC_I2C_SPI_UART_CAP		VSS		VSS		VSS		VDD_SOC		VSS	VSS	VSS	DRAM_SDBA0	VSS	DRAM_DATA29	DRAM_DATA24	**R**
T	GPIO1_IO11	GPIO1_IO12	GPIO1_IO13	VSS	GPIO1_IO14	GPIO1_IO15		NVCC_GPIO2		VSS		VSS		VSS		VSS		VDD_SOC		VSS	NVCC_DRAM	DRAM_ADDR12	DRAM_ADDR10	DRAM_SDQS3_P	DRAM_SDQS3_N	**T**
U	JTAG_MOD	JTAG_TRST_B	JTAG_TDI	JTAG_TMS	JTAG_TCK	JTAG_TDO	VSS		VDD_1P2_CAP		VSS		VDD_SOC		VDD_SOC		VDD_SOC		VSS	VSS	NVCC_DRAM	DRAM_ADDR11	VSS	DRAM_DATA30	DRAM_DATA28	**U**
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	