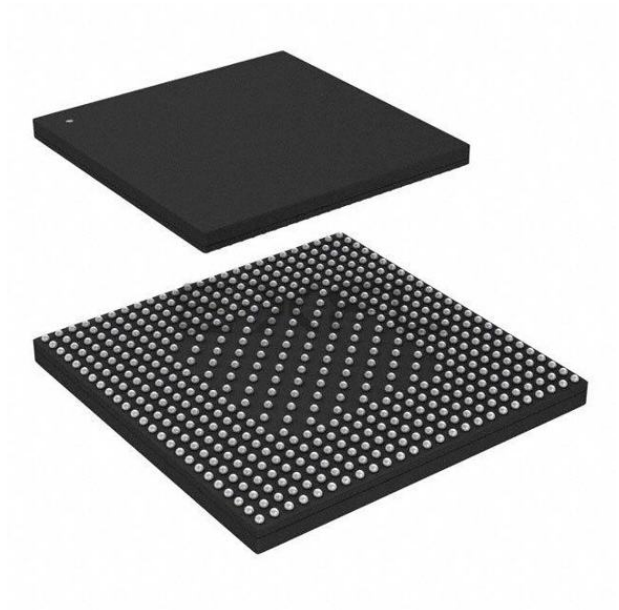

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A7, ARM® Cortex®-M4
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR2, LPDDR3, DDR3, DDR3L
Graphics Acceleration	No
Display & Interface Controllers	Keypad, LCD, MIPI
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (1), USB 2.0 OTG + PHY (2)
Voltage - I/O	1.8V, 3.3V
Operating Temperature	0°C ~ 95°C (TJ)
Security Features	A-HAB, ARM TZ, CAAM, CSU, SJC, SNVS
Package / Case	541-LFBGA
Supplier Device Package	541-MAPBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx7d7dvm10sc

- Advanced security—The processors deliver hardware-enabled security features that enable secure e-commerce, digital rights management (DRM), information encryption, secure boot, and secure software downloads. The security features are discussed in detail in the i.MX 7Dual security reference manual.
- Integrated power management—The processors integrate linear regulators and internally generate voltage levels for different power domains. This significantly simplifies system power management structure.

For a comprehensive list of the i.MX 7Dual features, see Section 1.2, "Features."

1.1 Ordering information

Table 1 provides examples of orderable sample part numbers covered by this data sheet.

Table 1. Orderable parts

Part Number	Options	Cortex-A7 CPU Speed Grade	Qualification Tier	Temperature (T_j)	Package
MCIMX7D7DVK10SD	EPDC, CAN 2 x Gigabit Ethernet 4 tamper pins 1 x ADC	1 GHz	Consumer[1]	0 to +95°C	12x12 mm 0.4 mm pitch BGA
MCIMX7D7DVM10SD	EPDC, CAN 2 x Gigabit Ethernet 10 tamper pins 2 x ADC	1 GHz	Consumer[1]	0 to +95°C	19x19 mm 0.75 mm pitch BGA
MCIMX7D5EVM10SD	No EPDC, CAN 2 x Gigabit Ethernet 10 tamper pins 2 x ADC	1 GHz	Industrial[2]	-20 to 105°C	19x19 mm 0.75 mm pitch BGA
MCIMX7D3DVK10SD	No EPDC, No CAN 2 x Gigabit Ethernet 4 tamper pins 1 x ADC	1 GHz	Consumer[1]	0 to +95°C	12x12 mm 0.4 mm pitch BGA
MCIMX7D3EVK10SD	No EPDC, No CAN 2 x Gigabit Ethernet 4 tamper pins 1 x ADC	1 GHz	Industrial[2]	–20 to +105°C	12x12 mm 0.4 mm pitch BGA
MCIMX7D2DVK12SD	No EPDC, No CAN 2 x Gigabit Ethernet 4 tamper pins 1x ADC	1.2 GHz	Consumer	0 to 85°C	12x12 mm 0.4 mm pitch BGA
MCIMX7D2DVM12SD	No EPDC, No CAN 2x Gigabit Ethernet 10 tamper pins 2x ADC	1.2 GHz	Consumer	0 to 85°C	19x19mm 0.75 mm pitch BGA

1 Consumer qualification grade assumes 5-year lifetime with 50% duty cycle.

2 Industrial qualification grade assumes 10-year lifetime with 100% duty cycle.

The typical values shown in Table 11 are required for use with NXP BSPs to ensure precise time keeping and USB operation. For RTC_XTALI operation, two clock sources are available. If there is not an externally applied oscillator to RTC_XTALI, the internal oscillator takes over.

- On-chip 32 kHz RC oscillator—this clock source has the following characteristics:
  - Approximately 25 µA more I_{DD} than crystal oscillator
  - Approximately ±10% tolerance
  - No external component required
  - Starts up faster than 32 kHz crystal oscillator
  - Three configurations for this input:
    - External oscillator
    - External crystal coupled to RTC_XTALI and RTC_XTALO
    - Internal oscillator

External crystal oscillator with on-chip support circuit:

- At power up, RC oscillator is utilized. After crystal oscillator is stable, the clock circuit switches over to the crystal oscillator automatically.
- Higher accuracy than RC oscillator
- If no external crystal is present, then the RC oscillator is utilized

The decision of choosing a clock source should be taken based on real-time clock use and precision timeout.

4.1.5 Maximum supply currents

The Power Virus numbers shown in Table 12 represent a use case designed specifically to show the maximum current consumption possible. All cores are running at the defined maximum frequency and are limited to L1 cache accesses only to ensure no pipeline stalls. Although a valid condition, it would have a very limited practical use case, if at all, and be limited to an extremely low duty cycle unless the intention was to specifically show the worst case power consumption.

The MC3xPF3000xxxx, NXP's power management IC targeted for the i.MX 7Dual family of processors, supports the Power Virus mode operating at 1% duty cycle. Higher duty cycles are allowed, but a robust thermal design is required for the increased system power dissipation.

Table 12 represents the maximum momentary current transients on power lines, and should be used for power supply selection. Maximum currents are higher by far than the average power consumption of typical use cases. For typical power consumption information, see the application note, *i.MX 7DS Power Consumption Measurement* (AN5383).

Table 12. Maximum supply currents

Power Rail	Source	Conditions	Max Current	Unit
VDD_ARM	From PMIC	—	500	mA
VDD_SOC	From PMIC	—	1000	mA

power saving. For example, the PMIC can change the DCDC rails to PFM mode to reduce the power consumption.

The power consumption in low power modes is defined in Table 15.

Table 15. Low Power Measurements

Power rail	System IDLE			Low Power IDLE			SUSPEND			LPSR		
	Voltage	Current	Power	Voltage	Current	Power	Voltage	Current	Power	Voltage	Current	Power
	(V)	(mA)	(mW)	(V)	(mA)	(mW)	(V)	(mA)	(mW)	(V)	(mA)	(mW)
VDD_ARM	1.0	2.7	2.70	1.0	0.428	0.43	1.0	0.3	0.30	0.0	—	0.00
VDD_SOC	1.0	19.38	19.38	1.0	1.423	1.42	1.0	0.6	0.60	0.0	—	0.00
VDDA_1P8_IN	1.8	3.46	6.23	1.8	0.206	0.37	1.8	0.4	0.72	0.0	—	0.00
VDD_SNVS_IN	3.0	0.006	0.018	3.0	0.005	0.015	3.0	0.006	0.018	3.0	0.003	0.009
VDD_LPSR_IN	1.8	0.04	0.07	1.8	0.041	0.07	1.8	0.039	0.0702	1.8	0.04	0.07
NVCC_GPIO1/2	1.8	0.072	0.13	1.8	0.073	0.13	1.8	0.072	0.13	1.8	0.072	0.13
Total	**—**	**—**	**28.53**	**—**	**—**	**2.45**	**—**	**—**	**1.84**	**—**	**—**	**0.21**

All the power numbers defined in Table 15 are based on typical silicon at 25°C.

4.1.7 USB PHY Suspend current consumption

4.1.7.1 Low Power Suspend Mode

The VBUS Valid comparators and their associated bandgap circuits are enabled by default. Table 16 shows the USB interface current consumption in Suspend mode with default settings.

Table 16. USB PHY current consumption with default settings[1]

	VDD_USB_OTG1_3P3_IN	VDD_USB_OTG2_3P3_IN
Current	790 uA	790 uA

1 Low Power Suspend is enabled by setting USBx_PORTSC1 [PHCD]=1 [Clock Disable (PLPSCD)].

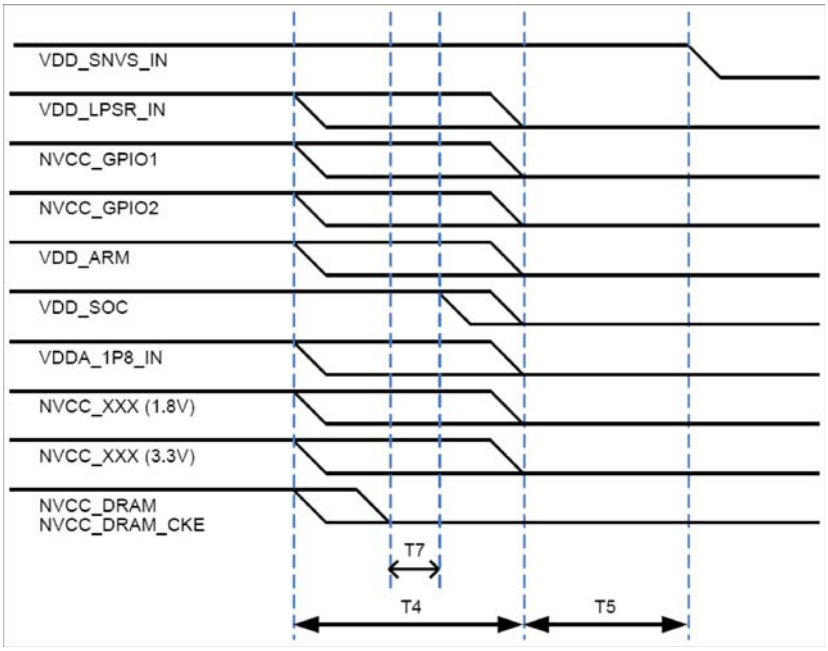

Figure 5. i.MX 7Dual power-down sequence

4.1.11 Power supplies usage

I/O pins should not be externally driven while the I/O power supply for the pin (NVCC_xxx) is OFF. This can cause internal latch-up and malfunctions due to reverse current flows. For information about I/O power supply of each pin, see "Power Rail" columns in pin list tables of Section 6, "Package information and contact assignments."

4.2 Integrated LDO voltage regulator parameters

Various internal supplies can be powered from internal LDO voltage regulators. All the supply pins named *_CAP must be connected to external capacitors. The onboard LDOs are intended for internal use only and should not be used to power any external circuitry. See the *i.MX 7Dual Application Processor Reference Manual* (IMX7DRM) for details on the power tree scheme.

NOTE

The *_CAP signals must not be powered externally. The *_CAP pins are for the bypass capacitor connection only.

4.2.1 Internal regulators

Table 26. LDO parameters

Parameter	Min	Max	Units
PVCC_GPIO_AT3P3_1P8	1.6	1.98	V
VDD_1P2	1.1	1.32	V
LPSR_1P0	0.95	1.155	V
VDDA_PHY_1P8	1.6	1.98	V
USB_OTG1_1P0	0.95	1.155	V

4.2.1.1 LDO_1P2

The LDO_1P2 regulator implements a programmable linear-regulator function from VDDA_1P8_IN (see Table 9 for minimum and maximum input requirements). The typical output of the LDO, VDD_1P2_CAP, is 1.2 V. It is intended for use with the USB HSIC PHY, which uses this voltage level for its output driver. For additional information, see the “Power Management Unit (PMU)” chapter of the *i.MX 7Dual Application Processor Reference Manual* (IMX7DRM).

4.2.1.2 LDO_1P0D

The LDO_1P0D regulator implements a programmable linear-regulator function from VDDA_1P8_IN (see Table 9 for minimum and maximum input requirements). The typical output of the LDO, VDD_1P0D_CAP, is 1.0 V. It is intended for use with the internal physical interfaces, including MIPI and PCIe PHY. For additional information, see the *i.MX 7Dual Application Processor Reference Manual* (IMX7DRM).

4.2.1.3 LDO_1P0A

The LDO_1P0A regulator implements a programmable linear-regulator function from VDDA_1P8_IN (see Table 9 for minimum and maximum input requirements). The typical output of the LDO, VDD_1P0A_CAP, is 1.0 V. It is intended for use with the internal analog modules, including the XTAL, ADC, PLL, and Temperature Sensor. For additional information, see the *i.MX 7Dual Application Processor Reference Manual* (IMX7DRM).

4.2.1.4 LDO_USB1_1PO/LDO_USB2_1P0

The LDO_USB1_1P0/LDO_USB2_1P0 regulators implement a fixed linear-regulator function from VDD_USB_OTG1_3P3_IN and VDD_USB_OTG2_3P3_IN power inputs respectively (see Table 9 for minimum and maximum input requirements). The typical output voltage is 1.0 V. It is intended for use with the internal USB physical interfaces (USB PHY1 and USB PHY2). For additional information, see the *i.MX 7Dual Application Processor Reference Manual* (IMX7DRM).

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR3 and DDR3 modes
- Differential I/O (CCM_CLK1)

4.5.1 General purpose I/O (GPIO) DC parameters

Table 29 shows DC parameters for GPIO pads. The parameters in Table 29 are guaranteed per the operating ranges in Table 9, unless otherwise noted.

Table 29. GPIO DC Parameters

Parameter	Symbol	Test Conditions	Min	Max	Units
High-level output voltage	V_{OH}	I_{OH}= –1.8mA, –3.6mA, –7.2mA, –10.8mA	0.8 × OVDD	OVDD	V
Low-level output voltage	V_{OL}	I_{OL}=1.8mA, 3.6mA, 7.2mA, 10.8mA	0	0.2 × OVDD	V
High-level input voltage	V_{IH}	—	0.7 × OVDD	OVDD + 0.3	V
Low-level input voltage	V_{IL}	—	–0.3	0.3 × OVDD	V
Input hysteresis	V_{HYS}	—	0.15	—	V
Pull-up resistor (5_kΩ PU)	—	V_{DD} = 1.8 ± 0.15 V	5.94	5.98	KΩ
Pull-up resistor (5_kΩ PU)	—	V_{DD} = 3.3 ± 0.3 V	4.8	5.3	KΩ
Pull-up resistor (47_kΩ PU)	—	V_{DD} = 1.8 ± 0.15 V	46.1	50.6	KΩ
Pull-up resistor (47_kΩ PU)	—	V_{DD} = 3.3 ± 0.3 V	45.8	49.8	KΩ
Pull-up resistor (100_kΩ PU)	—	V_{DD} = 1.8 ± 0.15 V	97.5	105.9	KΩ
Pull-up resistor (100_kΩ PU)	—	V_{DD} = 3.3 ± 0.3 V	101	105	KΩ
Pull-down resistor (100_kΩ PU)	—	V_{DD} = 1.8 ± 0.15 V	101	108.6	KΩ
Pull-down resistor (100_kΩ PD)	—	V_{DD} = 3.3 ± 0.3 V	101	108	KΩ
Input current (no PU/PD)	I_{OZ}	—	–5	5	μA
Sink/source current in Push-Pull mode	—	Driving currents (@100MHz, V_{OL}/H = 0.5×OV_{DD}, SS, 125°C) OV_{DD} = 2.7 V	–32.9	32.9	mA

4.5.2 DDR I/O DC electrical characteristics

The DDR I/O pads support DDR3/DDR3L, LPDDR2, and LPDDR3 operational modes. The DDR Memory Controller (DDRMC) is designed to be compatible with JEDEC-compliant SDRAMs. The DDRC supports the following memory types:

- DDR3 SDRAM compliant to JESD79-3E DDR3 JEDEC standard release July, 2010
- LPDDR2 SDRAM compliant to JESD209-2B LPDDR2 JEDEC standard release June, 2009
- LPDDR3 SDRAM compliant to JESD209-3B LPDDR3 JEDEC standard release August, 2013

4.8.3.3 Examples of EIM synchronous accesses

Table 45. EIM bus timing parameters [1]

ID	Parameter	BCD = 0		BCD = 1		BCD = 2		BCD = 3	
		Min	Max	Min	Max	Min	Max	Min	Max
WE1	EIM_BCLK Cycle time[2]	t	—	2 x t	—	3 x t	—	4 x t	—
WE2	EIM_BCLK Low Level Width	0.4 x t	—	0.8 x t	—	1.2 x t	—	1.6 x t	—
WE3	EIM_BCLK High Level Width	0.4 x t	—	0.8 x t	—	1.2 x t	—	1.6 x t	—
WE4	Clock rise to address valid[3]	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	-t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE5	Clock rise to address invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE6	Clock rise to EIM_CSx_B valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE7	Clock rise to EIM_CSx_B invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE8	Clock rise to EIM_WE_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE9	Clock rise to EIM_WE_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE10	Clock rise to EIM_OE_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE11	Clock rise to EIM_OE_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE12	Clock rise to EIM_EBx_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE13	Clock rise to EIM_EBx_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE14	Clock rise to EIM_LBA_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE15	Clock rise to EIM_LBA_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE16	Clock rise to Output Data Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	- t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE17	Clock rise to Output Data Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t +1.75	2 x t - 1.25	2 x t + 1.75
WE18	Input Data setup time to Clock rise	2	—	4	—	—	—	—	—
WE19	Input Data hold time from Clock rise	2	—	2	—	—	—	—	—
WE20	EIM_WAIT_B setup time to Clock rise	2	—	4	—	—	—	—	—
WE21	EIM_WAIT_B hold time from Clock rise	2	—	2	—	—	—	—	—

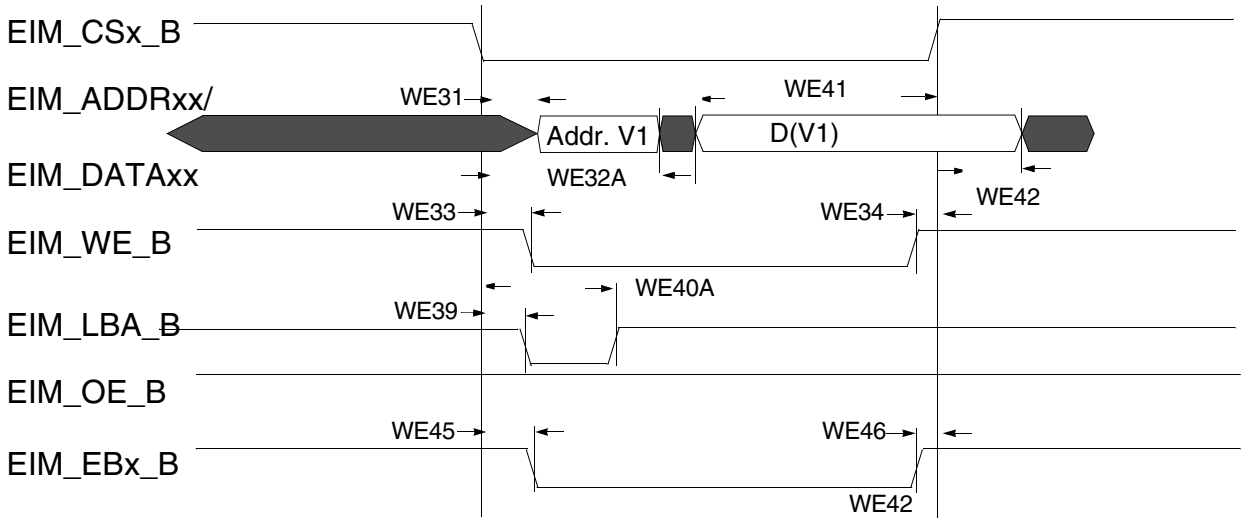

Figure 21. Asynchronous A/D muxed write access

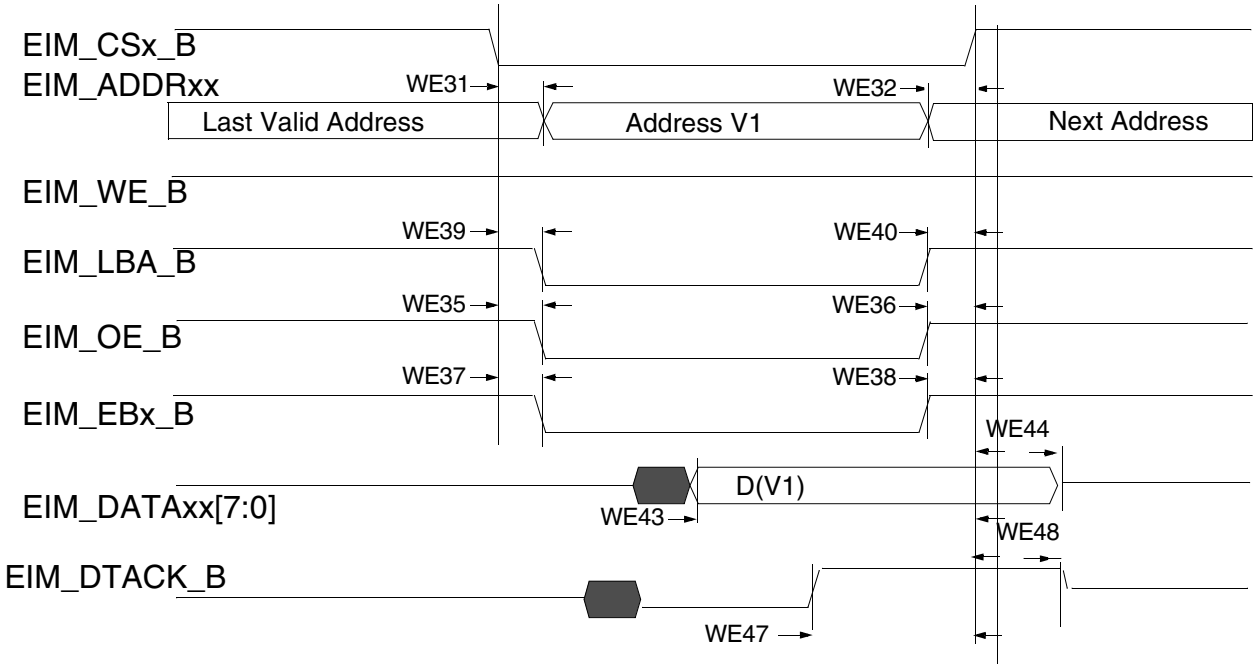

Figure 22. DTACK mode read access (DAP=0)

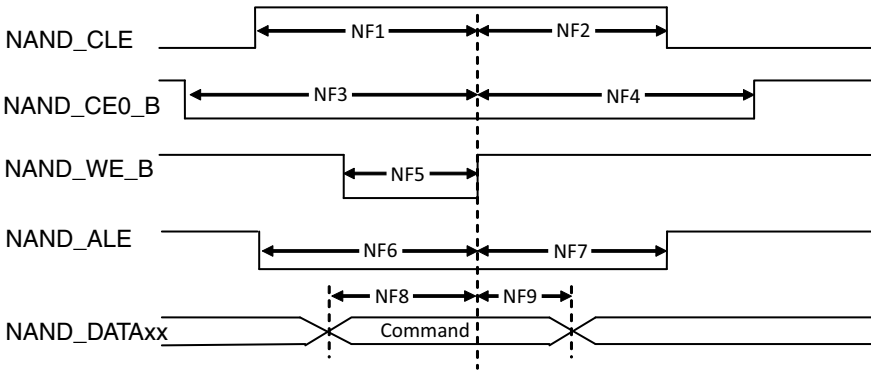

Figure 33. Command Latch cycle timing diagram

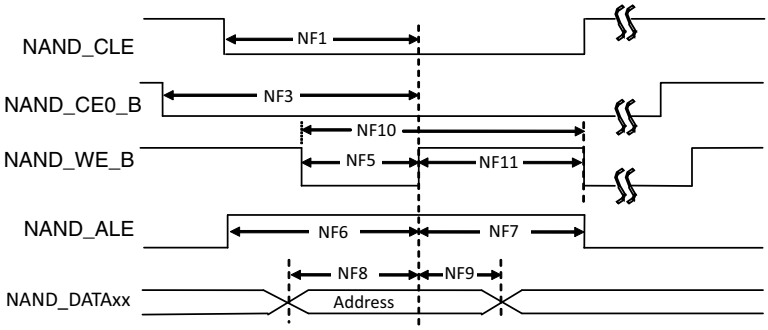

Figure 34. Address Latch cycle timing diagram

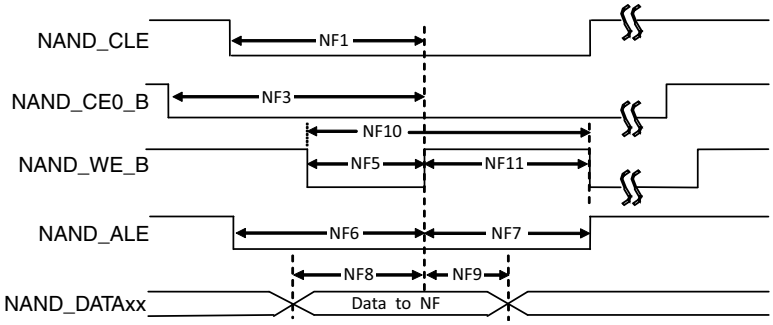

Figure 35. Write Data Latch cycle timing diagram

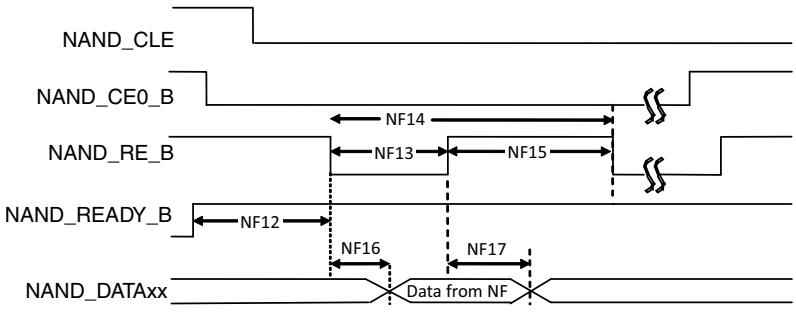

Figure 36. Read Data Latch cycle timing diagram (Non-EDO Mode)

Table 61. SD/eMMC4.3 interface timing specification(continued)

ID	Parameter	Symbols	Min	Max	Unit
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD7	uSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD8	uSDHC Input Hold Time[4]	t_{IH}	1.5	—	ns

1 In Low-Speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

2 In Normal (Full) -Speed mode for SD/SDIO card, clock frequency can be any value between 0—25 MHz. In High-speed mode, clock frequency can be any value between 0—50 MHz.

3 In Normal (Full) -Speed mode for MMC card, clock frequency can be any value between 0—20 MHz. In High-speed mode, clock frequency can be any value between 0—52 MHz.

4 To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

4.10.2.2 eMMC4.4/4.41 (dual data rate) AC timing

Figure 47 depicts the timing of eMMC4.4/4.41. Table 62 lists the eMMC4.4/4.41 timing characteristics. Be aware that only DATA is sampled on both edges of the clock (not applicable to CMD).

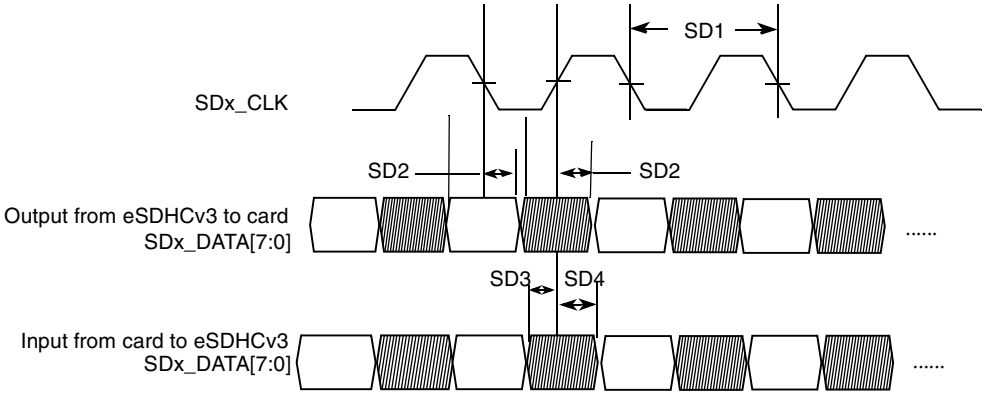

Figure 47. eMMC4.4/4.41 timing

Table 62. eMMC4.4/4.41 interface timing specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (eMMC4.4/4.41 DDR)	f_{PP}	0	52	MHz
SD1	Clock Frequency (SD3.0 DDR)	f_{PP}	0	50	MHz
uSDHC Output / Card Inputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD2	uSDHC Output Delay	t_{OD}	2.7	6.9	ns
uSDHC Input / Card Outputs SD_CMD, SDx_DATAx (Reference to CLK)					

4.10.3.1.3 MII asynchronous inputs signal timing (ENET_CRS and ENET_COL)

Figure 53 shows MII asynchronous input timings. Table 68 describes the timing parameter (M9) shown in the figure.

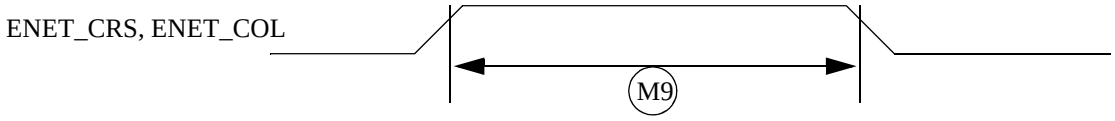

Figure 53. MII async inputs timing diagram

Table 68. MII asynchronous inputs signal timing

ID	Characteristic	Min.	Max.	Unit
M9[1]	ENET_CRS to ENET_COL minimum pulse width	1.5	—	ENET_TX_CLK period

[1] ENET_COL has the same timing in 10-Mbit 7-wire interface mode.

4.10.3.1.4 MII Serial management channel timing (ENET_MDIO and ENET_MDC)

The MDC frequency is designed to be equal to or less than 2.5 MHz to be compatible with the IEEE 802.3 MII specification. However the ENET can function correctly with a maximum MDC frequency of 15 MHz.

Figure 54 shows MII asynchronous input timings. Table 69 describes the timing parameters (M10–M15) shown in the figure.

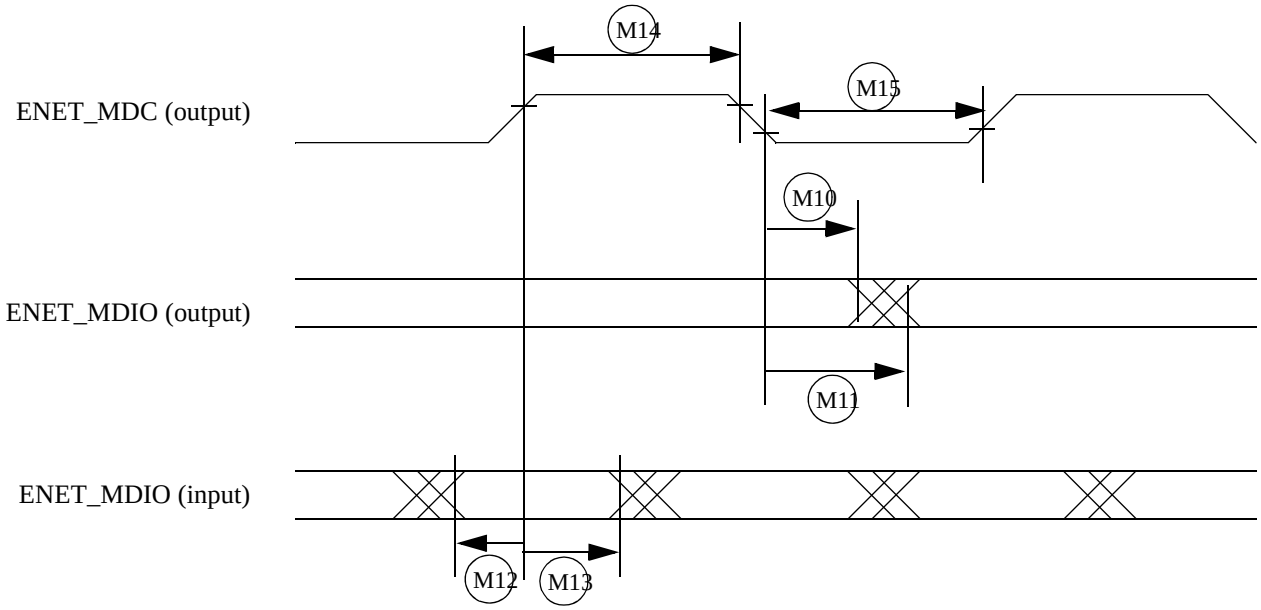

Figure 54. MII serial management channel timing diagram

Table 70. RMII signal timing

ID	Characteristic	Min.	Max.	Unit
M16	ENET_CLK pulse width high	35%	65%	ENET_CLK period
M17	ENET_CLK pulse width low	35%	65%	ENET_CLK period
M18	ENET_CLK to ENET0_TXD[1:0], ENET_TX_DATA invalid	4	—	ns
M19	ENET_CLK to ENET0_TXD[1:0], ENET_TX_DATA valid	—	15	ns
M20	ENET_RX_DATAD[1:0], ENET_RX_EN(ENET_RX_EN), ENET_RX_ER to ENET_CLK setup	4	—	ns
M21	ENET_CLK to ENET_RX_DATAD[1:0], ENET_RX_EN, ENET_RX_ER hold	2	—	ns

4.10.3.3 Signal switching specifications

The following timing specifications meet the requirements for RGMII interfaces for a range of transceiver devices.

Table 71. RGMII signal switching specifications[1]

Symbol	Description	Min.	Max.	Unit
T_{cyc}[2]	Clock cycle duration	7.2	8.8	ns
T_{skewT}[3]	Data to clock output skew at transmitter	-500	500	ps
T_{skewR}[3]	Data to clock input skew at receiver	1	2.6	ns
Duty_G[4]	Duty cycle for Gigabit	45	55	%
Duty_T[4]	Duty cycle for 10/100T	40	60	%
Tr/Tf	Rise/fall time (20–80%)	—	0.75	ns

1 The timings assume the following configuration:
DDR_SEL = (11)b
DSE (drive-strength) = (111)b

2 For 10 Mbps and 100 Mbps, T_{cyc} will scale to 400 ns ±40 ns and 40 ns ±4 ns respectively.

3 For all versions of RGMII prior to 2.0; This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns and less than 2.0 ns will be added to the associated clock signal. For 10/100, the Max value is unspecified.

4 Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.

(VSYNC), then CSI_HSYNC (HSYNC) is asserted and holds for the entire line. The pixel clock, CSI_PIXCLK (PIXCLK), is valid as long as HSYNC is asserted.

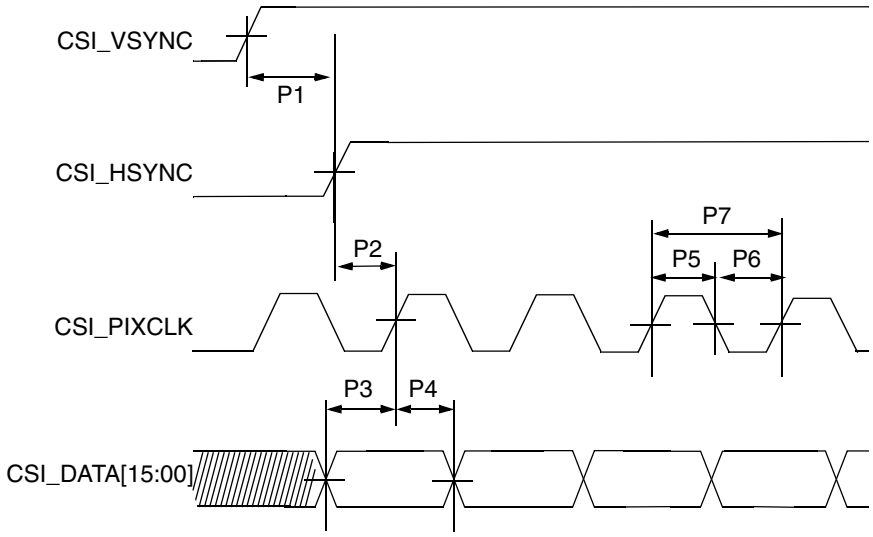

Figure 61. CSI Gated Clock Mode—Sensor Data at Falling Edge, Latch Data at Rising Edge

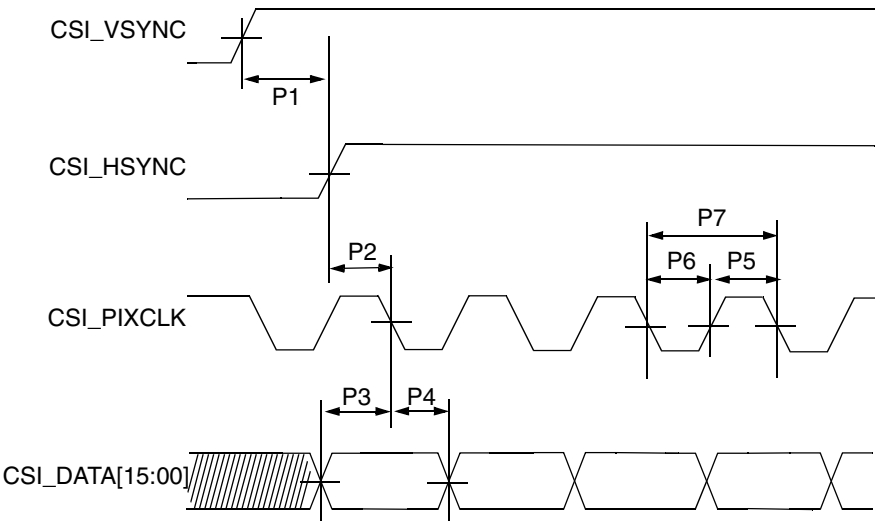

Figure 62. CSI Gated Clock Mode—Sensor Data at Rising Edge, Latch Data at Falling Edge

Table 74. CSI Gated Clock Mode Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
P1	CSI_VSYNC to CSI_HSYNC time	tV2H	33.5	—	ns
P2	CSI_HSYNC setup time	tHsu	1	—	ns
P3	CSI DATA setup time	tDsu	1	—	ns

Table 77. Electrical and Timing Information(continued)

Symbol	Parameters	Test Conditions	Min	Typ	Max	Unit
LP Line Drivers AC Specifications						
t_{rlp},t_{flp}	Single ended output rise/fall time	15% to 85%, C_L<70 pF	—	—	25	ns
t_{reo}		30% to 85%, C_L<70 pF	—	—	35	ns
$\delta V/\delta t_{SR}$	Signal slew rate	15% to 85%, C_L<70 pF	—	—	120	mV/ns
C_L	Load capacitance	—	0	—	70	pF
HS Line Receiver AC Specifications						
$t_{SETUP[RX]}$	Data to Clock Receiver Setup time	—	0.15	—	—	UI
$t_{HOLD[RX]}$	Clock to Data Receiver Hold time	—	0.15	—	—	UI
$\Delta V_{CMRX(HF)}$	Common mode interference beyond 450 MHz	—	—	—	200	mVpp
$\Delta V_{CMRX(LF)}$	Common mode interference between 50 MHz and 450 MHz.	—	-50	—	50	mVpp
C_{CM}	Common mode termination	—	—	—	60	pF
LP Line Receiver AC Specifications						
e_{SPIKE}	Input pulse rejection	—		—	300	Vps
T_{MIN}	Minimum pulse response	—	50	—		ns
V_{INT}	Pk-to-Pk interference voltage	—	—	—	400	mV
f_{INT}	Interference frequency	—	450	—	—	MHz
Model Parameters used for Driver Load switching performance evaluation						
C_{PAD}	Equivalent Single ended I/O PAD capacitance.	—	—	—	1	pF
C_{PIN}	Equivalent Single ended Package + PCB capacitance.	—	—	—	2	pF
L_S	Equivalent wire bond series inductance	—	—	—	1.5	nH
R_S	Equivalent wire bond series resistance	—	—	—	0.15	Ω
R_L	Load resistance	—	80	100	125	Ω

Table 85. Master mode SAI timing(continued)

Num	Characteristic	Min	Max	Unit
S5	SAI_BCLK to SAI_FS output valid	—	15	ns
S6	SAI_BCLK to SAI_FS output invalid	0	—	ns
S7	SAI_BCLK to SAI_TXD valid	—	15	ns
S8	SAI_BCLK to SAI_TXD invalid	0	—	ns
S9	SAI_RXD/SAI_FS input setup before SAI_BCLK	15	—	ns
S10	SAI_RXD/SAI_FS input hold after SAI_BCLK	0	—	ns

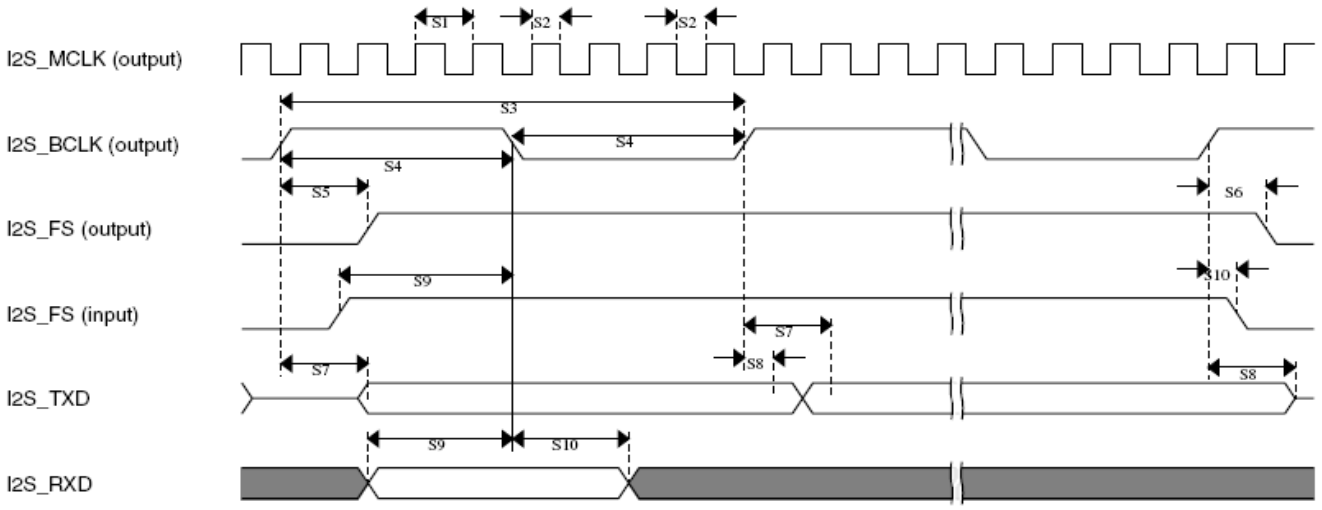

Figure 77. SAI timing — master modes

Table 86. Master mode SAI timing

Num	Characteristic	Min	Max	Unit
S11	SAI_BCLK cycle time (input)	40	—	ns
S12	SAI_BCLK pulse width high/low (input)	40%	60%	BCLK period
S13	SAI_FS input setup before SAI_BCLK	10	—	ns
S14	SAI_FA input hold after SAI_BCLK	2	—	ns
S15	SAI_BCLK to SAI_TXD/SAI_FS output valid	—	20	ns
S16	SAI_BCLK to SAI_TXD/SAI_FS output invalid	0	—	ns
S17	SAI_RXD setup before SAI_BCLK	10	—	ns
S18	SAI_RXD hold after SAI_BCLK	2	—	ns

NOTE

HSIC is DDR signal, following timing spec is for both rising and falling edge.

4.10.15.1 Transmit timing

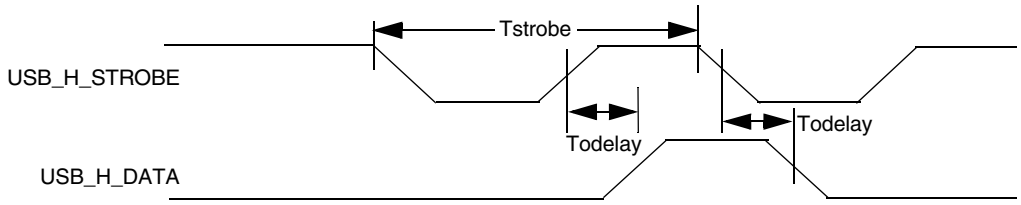

Figure 85. USB HSIC transmit waveform

Table 91. USB HSIC transmit parameters

Name	Parameter	Min	Max	Unit	Comment
Tstrobe	strobe period	4.165	4.169	ns	
Todelay	data output delay time	550	1350	ps	Measured at 50% point
Tslew	strobe/data rising/falling time	0.7	2	V/ns	Averaged from 30% – 70% points

4.10.15.2 Receive timing

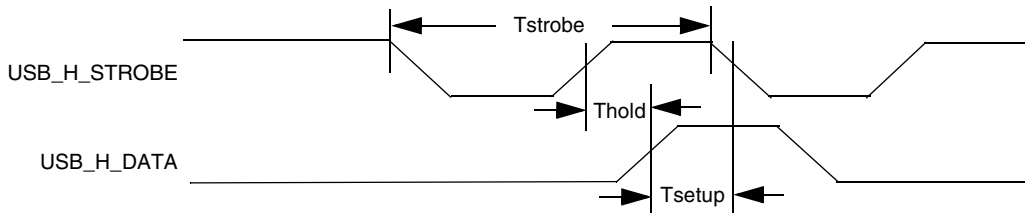

Figure 86. USB HSIC receive waveform

Table 92. USB HSIC receive parameters[1]

Name	Parameter	Min	Max	Unit	Comment
Tstrobe	strobe period	4.165	4.169	ns	
Thold	data hold time	300		ps	Measured at 50% point
Tsetup	data setup time	365		ps	Measured at 50% point
Tslew	strobe/data rising/falling time	0.7	2	V/ns	Averaged from 30% – 70% points

1 The timings in the table are guaranteed when:
—AC I/O voltage is between 0.9x to 1x of the I/O supply
—DDR_SEL configuration bits of the I/O are set to (10)b

6 Package information and contact assignments

This section includes the contact assignment information and mechanical package drawing.

6.1 12 x 12 mm package information

6.1.1 Case 1997-01, 12 x 12, 0.4 mm pitch, ball matrix

The following figure shows the top, bottom, and side views of the 12×12 mm BGA package.

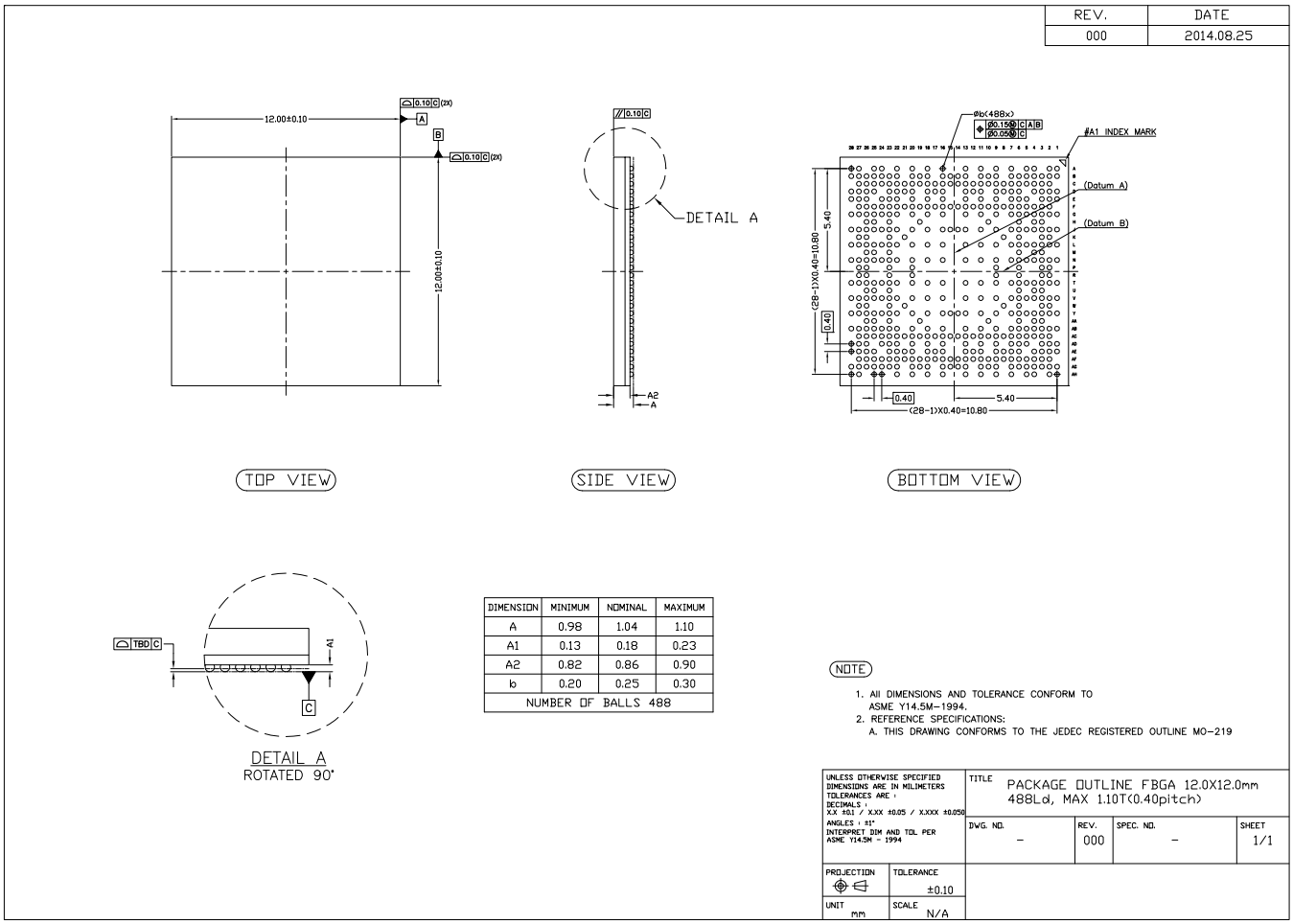

Figure 87. 12 x 12 mm BGA, Case x Package Top, Bottom, and Side Views

Table 99. i.MX 7Dual 12 x 12 mm functional contact assignments(continued)

Ball	Ball Name	Power Group	Ball type[1]	Default Mode[1]	Default Function[1]	PD/PU
P27	EPDC_D06	NVCC_EPDC1	GPIO	ALT5	GPIO2_IO[6]	100K PD
N28	EPDC_D07	NVCC_EPDC1	GPIO	ALT5	GPIO2_IO[7]	100K PD
N27	EPDC_D08	NVCC_EPDC1	GPIO	ALT5	GPIO2_IO[8]	100K PD
N26	EPDC_D09	NVCC_EPDC1	GPIO	ALT5	GPIO2_IO[9]	100K PD
N25	EPDC_D10	NVCC_EPDC1	GPIO	ALT5	GPIO2_IO[10]	100K PD
N24	EPDC_D11	NVCC_EPDC1	GPIO	ALT5	GPIO2_IO[11]	100K PD
M26	EPDC_D12	NVCC_EPDC1	GPIO	ALT5	GPIO2_IO[12]	100K PD
L26	EPDC_D13	NVCC_EPDC1	GPIO	ALT5	GPIO2_IO[13]	100K PD
L25	EPDC_D14	NVCC_EPDC1	GPIO	ALT5	GPIO2_IO[14]	100K PD
N22	EPDC_D15	NVCC_EPDC1	GPIO	ALT5	GPIO2_IO[15]	100K PD
J23	EPDC_GDCLK	NVCC_EPDC2	GPIO	ALT5	GPIO2_IO[24]	100K PD
J22	EPDC_GDOE	NVCC_EPDC2	GPIO	ALT5	GPIO2_IO[25]	100K PD
L24	EPDC_GDRL	NVCC_EPDC2	GPIO	ALT5	GPIO2_IO[26]	100K PD
K27	EPDC_GDSP	NVCC_EPDC2	GPIO	ALT5	GPIO2_IO[27]	100K PD
J27	EPDC_PWRCOM	NVCC_EPDC2	GPIO	ALT5	GPIO2_IO[30]	100K PD
J26	EPDC_PWRSTAT	NVCC_EPDC2	GPIO	ALT5	GPIO2_IO[31]	100K PD
J25	EPDC_SDCE0	NVCC_EPDC2	GPIO	ALT5	GPIO2_IO[20]	100K PD
J24	EPDC_SDCE1	NVCC_EPDC2	GPIO	ALT5	GPIO2_IO[21]	100K PD
G22	EPDC_SDCE2	NVCC_EPDC2	GPIO	ALT5	GPIO2_IO[22]	100K PD
G23	EPDC_SDCE3	NVCC_EPDC2	GPIO	ALT5	GPIO2_IO[23]	100K PD
G24	EPDC_SDCLK	NVCC_EPDC2	GPIO	ALT5	GPIO2_IO[16]	100K PD
J28	EPDC_SDLE	NVCC_EPDC2	GPIO	ALT5	GPIO2_IO[17]	100K PD
G25	EPDC_SDOE	NVCC_EPDC2	GPIO	ALT5	GPIO2_IO[18]	100K PD
F26	EPDC_SDSHR	NVCC_EPDC2	GPIO	ALT5	GPIO2_IO[19]	100K PD
AF02	GPANAIO	VDDA_1P8	GPIO		GPANAIO	
V04	GPIO1_IO00	NVCC_GPIO1	GPIO	ALT0	GPIO1_IO00	100K PU
V05	GPIO1_IO01	NVCC_GPIO1	GPIO	ALT0	GPIO1_IO01	100K PD
Y07	GPIO1_IO02	NVCC_GPIO1	GPIO	ALT0	GPIO1_IO02	100K PD
Y06	GPIO1_IO03	NVCC_GPIO1	GPIO	ALT0	GPIO1_IO03	100K PD
Y05	GPIO1_IO04	NVCC_GPIO1	GPIO	ALT0	GPIO1_IO04	100K PD
Y04	GPIO1_IO05	NVCC_GPIO1	GPIO	ALT0	GPIO1_IO05	100K PD
V06	GPIO1_IO06	NVCC_GPIO1	GPIO	ALT0	GPIO1_IO06	100K PD

Table 100. i.MX 7Dual 12 x 12 mm 0.4 mm pitch ball map(continued)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	
H			SD2_DATA2	VSS		VSS				VDD_SOC									VDD_ARM				VSS		VSS	LCD1_DATA21			**H**
J	SD3_STROBE	SD3_RESET_B	SD2_RESET_B	SD3_DATA7	SD3_DATA6	SD3_CLK	SD3_DATA5		VDD_SOC		NVCC_SD1		NVCC_SAI	PVCC_SAI_SD_CAP	VDDA_MIPI_1P8	VDD_MIPI_1P0		NVCC_ENET1		VDD_ARM		EPDC1_GDOE	EPDC1_GDCLK	EPDC1_SDCE1	EPDC1_SDCE0	EPDC1_PWRSTAT	EPDC1_PWRCOM	EPDC1_SDLE		**J**
K		ECSPI1_SCLK	VDD_SOC					VDD_SOC													VDD_ARM		VDD_ARM			VDD_ARM	EPDC1_GDSP			**K**
L	VDD_SOC	VDD_SOC	ECSPI1_MOSI	SD3_CMD	SD3_DATA4	SD3_DATA3	SD3_DATA2		NVCC_SD2		VDD_SOC		VSS			VSS		VDD_SOC		NVCC_LCD		EPDC1_BDR1	EPDC1_BDR0	EPDC1_GDRL	EPDC1_DATA14	EPDC1_DATA13	VDD_ARM	VDD_ARM	**L**
M			ECSPI1_MISO	VSS		VSS																			VSS	EPDC1_DATA12			**M**
N	ECSPI2_SCLK	ECSPI2_MOSI	ECSPI1_SS0	I2C1_SCL	I2C1_SDA	I2C2_SCL	I2C2_SDA		NVCC_SD3		VSS		VDD_SOC			VDD_SOC		VSS		NVCC_EPDC2		EPDC1_DATA15	EPDC1_DATA04	EPDC1_DATA11	EPDC1_DATA10	EPDC1_DATA09	EPDC1_DATA08	EPDC1_DATA07	**N**
P		ECSPI2_MISO	VDD_SOC			VDD_SOC			NVCC_SPI											NVCC_EPDC1			VDD_SOC			VDD_SOC	EPDC1_DATA06		**P**
R		ECSPI2_SS0	VDD_SOC			VDD_SOC			NVCC_I2C											PVCC_EPDC_LCD_CAP			VDD_SOC			VDD_SOC	EPDC1_DATA03			**R**
T	UART1_RXD	UART2_RXD	UART2_TXD	I2C4_SDA	I2C4_SCL	I2C3_SCL	I2C3_SDA		NVCC_UART		VSS		VDD_SOC			VDD_SOC		VSS		DRAM_VREF		DRAM_DATA27	DRAM_DATA26	DRAM_DATA31	DRAM_DATA30	EPDC1_DATA02	EPDC1_DATA00	EPDC1_DATA05	**T**
U			UART3_TXD	VSS		VSS																	VSS		VSS	EPDC1_DATA01			**U**
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	

Table 100. i.MX 7Dual 12 x 12 mm 0.4 mm pitch ball map(continued)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	
AF		GPANAIO	VSS	VDDA_1P8_IN	VSS	TEMPSENSOR_RESERVE	TEMPSENSOR_REXT	VSS	VSS	VSS	VSS	VDDD_1P0_CAP	VSS	VSS	VSS	DRAM_ODT0	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	DRAM_DATA04	DRAM_DATA06	DRAM_DATA03	DRAM_ADDR06	VSS	DRAM_SDCLK0_N	VSS	DRAM_SDBA2		**AF**
AG	XTALO	XTALI	VDDA_1P8_IN	VDDA_1P8_IN	VDD_LPSR_IN	VDD_LPSR_1P0_CAP	VDD_SNVS_1P8_CAP		RTC_XTALI	VSS	PCIE_REFCLKOUT_N		PCIE_REFCLKIN_N	PCIE_TX_N	PCIE_TX_P	PCIE_RX_N		NVCC_DRAM	DRAM_DATA01	DRAM_DATA02		DRAM_DATA05	DRAM_SDQS0_N	DRAM_SDQS0_P	DRAM_CAS_B	DRAM_ADDR15	DRAM_ADDR11	DRAM_ADDR13	**AG**
AH	VSS	VDD_XTAL_1P8		VDDA_ADC1_1P8	VDD_TEMPSENSOR_1P8		VDDA_1P0_CAP		RTC_XTALO		PCIE_REFCLKOUT_P		PCIE_REFCLKIN_P			PCIE_RX_P		NVCC_DRAM		DRAM_DATA07		DRAM_DATA00		DRAM_DQM0	DRAM_RAS_B		DRAM_SDWE_B	VSS	**AH**
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	