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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex® -M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I ² C, IrDA, SPI, UART/USART
Peripherals	DMA, I ² S, LVD, POR, PWM, WDT
Number of I/O	104
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 46x16b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk10dx128vlq10

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3.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

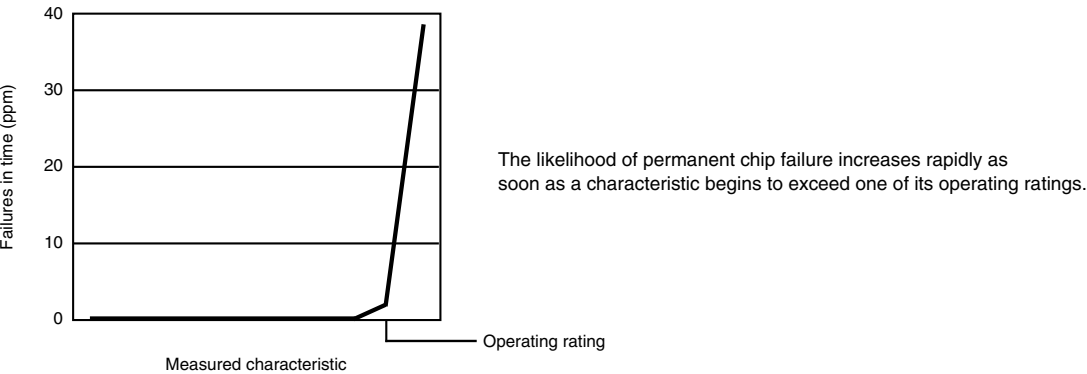
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

3.4.1 Example

This is an example of an operating rating:

Symbol	Description	Min.	Max.	Unit
V _{DD}	1.0 V core supply voltage	−0.3	1.2	V

3.5 Result of exceeding a rating



5.2.2 LVD and POR operating requirements

Table 2. V_{DD} supply LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V _{POR}	Falling VDD POR detect voltage	0.8	1.1	1.5	V	
V _{LVDH}	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
V _{LVW1H}	Low-voltage warning thresholds — high range					1
V _{LVW2H}	• Level 1 falling (LVWV=00)	2.62	2.70	2.78	V	
V _{LVW3H}	• Level 2 falling (LVWV=01)	2.72	2.80	2.88	V	
V _{LVW4H}	• Level 3 falling (LVWV=10)	2.82	2.90	2.98	V	
V _{LVW4H}	• Level 4 falling (LVWV=11)	2.92	3.00	3.08	V	
V _{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	±80	—	mV	
V _{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
V _{LVW1L}	Low-voltage warning thresholds — low range					1
V _{LVW2L}	• Level 1 falling (LVWV=00)	1.74	1.80	1.86	V	
V _{LVW3L}	• Level 2 falling (LVWV=01)	1.84	1.90	1.96	V	
V _{LVW4L}	• Level 3 falling (LVWV=10)	1.94	2.00	2.06	V	
V _{LVW4L}	• Level 4 falling (LVWV=11)	2.04	2.10	2.16	V	
V _{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	±60	—	mV	
V _{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	
t _{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	μs	

1. Rising thresholds are falling threshold + hysteresis voltage

Table 3. VBAT power operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V _{POR_VBAT}	Falling VBAT supply POR detect voltage	0.8	1.1	1.5	V	

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I _{DD_VLPW}	Very-low-power wait mode current at 3.0 V — all peripheral clocks disabled	—	0.61	—	mA	8
I _{DD_STOP}	Stop mode current at 3.0 V					
	• @ –40 to 25°C	—	0.35	0.567	mA	
	• @ 70°C	—	0.384	0.793	mA	
	• @ 105°C	—	0.628	1.2	mA	
I _{DD_VLPS}	Very-low-power stop mode current at 3.0 V					
	• @ –40 to 25°C	—	5.9	32.7	μA	
	• @ 70°C	—	26.1	59.8	μA	
	• @ 105°C	—	98.1	188	μA	
I _{DD_LLS}	Low leakage stop mode current at 3.0 V					9
	• @ –40 to 25°C	—	2.6	8.6	μA	
	• @ 70°C	—	10.3	29.1	μA	
	• @ 105°C	—	42.5	92.5	μA	
I _{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V					9
	• @ –40 to 25°C	—	1.9	5.8	μA	
	• @ 70°C	—	6.9	12.1	μA	
	• @ 105°C	—	28.1	41.9	μA	
I _{DD_VLLS2}	Very low-leakage stop mode 2 current at 3.0 V					
	• @ –40 to 25°C	—	1.59	5.5	μA	
	• @ 70°C	—	4.3	9.5	μA	
	• @ 105°C	—	17.5	34	μA	
I _{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V					
	• @ –40 to 25°C	—	1.47	5.4	μA	
	• @ 70°C	—	2.97	8.1	μA	
	• @ 105°C	—	12.41	32	μA	
I _{DD_VBAT}	Average current with RTC and 32kHz disabled at 3.0 V					
	• @ –40 to 25°C	—	0.19	0.22	μA	
	• @ 70°C	—	0.49	0.64	μA	
	• @ 105°C	—	2.2	3.2	μA	

Table continues on the next page...

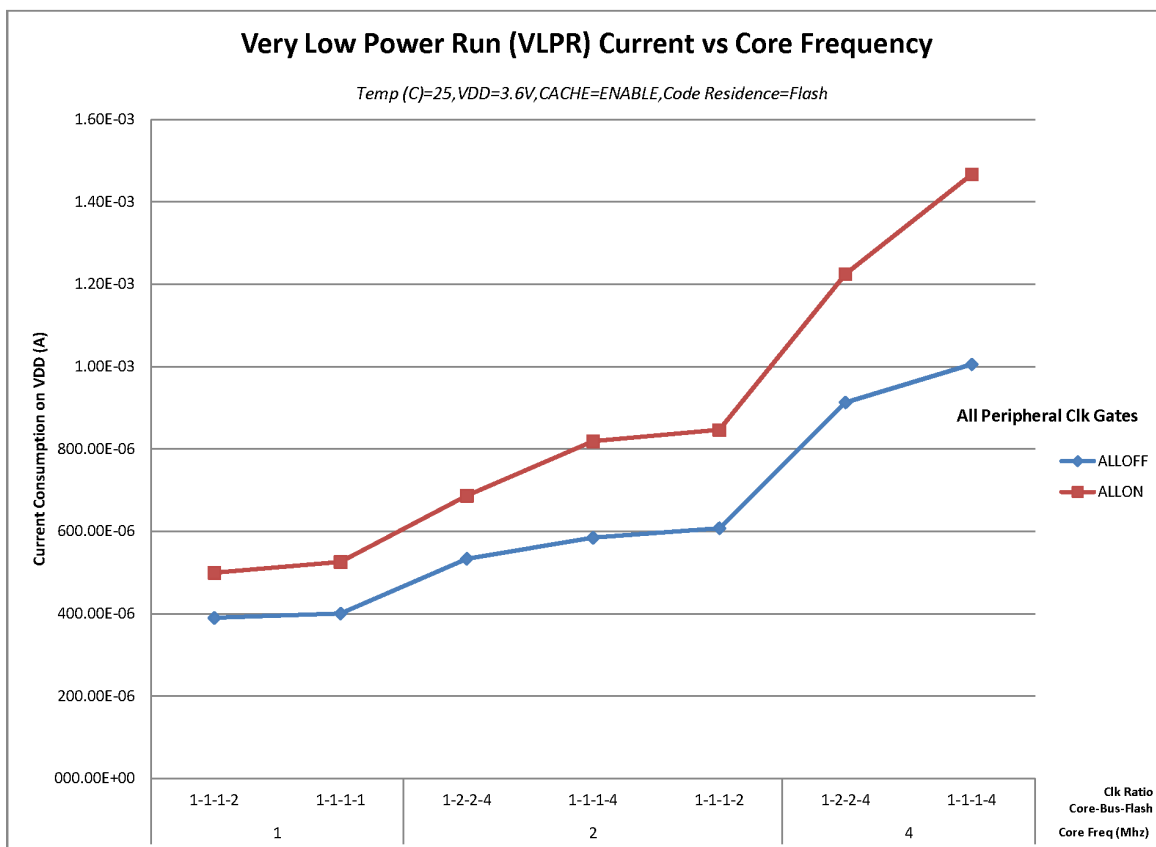


Figure 3. VLPR mode supply current vs. core frequency

5.2.6 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for “EMC design.”

5.2.7 Capacitance attributes

Table 7. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C _{IN_A}	Input capacitance: analog pins	—	7	pF
C _{IN_D}	Input capacitance: digital pins	—	7	pF

5.3 Switching specifications

5.3.1 Device clock specifications

Table 8. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
f_{SYS}	System and core clock	—	72	MHz	
f_{BUS}	Bus clock	—	50	MHz	
FB_CLK	FlexBus clock	—	50	MHz	
f_{FLASH}	Flash clock	—	25	MHz	
f_{LPTMR}	LPTMR clock	—	25	MHz	
VLPR mode ¹					
f_{SYS}	System and core clock	—	4	MHz	
f_{BUS}	Bus clock	—	4	MHz	
FB_CLK	FlexBus clock	—	4	MHz	
f_{FLASH}	Flash clock	—	0.5	MHz	
f_{ERCLK}	External reference clock	—	16	MHz	
$f_{\text{LPTMR_pin}}$	LPTMR clock	—	25	MHz	
$f_{\text{LPTMR_ERCLK}}$	LPTMR external reference clock	—	16	MHz	
$f_{\text{FlexCAN_ERCLK}}$	FlexCAN external reference clock	—	8	MHz	
$f_{\text{I2S_MCLK}}$	I2S master clock	—	12.5	MHz	
$f_{\text{I2S_BCLK}}$	I2S bit clock	—	4	MHz	

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

5.3.2 General switching specifications

These general purpose specifications apply to all signals configured for GPIO, UART, CAN, CMT, and I²C signals.

Table 9. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1, 2
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter enabled) — Asynchronous path	100	—	ns	3

Table continues on the next page...

Table 9. General switching specifications (continued)

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) — Asynchronous path	16	—	ns	3
	External reset pulse width (digital glitch filter disabled)	100	—	ns	3
	Mode select (EZP_CS) hold time after reset deassertion	2	—	Bus clock cycles	
	Port rise and fall time (high drive strength) - Slew disabled $1.71 \leq V_{DD} \leq 2.7V$ $2.7 \leq V_{DD} \leq 3.6V$ - Slew enabled $1.71 \leq V_{DD} \leq 2.7V$ $2.7 \leq V_{DD} \leq 3.6V$	— — — —	12 6 36 24	ns ns ns ns	4
	Port rise and fall time (low drive strength) - Slew disabled $1.71 \leq V_{DD} \leq 2.7V$ $2.7 \leq V_{DD} \leq 3.6V$ - Slew enabled $1.71 \leq V_{DD} \leq 2.7V$ $2.7 \leq V_{DD} \leq 3.6V$	— — — —	12 6 36 24	ns ns ns ns	5

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop, VLPS, LLS, and VLLSx modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
2. The greater synchronous and asynchronous timing must be met.
3. This is the minimum pulse width that is guaranteed to be recognized as a pin interrupt request in Stop, VLPS, LLS, and VLLSx modes.
4. 75pF load
5. 15pF load

5.4 Thermal specifications

5.4.1 Thermal operating requirements

Table 10. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T_J	Die junction temperature	−40	125	°C
T_A	Ambient temperature	−40	105	°C

Table 12. JTAG limited voltage range electricals (continued)

Symbol	Description	Min.	Max.	Unit
J1	TCLK frequency of operation - Boundary Scan - JTAG and CJTAG - Serial Wire Debug	0 0 0	10 25 50	MHz
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width - Boundary Scan - JTAG and CJTAG - Serial Wire Debug	50 20 10	— — —	ns ns ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	0	—	ns
J7	TCLK low to boundary scan output data valid	—	25	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1	—	ns
J11	TCLK low to TDO data valid	—	17	ns
J12	TCLK low to TDO high-Z	—	17	ns
J13	TRST assert time	100	—	ns
J14	TRST setup time (negation) to TCLK high	8	—	ns

Table 13. JTAG full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	TCLK frequency of operation - Boundary Scan - JTAG and CJTAG - Serial Wire Debug	0 0 0	10 20 40	MHz
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width - Boundary Scan - JTAG and CJTAG - Serial Wire Debug	50 25 12.5	— — —	ns ns ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	0	—	ns

Table continues on the next page...

Table 14. MCG specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
J_{cyc_fll}	FLL period jitter $f_{VCO} = 48 \text{ MHz}$ $f_{VCO} = 98 \text{ MHz}$	—	180	—	ps	
$t_{fll_acquire}$	FLL target frequency acquisition time	—	—	1	ms	6
PLL						
f_{vco}	VCO operating frequency	48.0	—	100	MHz	
I_{pll}	PLL operating current PLL @ 96 MHz ($f_{osc_hi_1} = 8 \text{ MHz}$, $f_{pll_ref} = 2 \text{ MHz}$, VDIV multiplier = 48)	—	1060	—	μA	7
I_{pll}	PLL operating current PLL @ 48 MHz ($f_{osc_hi_1} = 8 \text{ MHz}$, $f_{pll_ref} = 2 \text{ MHz}$, VDIV multiplier = 24)	—	600	—	μA	7
f_{pll_ref}	PLL reference frequency range	2.0	—	4.0	MHz	
J_{cyc_pll}	PLL period jitter (RMS) $f_{vco} = 48 \text{ MHz}$ $f_{vco} = 100 \text{ MHz}$	—	120	—	ps	8
J_{acc_pll}	PLL accumulated jitter over 1 μs (RMS) $f_{vco} = 48 \text{ MHz}$ $f_{vco} = 100 \text{ MHz}$	—	1350	—	ps	8
D_{lock}	Lock entry frequency tolerance	± 1.49	—	± 2.98	%	
D_{unl}	Lock exit frequency tolerance	± 4.47	—	± 5.97	%	
t_{pll_lock}	Lock detector detection time	—	—	$150 \times 10^{-6} + 1075(1/f_{pll_ref})$	s	9

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
3. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation (Δf_{dco_t}) over voltage and temperature should be considered.
4. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
5. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
6. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
7. Excludes any oscillator currents that are also consuming power while PLL is in operation.
8. This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
9. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

6.3.2 Oscillator electrical specifications

This section provides the electrical characteristics of the module.

Table 15. Oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{pp}^5	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	

- $V_{DD}=3.3$ V, Temperature =25 °C
- See crystal or resonator manufacturer's recommendation
- C_x, C_y can be provided by using either the integrated capacitors or by using external components.
- When low power mode is selected, R_F is integrated and must not be attached externally.
- The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

6.3.2.2 Oscillator frequency specifications

Table 16. Oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal or resonator frequency — low frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
$f_{osc_hi_1}$	Oscillator crystal or resonator frequency — high frequency mode (low range) (MCG_C2[RANGE]=01)	3	—	8	MHz	
$f_{osc_hi_2}$	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	8	—	32	MHz	
f_{ec_extal}	Input clock frequency (external clock mode)	—	—	50	MHz	1, 2
t_{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t_{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—	750	—	ms	3, 4
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—	250	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	—	0.6	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	—	1	—	ms	

- Other frequency limits may apply when external clock is being used as a reference for the FLL or PLL.
- When transitioning from FBE to FEI mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
- Proper PC board layout procedures must be followed to achieve specifications.

Table 20. Flash command timing specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	μs	1
t_{swapx01}	Swap Control execution time	—	200	—	μs	
t_{swapx02}	• control code 0x02	—	70	150	μs	
t_{swapx04}	• control code 0x04	—	70	150	μs	
t_{swapx08}	• control code 0x08	—	—	30	μs	
$t_{\text{pgmpart32k}}$	Program Partition for EEPROM execution time	—	70	—	ms	
	• 32 KB FlexNVM					
t_{setramff}	Set FlexRAM Function execution time:	—	50	—	μs	
t_{setram8k}	• Control Code 0xFF	—	0.3	0.5	ms	
$t_{\text{setram32k}}$	• 8 KB EEPROM backup	—	0.7	1.0	ms	
	• 32 KB EEPROM backup					
Byte-write to FlexRAM for EEPROM operation						
$t_{\text{eewr8bers}}$	Byte-write to erased FlexRAM location execution time	—	175	260	μs	3
t_{eewr8b8k}	Byte-write to FlexRAM execution time:	—	340	1700	μs	
$t_{\text{eewr8b16k}}$	• 8 KB EEPROM backup	—	385	1800	μs	
$t_{\text{eewr8b32k}}$	• 16 KB EEPROM backup	—	475	2000	μs	
	• 32 KB EEPROM backup					
Word-write to FlexRAM for EEPROM operation						
$t_{\text{eewr16bers}}$	Word-write to erased FlexRAM location execution time	—	175	260	μs	
$t_{\text{eewr16b8k}}$	Word-write to FlexRAM execution time:	—	340	1700	μs	
$t_{\text{eewr16b16k}}$	• 8 KB EEPROM backup	—	385	1800	μs	
$t_{\text{eewr16b32k}}$	• 16 KB EEPROM backup	—	475	2000	μs	
	• 32 KB EEPROM backup					
Longword-write to FlexRAM for EEPROM operation						
$t_{\text{eewr32bers}}$	Longword-write to erased FlexRAM location execution time	—	360	540	μs	
$t_{\text{eewr32b8k}}$	Longword-write to FlexRAM execution time:	—	545	1950	μs	
$t_{\text{eewr32b16k}}$	• 8 KB EEPROM backup	—	630	2050	μs	
$t_{\text{eewr32b32k}}$	• 16 KB EEPROM backup	—	810	2250	μs	
	• 32 KB EEPROM backup					

- Assumes 25 MHz flash clock frequency.
- Maximum times for erase parameters based on expectations at cycling end-of-life.
- For byte-writes to an erased FlexRAM location, the aligned word containing the byte must be erased.

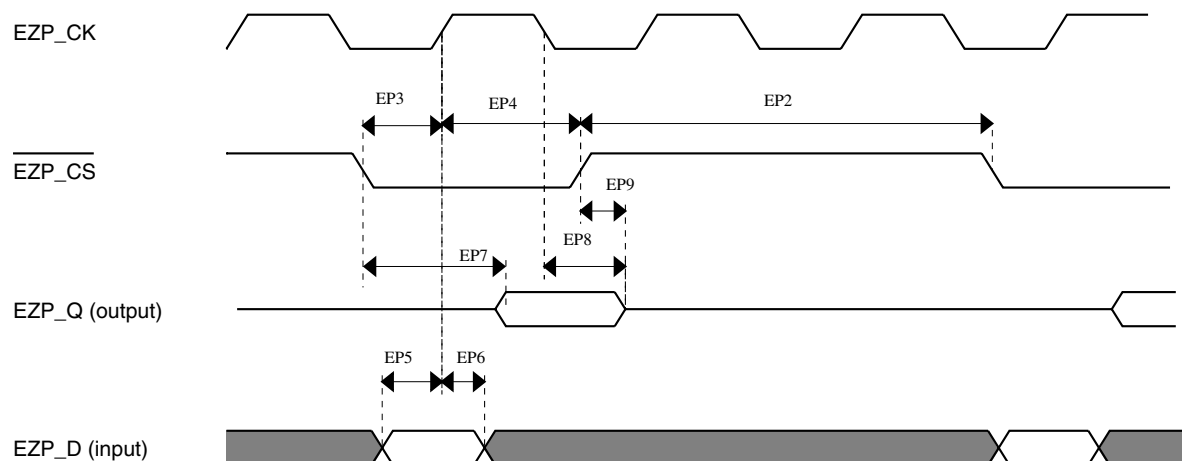


Figure 11. EzPort Timing Diagram

6.4.3 Flexbus Switching Specifications

All processor bus timings are synchronous; input setup/hold and output delay are given in respect to the rising edge of a reference clock, FB_CLK. The FB_CLK frequency may be the same as the internal system bus frequency or an integer divider of that frequency.

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the Flexbus output clock (FB_CLK). All other timing relationships can be derived from these values.

Table 24. Flexbus limited voltage range switching specifications

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	FB_CLK	MHz	
FB1	Clock period	20	—	ns	
FB2	Address, data, and control output valid	—	11.5	ns	1
FB3	Address, data, and control output hold	0.5	—	ns	1
FB4	Data and $\overline{\text{FB_TA}}$ input setup	8.5	—	ns	2
FB5	Data and $\overline{\text{FB_TA}}$ input hold	0.5	—	ns	2

1. Specification is valid for all FB_AD[31:0], $\overline{\text{FB_BE/BWEn}}$, $\overline{\text{FB_CSn}}$, $\overline{\text{FB_OE}}$, FB_R/W, $\overline{\text{FB_TBST}}$, FB_TSIZ[1:0], FB_ALE, and $\overline{\text{FB_TS}}$.

Table 27. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
f_{ADACK}	ADC asynchronous clock source	- ADLPC = 1, ADHSC = 0 - ADLPC = 1, ADHSC = 1 - ADLPC = 0, ADHSC = 0 - ADLPC = 0, ADHSC = 1	1.2 2.4 3.0 4.4	2.4 4.0 5.2 6.2	3.9 6.1 7.3 9.5	MHz MHz MHz MHz	$t_{ADACK} = 1/f_{ADACK}$
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	12-bit modes <12-bit modes	— —	±4 ±1.4	±6.8 ±2.1	LSB ⁴	5
DNL	Differential non-linearity	12-bit modes <12-bit modes	— —	±0.7 ±0.2	-1.1 to +1.9 -0.3 to 0.5	LSB ⁴	5
INL	Integral non-linearity	12-bit modes <12-bit modes	— —	±1.0 ±0.5	-2.7 to +1.9 -0.7 to +0.5	LSB ⁴	5
E_{FS}	Full-scale error	12-bit modes <12-bit modes	— —	-4 -1.4	-5.4 -1.8	LSB ⁴	$V_{ADIN} = V_{DDA}$ 5
E_Q	Quantization error	16-bit modes ≤13-bit modes	— —	-1 to 0 —	— ±0.5	LSB ⁴	
ENOB	Effective number of bits	16-bit differential mode - Avg = 32 - Avg = 4 16-bit single-ended mode - Avg = 32 - Avg = 4	12.8 11.9 12.2 11.4	14.5 13.8 13.9 13.1	— — — —	bits bits bits bits	6
SINAD	Signal-to-noise plus distortion	See ENOB	$6.02 \times \text{ENOB} + 1.76$			dB	
THD	Total harmonic distortion	16-bit differential mode - Avg = 32 16-bit single-ended mode - Avg = 32	— —	-94 -85	— —	dB dB	7
SFDR	Spurious free dynamic range	16-bit differential mode - Avg = 32 16-bit single-ended mode - Avg = 32	82 78	95 90	— —	dB dB	7

Table continues on the next page...

Table 27. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
E_{IL}	Input leakage error			$I_{IN} \times R_{AS}$		mV	I_{IN} = leakage current (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	—	1.715	—	mV/°C	
V_{TEMP25}	Temp sensor voltage	25 °C	—	719	—	mV	

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH} = V_{DDA}$
2. Typical values assume $V_{DDA} = 3.0$ V, Temp = 25°C, $f_{ADCK} = 2.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and the ADLPC bit (low power). For lowest power operation the ADLPC bit must be set, the HSC bit must be clear with 1 MHz ADC conversion clock speed.
4. $1 \text{ LSB} = (V_{REFH} - V_{REFL})/2^N$
5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
7. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.

Typical ADC 16-bit Differential ENOB vs ADC Clock
100Hz, 90% FS Sine Input

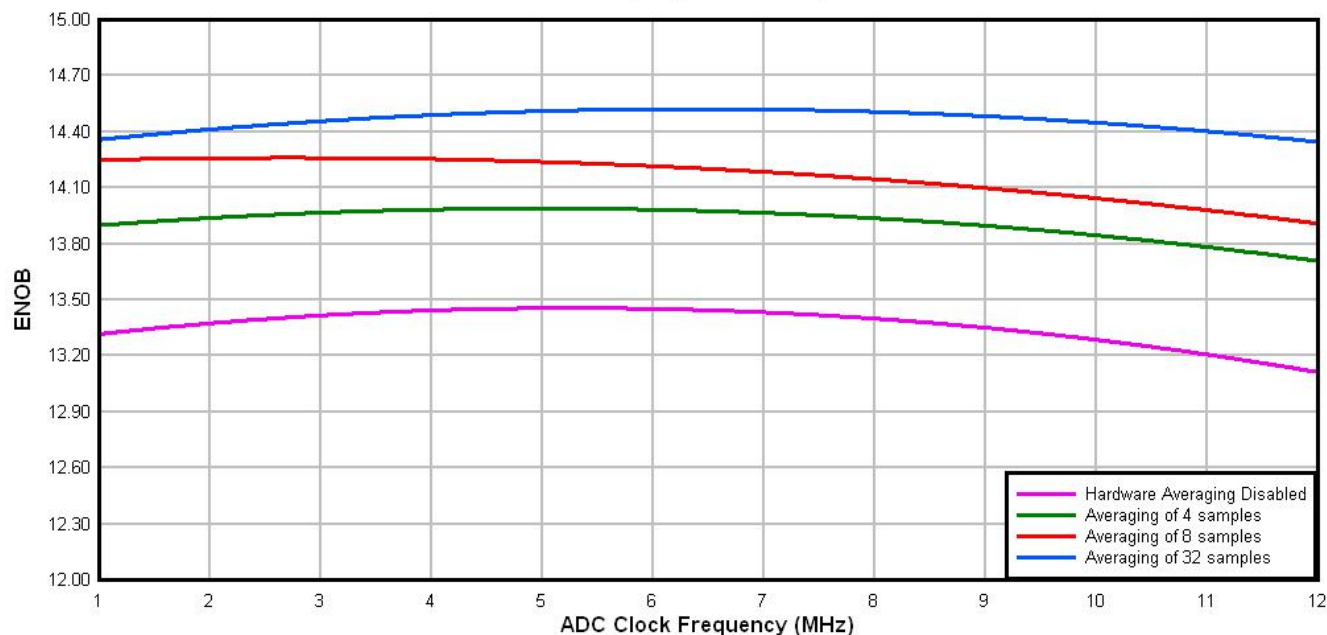

Figure 15. Typical ENOB vs. ADC_CLK for 16-bit differential mode

Table 28. 16-bit ADC with PGA operating conditions (continued)

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
C _{rate}	ADC conversion rate	≤ 13 bit modes No ADC hardware averaging Continuous conversions enabled Peripheral clock = 50 MHz	18.484	—	450	Ksps	7
		16 bit modes No ADC hardware averaging Continuous conversions enabled Peripheral clock = 50 MHz	37.037	—	250	Ksps	8

1. Typical values assume V_{DDA} = 3.0 V, Temp = 25°C, f_{ADCK} = 6 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. ADC must be configured to use the internal voltage reference (VREF_OUT)
3. PGA reference is internally connected to the VREF_OUT pin. If the user wishes to drive VREF_OUT with a voltage other than the output of the VREF module, the VREF module must be disabled.
4. For single ended configurations the input impedance of the driven input is R_{PGAD}/2
5. The analog source resistance (R_{AS}), external to MCU, should be kept as minimum as possible. Increased R_{AS} causes drop in PGA gain without affecting other performances. This is not dependent on ADC clock frequency.
6. The minimum sampling time is dependent on input signal frequency and ADC mode of operation. A minimum of 1.25μs time should be allowed for F_{in}=4 kHz at 16-bit differential mode. Recommended ADC setting is: ADLSMP=1, ADLSTS=2 at 8 MHz ADC clock.
7. ADC clock = 18 MHz, ADLSMP = 1, ADLST = 00, ADHSC = 1
8. ADC clock = 12 MHz, ADLSMP = 1, ADLST = 01, ADHSC = 1

6.6.1.4 16-bit ADC with PGA characteristics with Chop enabled (ADC_PGA[PGACHPb] =0)

Table 29. 16-bit ADC with PGA characteristics

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
I _{DDA_PGA}	Supply current	Low power (ADC_PGA[PGALPb]=0)	—	420	644	μA	2
I _{DC_PGA}	Input DC current		$\frac{2}{R_{PGAD}} \left(\frac{(V_{REFPGA} \times 0.583) - V_{CM}}{(Gain+1)} \right)$			A	3
		Gain =1, V _{REFPGA} =1.2V, V _{CM} =0.5V	—	1.54	—	μA	
		Gain =64, V _{REFPGA} =1.2V, V _{CM} =0.1V	—	0.57	—	μA	

Table continues on the next page...

Table 29. 16-bit ADC with PGA characteristics (continued)

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
SFDR	Spurious free dynamic range	- Gain=1 - Gain=64	85 53	105 88	— —	dB dB	16-bit differential mode, Average=32, $f_{in}=100\text{Hz}$
ENOB	Effective number of bits	- Gain=1, Average=4 - Gain=64, Average=4 - Gain=1, Average=32 - Gain=2, Average=32 - Gain=4, Average=32 - Gain=8, Average=32 - Gain=16, Average=32 - Gain=32, Average=32 - Gain=64, Average=32	11.6 7.2 12.8 11.0 7.9 7.3 6.8 6.8 7.5	13.4 9.6 14.5 14.3 13.8 13.1 12.5 11.5 10.6	— — — — — — — — —	bits bits bits bits bits bits bits bits bits	16-bit differential mode, $f_{in}=100\text{Hz}$
SINAD	Signal-to-noise plus distortion ratio	See ENOB	$6.02 \times \text{ENOB} + 1.76$			dB	

- Typical values assume $V_{DDA}=3.0\text{V}$, $\text{Temp}=25^{\circ}\text{C}$, $f_{ADCK}=6\text{MHz}$ unless otherwise stated.
- This current is a PGA module adder, in addition to ADC conversion currents.
- Between $\text{IN}+$ and $\text{IN}-$. The PGA draws a DC current from the input terminals. The magnitude of the DC current is a strong function of input common mode voltage (V_{CM}) and the PGA gain.
- Gain = 2^{PGAG}
- After changing the PGA gain setting, a minimum of 2 ADC+PGA conversions should be ignored.
- Limit the input signal swing so that the PGA does not saturate during operation. Input signal swing is dependent on the PGA reference voltage and gain setting.

6.6.2 CMP and 6-bit DAC electrical specifications

Table 30. Comparator and 6-bit DAC electrical specifications

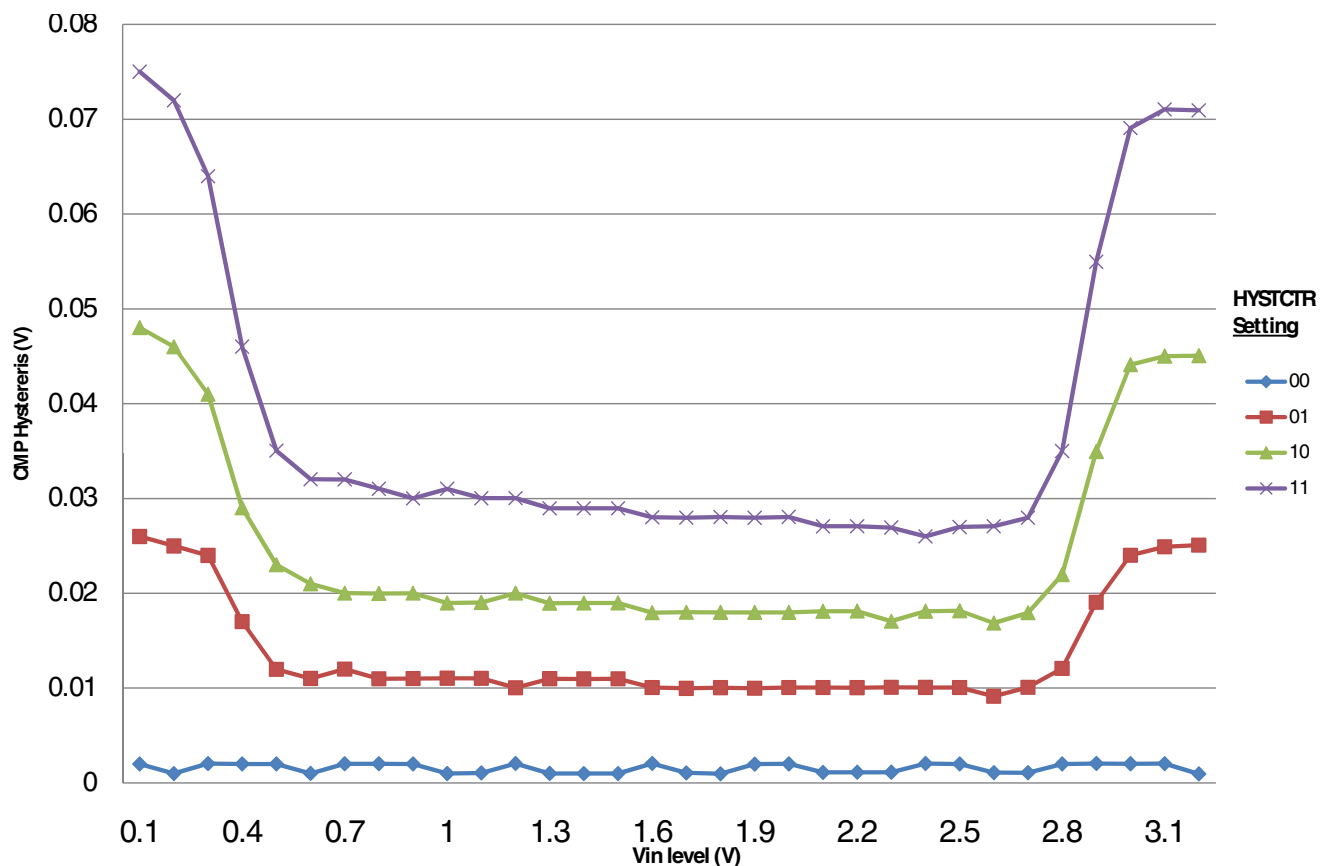
Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	1.71	—	3.6	V
I_{DDHS}	Supply current, High-speed mode ($\text{EN}=1$, $\text{PMODE}=1$)	—	—	200	μA
$I_{DDL S}$	Supply current, low-speed mode ($\text{EN}=1$, $\text{PMODE}=0$)	—	—	20	μA
V_{AIN}	Analog input voltage	$V_{SS} - 0.3$	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV
V_H	Analog comparator hysteresis ¹ $\text{CR0}[\text{HYSTCTR}] = 00$ $\text{CR0}[\text{HYSTCTR}] = 01$ $\text{CR0}[\text{HYSTCTR}] = 10$ $\text{CR0}[\text{HYSTCTR}] = 11$	— — — —	5 10 20 30	— — — —	mV mV mV mV

Table continues on the next page...

Table 30. Comparator and 6-bit DAC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
V_{CMPOH}	Output high	$V_{DD} - 0.5$	—	—	V
V_{CMPOI}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay ²	—	—	40	μ s
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	μ A
INL	6-bit DAC integral non-linearity	-0.5	—	0.5	LSB ³
DNL	6-bit DAC differential non-linearity	-0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.6 to $V_{DD}-0.6V$.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}/64$


Figure 17. Typical hysteresis vs. Vin level (VDD=3.3V, PMODE=0)

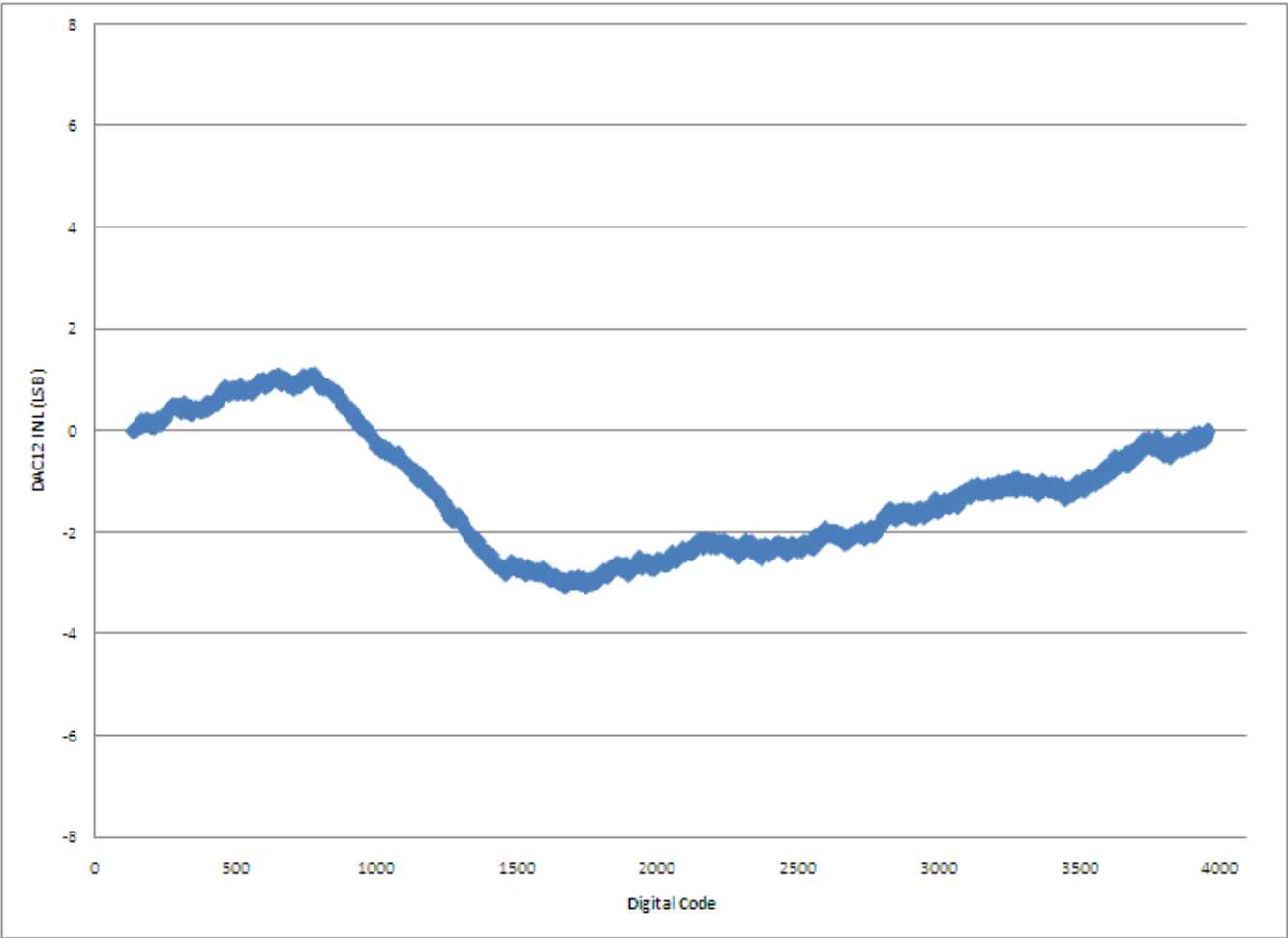


Figure 19. Typical INL error vs. digital code

Table 41. I2S/SAI master mode timing in Normal Run, Wait and Stop modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	40	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	80	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	15	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	-1.0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	15	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	20.5	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

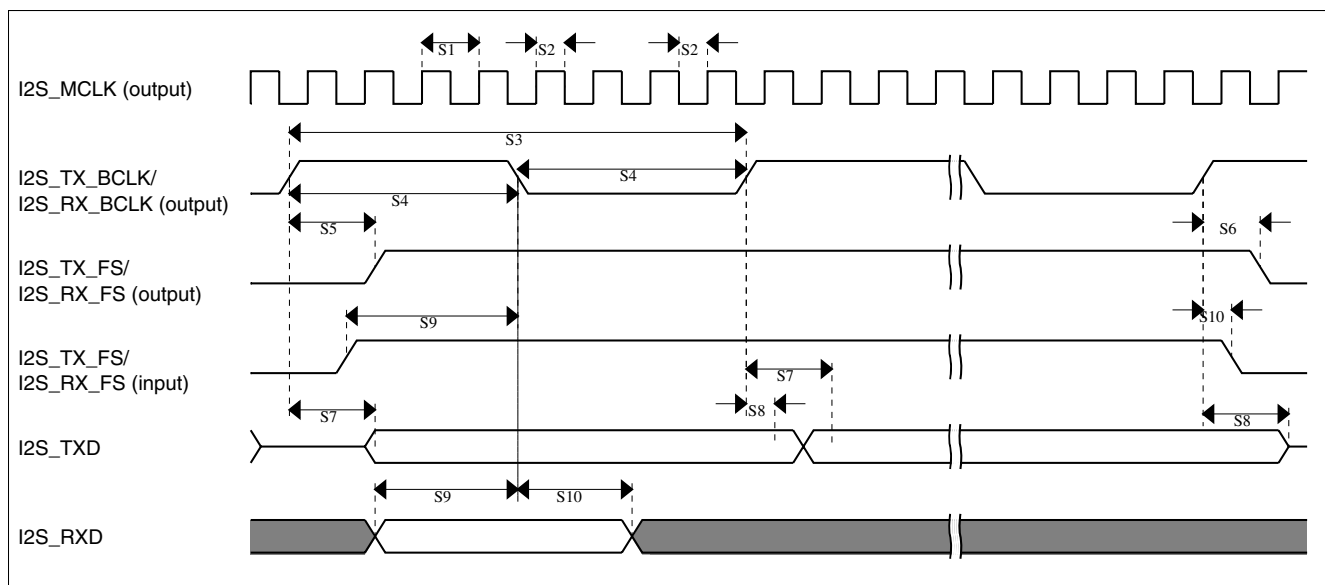


Figure 25. I2S/SAI timing — master modes

Table 42. I2S/SAI slave mode timing in Normal Run, Wait and Stop modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	80	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period

Table continues on the next page...

80 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
46	PTB3	ADC0_SE13/ TSI0_CH8	ADC0_SE13/ TSI0_CH8	PTB3	I2C0_SDA	UART0_CTS_ b/ UART0_COL_b			FTM0_FLT0		
47	PTB10	ADC1_SE14	ADC1_SE14	PTB10	SPI1_PCS0	UART3_RX		FB_AD19	FTM0_FLT1		
48	PTB11	ADC1_SE15	ADC1_SE15	PTB11	SPI1_SCK	UART3_TX		FB_AD18	FTM0_FLT2		
49	VSS	VSS	VSS								
50	VDD	VDD	VDD								
51	PTB16	TSI0_CH9	TSI0_CH9	PTB16	SPI1_SOUT	UART0_RX		FB_AD17	EWM_IN		
52	PTB17	TSI0_CH10	TSI0_CH10	PTB17	SPI1_SIN	UART0_TX		FB_AD16	EWM_OUT_b		
53	PTB18	TSI0_CH11	TSI0_CH11	PTB18	CAN0_TX	FTM2_CH0	I2S0_TX_BCLK	FB_AD15	FTM2_QD_ PHA		
54	PTB19	TSI0_CH12	TSI0_CH12	PTB19	CAN0_RX	FTM2_CH1	I2S0_TX_FS	FB_OE_b	FTM2_QD_ PHB		
55	PTC0	ADC0_SE14/ TSI0_CH13	ADC0_SE14/ TSI0_CH13	PTC0	SPI0_PCS4	PDB0_EXTRG		FB_AD14	I2S0_TXD1		
56	PTC1/ LLWU_P6	ADC0_SE15/ TSI0_CH14	ADC0_SE15/ TSI0_CH14	PTC1/ LLWU_P6	SPI0_PCS3	UART1_RTS_b	FTM0_CH0	FB_AD13	I2S0_TXD0		
57	PTC2	ADC0_SE4b/ CMP1_IN0/ TSI0_CH15	ADC0_SE4b/ CMP1_IN0/ TSI0_CH15	PTC2	SPI0_PCS2	UART1_CTS_b	FTM0_CH1	FB_AD12	I2S0_TX_FS		
58	PTC3/ LLWU_P7	CMP1_IN1	CMP1_IN1	PTC3/ LLWU_P7	SPI0_PCS1	UART1_RX	FTM0_CH2	CLKOUT	I2S0_TX_BCLK		
59	VSS	VSS	VSS								
60	VDD	VDD	VDD								
61	PTC4/ LLWU_P8	DISABLED		PTC4/ LLWU_P8	SPI0_PCS0	UART1_TX	FTM0_CH3	FB_AD11	CMP1_OUT		
62	PTC5/ LLWU_P9	DISABLED		PTC5/ LLWU_P9	SPI0_SCK	LPTMR0_ALT2	I2S0_RXD0	FB_AD10	CMP0_OUT		
63	PTC6/ LLWU_P10	CMP0_IN0	CMP0_IN0	PTC6/ LLWU_P10	SPI0_SOUT	PDB0_EXTRG	I2S0_RX_BCLK	FB_AD9	I2S0_MCLK		
64	PTC7	CMP0_IN1	CMP0_IN1	PTC7	SPI0_SIN		I2S0_RX_FS	FB_AD8			
65	PTC8	ADC1_SE4b/ CMP0_IN2	ADC1_SE4b/ CMP0_IN2	PTC8			I2S0_MCLK	FB_AD7			
66	PTC9	ADC1_SE5b/ CMP0_IN3	ADC1_SE5b/ CMP0_IN3	PTC9			I2S0_RX_BCLK	FB_AD6	FTM2_FLT0		
67	PTC10	ADC1_SE6b	ADC1_SE6b	PTC10	I2C1_SCL		I2S0_RX_FS	FB_AD5			
68	PTC11/ LLWU_P11	ADC1_SE7b	ADC1_SE7b	PTC11/ LLWU_P11	I2C1_SDA		I2S0_RXD1	FB_RW_b			
69	VSS	VSS	VSS								
70	VDD	VDD	VDD								
71	PTC16	DISABLED		PTC16		UART3_RX		FB_CS5_b/ FB_TSI21/ FB_BE23_16_b			
72	PTC17	DISABLED		PTC17		UART3_TX		FB_CS4_b/ FB_TSI20/ FB_BE31_24_b			