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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, EBI/EMI, I ² C, IrDA, SPI, UART/USART
Peripherals	DMA, I ² S, LVD, POR, PWM, WDT
Number of I/O	56
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	16К х 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 31x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mk10dx64vlk7r

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong





1 Ordering parts

1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to www.freescale.com and perform a part number search for the following device numbers: PK10 and MK10.

2 Part identification

2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

2.2 Format

Part numbers for this device have the following format:

Q K## A M FFF R T PP CC N

2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	 M = Fully qualified, general market flow P = Prequalification
K##	Kinetis family	• K10
A	Key attribute	 D = Cortex-M4 w/ DSP F = Cortex-M4 w/ DSP and FPU
Μ	Flash memory type	 N = Program flash only X = Program flash and FlexMemory



reminology and guidelines

Field	Description	Values
FFF	Program flash memory size	 32 = 32 KB 64 = 64 KB 128 = 128 KB 256 = 256 KB 512 = 512 KB 1M0 = 1 MB
R	Silicon revision	 Z = Initial (Blank) = Main A = Revision after main
Т	Temperature range (°C)	 V = -40 to 105 C = -40 to 85
PP	Package identifier	 FM = 32 QFN (5 mm x 5 mm) FT = 48 QFN (7 mm x 7 mm) LF = 48 LQFP (7 mm x 7 mm) LH = 64 LQFP (10 mm x 10 mm) MP = 64 MAPBGA (5 mm x 5 mm) LK = 80 LQFP (12 mm x 12 mm) LL = 100 LQFP (14 mm x 14 mm) MC = 121 MAPBGA (8 mm x 8 mm) LQ = 144 LQFP (20 mm x 20 mm) MD = 144 MAPBGA (13 mm x 13 mm) MJ = 256 MAPBGA (17 mm x 17 mm)
СС	Maximum CPU frequency (MHz)	 5 = 50 MHz 7 = 72 MHz 10 = 100 MHz 12 = 120 MHz 15 = 150 MHz
N	Packaging type	 R = Tape and reel (Blank) = Trays

2.4 Example

This is an example part number:

MK10DN512ZVMD10

3 Terminology and guidelines

3.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.



Symbol	Description	Min.	Max.	Unit
I _{DD}	Digital supply current	—	185	mA
V _{DIO}	Digital input voltage (except RESET, EXTAL, and XTAL)	-0.3	5.5	V
V _{AIO}	Analog ¹ , RESET, EXTAL, and XTAL input voltage	-0.3	V _{DD} + 0.3	V
I _D	Maximum current single pin limit (applies to all digital pins)	-25	25	mA
V _{DDA}	Analog supply voltage	V _{DD} – 0.3	V _{DD} + 0.3	V
V _{BAT}	RTC battery supply voltage	-0.3	3.8	V

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

5 General

5.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is $V_{IL} + (V_{IH} - V_{IL})/2$.

Figure 1. Input signal measurement reference

All digital I/O switching characteristics assume:

- 1. output pins
 - have $C_L=30$ pF loads,
 - are configured for fast slew rate (PORTx_PCRn[SRE]=0), and
 - are configured for high drive strength (PORTx_PCRn[DSE]=1)
- 2. input pins
 - have their passive filter disabled (PORTx_PCRn[PFE]=0)

5.2 Nonswitching electrical specifications



General

5.2.2 LVD and POR operating requirements

 Table 2.
 V_{DD} supply LVD and POR operating requirements

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
V _{POR}	Falling VDD POR detect voltage	0.8	1.1	1.5	V	
V _{LVDH}	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
	Low-voltage warning thresholds — high range					1
V _{LVW1H}	Level 1 falling (LVWV=00)	2.62	2.70	2.78	V	
V _{LVW2H}	Level 2 falling (LVWV=01)	2.72	2.80	2.88	V	
V _{LVW3H}	Level 3 falling (LVWV=10)	2.82	2.90	2.98	V	
V _{LVW4H}	Level 4 falling (LVWV=11)	2.92	3.00	3.08	V	
V _{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	±80	_	mV	
V _{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
	Low-voltage warning thresholds — low range					1
V _{LVW1L}	Level 1 falling (LVWV=00)	1.74	1.80	1.86	V	
V _{LVW2L}	Level 2 falling (LVWV=01)	1.84	1.90	1.96	V	
V _{LVW3L}	Level 3 falling (LVWV=10)	1.94	2.00	2.06	V	
V _{LVW4L}	Level 4 falling (LVWV=11)	2.04	2.10	2.16	V	
V _{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	±60	_	mV	
V _{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	
t _{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	μs	

1. Rising thresholds are falling threshold + hysteresis voltage

Table 3. VBAT power operating requirements

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
V _{POR_VBAT}	Falling VBAT supply POR detect voltage	0.8	1.1	1.5	V	



5.2.3	Voltage and current operating behaviors
	Table 4. Voltage and current operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V _{OH}	Output high voltage — high drive strength				
	• 2.7 V \leq V _{DD} \leq 3.6 V, I _{OH} = -9mA	V _{DD} – 0.5	_	V	
	• $1.71 \text{ V} \le \text{V}_{\text{DD}} \le 2.7 \text{ V}, \text{ I}_{\text{OH}} = -3\text{mA}$	V _{DD} – 0.5	_	V	
	Output high voltage — low drive strength				
	• 2.7 V \leq V _{DD} \leq 3.6 V, I _{OH} = -2mA	V _{DD} – 0.5	_	V	
	• $1.71 \text{ V} \le \text{V}_{\text{DD}} \le 2.7 \text{ V}, \text{ I}_{\text{OH}} = -0.6 \text{mA}$	V _{DD} – 0.5	_	V	
I _{OHT}	Output high current total for all ports	_	100	mA	
V _{OL}	Output low voltage — high drive strength				
	• 2.7 V \leq V _{DD} \leq 3.6 V, I _{OL} = 9mA	_	0.5	V	
	• $1.71 \text{ V} \le \text{V}_{\text{DD}} \le 2.7 \text{ V}, \text{ I}_{\text{OL}} = 3\text{mA}$	—	0.5	V	
	Output low voltage — low drive strength				
	• 2.7 V \leq V _{DD} \leq 3.6 V, I _{OL} = 2mA	_	0.5	V	
	• $1.71 \text{ V} \le \text{V}_{\text{DD}} \le 2.7 \text{ V}, \text{ I}_{\text{OL}} = 0.6 \text{mA}$	_	0.5	V	
I _{OLT}	Output low current total for all ports	_	100	mA	
I _{IN}	Input leakage current (per pin) for full temperature range	-	1	μA	1
l _{IN}	Input leakage current (per pin) at 25°C	_	0.025	μA	1
I _{OZ}	Hi-Z (off-state) leakage current (per pin)	_	1	μA	
R _{PU}	Internal pullup resistors	20	50	kΩ	2
R _{PD}	Internal pulldown resistors	20	50	kΩ	3

1. Measured at VDD=3.6V

2. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{SS}

3. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{DD}

5.2.4 Power mode transition operating behaviors

All specifications except t_{POR} , and VLLSx \rightarrow RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 72 MHz
- Bus clock = 36 MHz
- FlexBus clock = 36 MHz
- Flash clock = 24 MHz



General

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
I _{DD_VBAT}	Average current when CPU is not accessing RTC registers					10
	• @ 1.8V					
	● @ -40 to 25°C	_	0.57	0.67	μA	
	• @ 70°C	_	0.90	1.2	μΑ	
	• @ 105°C	_	2.4	3.5	μA	
	• @ 3.0V					
	• @ –40 to 25°C	_	0.67	0.94	μA	
	• @ 70°C		1.0	1.4	μA	
	• @ 105°C	_	2.7	3.9	μA	

 Table 6. Power consumption operating behaviors (continued)

- 1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
- 2. 72MHz core and system clock, 36MHz bus and FlexBus clock, and 24MHz flash clock. MCG configured for FEE mode. All peripheral clocks disabled.
- 3. 72MHz core and system clock, 36MHz bus and FlexBus clock, and 24MHz flash clock. MCG configured for FEE mode. All peripheral clocks enabled.
- 4. Max values are measured with CPU executing DSP instructions.
- 5. 25MHz core, system, bus, FlexBus and flash clock. MCG configured for FEI mode.
- 6. 4 MHz core and system clock, 4 MHz FlexBus and bus clock, and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing from flash.
- 7. 4 MHz core and system clock, 4 MHz FlexBus and bus clock, and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks enabled but peripherals are not in active operation. Code executing from flash.
- 8. 4 MHz core and system clock, 4 MHz FlexBus and bus clock, and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled.
- 9. Data reflects devices with 128 KB of RAM.
- 10. Includes 32kHz oscillator current and RTC operation.

5.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE mode for 50 MHz and lower frequencies. MCG in FEE mode at greater than 50 MHz frequencies.
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFL



6.1 Core modules

6.1.1 Debug trace timing specifications Table 11. Debug trace operating behaviors

Symbol	Description	Min.	Max.	Unit
T _{cyc}	Clock period	Frequency	MHz	
T _{wl}	Low pulse width	2	—	ns
T _{wh}	High pulse width	2	_	ns
Tr	Clock and data rise time	—	3	ns
T _f	Clock and data fall time	—	3	ns
T _s	Data setup	3	—	ns
T _h	Data hold	2	—	ns



Figure 4. TRACE_CLKOUT specifications



Figure 5. Trace data specifications

6.1.2 JTAG electricals

Table 12. JTAG limited voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V

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6.3.1 MCG specifications Table 14. MCG specifications

Symbol	Description		Min.	Тур.	Max.	Unit	Notes
f _{ints_ft}	Internal reference factory trimmed at	frequency (slow clock) — nominal VDD and 25 °C	_	32.768	—	kHz	
f _{ints_t}	Internal reference trimmed	frequency (slow clock) — user	31.25	_	39.0625	kHz	
Δ _{fdco_res_t}	Resolution of trimr frequency at fixed using SCTRIM and	ned average DCO output voltage and temperature — d SCFTRIM	_	± 0.3	± 0.6	%f _{dco}	1
$\Delta f_{dco_res_t}$	Resolution of trimr frequency at fixed using SCTRIM onl	ned average DCO output voltage and temperature — y	_	± 0.2	± 0.5	%f _{dco}	1
Δf _{dco_t}	Total deviation of t frequency over vo	—	+0.5/-0.7	_	%f _{dco}	1	
∆f _{dco_t}	Total deviation of t frequency over fixe range of 0–70°C	_	± 0.3	± 0.3	%f _{dco}	1	
f _{intf_ft}	Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C			4	_	MHz	
f _{intf_t}	Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C		3	_	5	MHz	
f _{loc_low}	Loss of external clock minimum frequency — RANGE = 00		(3/5) x f _{ints_t}	_		kHz	
f _{loc_high}	Loss of external clock minimum frequency — RANGE = 01, 10, or 11		(16/5) x f _{ints_t}	_		kHz	
		FI	LL				
f _{fll_ref}	FLL reference free	luency range	31.25	—	39.0625	kHz	
f _{dco}	DCO output frequency range	Low range (DRS=00) 640 × f _{fll ref}	20	20.97	25	MHz	2, 3
		Mid range (DRS=01) 1280 × f _{fll_ref}	40	41.94	50	MHz	
		Mid-high range (DRS=10) 1920 × f _{fll_ref}	60	62.91	75	MHz	
		High range (DRS=11) 2560 × f _{fll ref}	80	83.89	100	MHz	
f _{dco_t_DMX32}	DCO output frequency	Low range (DRS=00) 732 × f _{fll ref}	_	23.99		MHz	4, 5
		Mid range (DRS=01) 1464 × f _{fll_ref}		47.97		MHz	
		Mid-high range (DRS=10) 2197 × f _{fll ref}	—	71.99	—	MHz	
		High range (DRS=11) 2929 × f _{fll_ref}	_	95.98	—	MHz	

Table continues on the next page...

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Symbol	Description	Min.	Тур.	Max.	Unit	Notes
J _{cyc_fll}	FLL period jitter	_	180	_	ps	
	 f_{VCO} = 48 MHz f_{VCO} = 98 MHz 	_	150	_		
t _{fll_acquire}	FLL target frequency acquisition time	_	_	1	ms	6
	PI	L				
f _{vco}	VCO operating frequency	48.0	—	100	MHz	
I _{pll}	PLL operating current • PLL @ 96 MHz (f _{osc_hi_1} = 8 MHz, f _{pll_ref} = 2 MHz, VDIV multiplier = 48)	_	1060	_	μA	7
I _{pll}	PLL operating current • PLL @ 48 MHz (f _{osc_hi_1} = 8 MHz, f _{pll_ref} = 2 MHz, VDIV multiplier = 24)	_	600	_	μA	7
f _{pll_ref}	PLL reference frequency range	2.0	—	4.0	MHz	
J _{cyc_pll}	PLL period jitter (RMS)					8
	• f _{vco} = 48 MHz	_	120	_	ps	
	• f _{vco} = 100 MHz	_	50	—	ps	
J _{acc_pll}	PLL accumulated jitter over 1µs (RMS)					8
	• f _{vco} = 48 MHz	_	1350	—	ps	
	• f _{vco} = 100 MHz	_	600	—	ps	
D _{lock}	Lock entry frequency tolerance	± 1.49	—	± 2.98	%	
D _{unl}	Lock exit frequency tolerance	± 4.47	—	± 5.97	%	
t _{pll_lock}	Lock detector detection time	_	_	150 × 10 ⁻⁶ + 1075(1/ f _{pll_ref})	S	9

Table 14. MCG specifications (continued)

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).

- 2. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
- The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation
 (Δf_{dco t}) over voltage and temperature should be considered.
- 4. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
- 5. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
- 6. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
- 7. Excludes any oscillator currents that are also consuming power while PLL is in operation.
- 8. This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
- This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

6.3.2 Oscillator electrical specifications

This section provides the electrical characteristics of the module.

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4. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

NOTE

The 32 kHz oscillator works in low power mode by default and cannot be moved into high power/gain mode.

6.3.3 32 kHz Oscillator Electrical Characteristics

This section describes the module electrical characteristics.

6.3.3.1 32 kHz oscillator DC electrical specifications Table 17. 32kHz oscillator DC electrical specifications

Symbol	Description	Min.	Тур.	Max.	Unit
V _{BAT}	Supply voltage	1.71	—	3.6	V
R _F	Internal feedback resistor	_	100	_	MΩ
C _{para}	Parasitical capacitance of EXTAL32 and XTAL32	_	5	7	pF
V _{pp} ¹	Peak-to-peak amplitude of oscillation	_	0.6	_	V

1. When a crystal is being used with the 32 kHz oscillator, the EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

6.3.3.2 32kHz oscillator frequency specifications Table 18. 32kHz oscillator frequency specifications

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
f _{osc_lo}	Oscillator crystal	—	32.768	—	kHz	
t _{start}	Crystal start-up time	_	1000	_	ms	1
V _{ec_extal32}	Externally provided input clock amplitude	700	_	V _{BAT}	mV	2, 3

1. Proper PC board layout procedures must be followed to achieve specifications.

2. This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.

3. The parameter specified is a peak-to-peak value and V_{IH} and V_{IL} specifications do not apply. The voltage of the applied clock must be within the range of V_{SS} to V_{BAT} .

6.4 Memories and memory interfaces

6.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.



Peripheral operating requirements and behaviors



Figure 10. EEPROM backup writes to FlexRAM

6.4.2 EzPort Switching Specifications Table 23. EzPort switching specifications

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
EP1	EZP_CK frequency of operation (all commands except READ)	—	f _{SYS} /2	MHz
EP1a	EZP_CK frequency of operation (READ command)	—	f _{SYS} /8	MHz
EP2	EZP_CS negation to next EZP_CS assertion	2 x t _{EZP_CK}		ns
EP3	EZP_CS input valid to EZP_CK high (setup)	5		ns
EP4	EZP_CK high to EZP_CS input invalid (hold)	5		ns
EP5	EZP_D input valid to EZP_CK high (setup)	2		ns
EP6	EZP_CK high to EZP_D input invalid (hold)	5		ns
EP7	EZP_CK low to EZP_Q output valid	—	16	ns
EP8	EZP_CK low to EZP_Q output invalid (hold)	0	_	ns
EP9	EZP_CS negation to EZP_Q tri-state	—	12	ns



Figure 11. EzPort Timing Diagram

6.4.3 Flexbus Switching Specifications

All processor bus timings are synchronous; input setup/hold and output delay are given in respect to the rising edge of a reference clock, FB_CLK. The FB_CLK frequency may be the same as the internal system bus frequency or an integer divider of that frequency.

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the Flexbus output clock (FB_CLK). All other timing relationships can be derived from these values.

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	_	FB_CLK	MHz	
FB1	Clock period	20	—	ns	
FB2	Address, data, and control output valid	—	11.5	ns	1
FB3	Address, data, and control output hold	0.5	_	ns	1
FB4	Data and FB_TA input setup	8.5	_	ns	2
FB5	Data and FB_TA input hold	0.5	_	ns	2

Table 24. Flexbus limited voltage range switching specifications

1. Specification is valid for all FB_AD[31:0], FB_BE/BWEn, FB_CSn, FB_OE, FB_R/W, FB_TBST, FB_TSIZ[1:0], FB_ALE, and FB_TS.



Table 27.	16-bit ADC characteristics	$(V_{REFH} = V_{DE})$	DA, V _{REFL} =	V _{SSA}) (continued)
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Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
EıL	Input leakage error			I _{In} × R _{AS}		mV	I _{In} = leakage current (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	_	1.715		mV/°C	
V _{TEMP25}	Temp sensor voltage	25 °C	_	719	_	mV	

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH} = V_{DDA}$

- Typical values assume V_{DDA} = 3.0 V, Temp = 25°C, f_{ADCK} = 2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
- The ADC supply current depends on the ADC conversion clock speed, conversion rate and the ADLPC bit (low power). For lowest power operation the ADLPC bit must be set, the HSC bit must be clear with 1 MHz ADC conversion clock speed.
- 4. 1 LSB = $(V_{REFH} V_{REFL})/2^N$
- 5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
- 6. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
- 7. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.













Typical ADC 16-bit Single-Ended ENOB vs ADC Clock 100Hz, 90% FS Sine Input



6.6.1.3 16-bit ADC with PGA operating conditions Table 28. 16-bit ADC with PGA operating conditions

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
V _{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	
V _{REFPGA}	PGA ref voltage		VREF_OU T	VREF_OU T	VREF_OU T	V	2, 3
V _{ADIN}	Input voltage		V _{SSA}	—	V _{DDA}	V	
V _{CM}	Input Common Mode range		V _{SSA}	_	V _{DDA}	V	
R _{PGAD}	Differential input	Gain = 1, 2, 4, 8	—	128	—	kΩ	IN+ to IN- ⁴
	impedance	Gain = 16, 32	_	64	—		
		Gain = 64	_	32	—		
R _{AS}	Analog source resistance		_	100	_	Ω	5
T _S	ADC sampling time		1.25	_	_	μs	6



Peripheral operating requirements and behaviors

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
C _{rate}	ADC conversion	≤ 13 bit modes	18.484	—	450	Ksps	7
	rate	No ADC hardware averaging					
		Continuous conversions enabled					
		Peripheral clock = 50 MHz					
		16 bit modes	37.037	—	250	Ksps	8
		No ADC hardware averaging					
		Continuous conversions enabled					
		Peripheral clock = 50 MHz					

Table 28. 16-bit ADC with PGA operating conditions (continued)

- 1. Typical values assume V_{DDA} = 3.0 V, Temp = 25°C, f_{ADCK} = 6 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
- 2. ADC must be configured to use the internal voltage reference (VREF_OUT)
- 3. PGA reference is internally connected to the VREF_OUT pin. If the user wishes to drive VREF_OUT with a voltage other than the output of the VREF module, the VREF module must be disabled.
- 4. For single ended configurations the input impedance of the driven input is R_{PGAD}/2
- 5. The analog source resistance (R_{AS}), external to MCU, should be kept as minimum as possible. Increased R_{AS} causes drop in PGA gain without affecting other performances. This is not dependent on ADC clock frequency.
- 6. The minimum sampling time is dependent on input signal frequency and ADC mode of operation. A minimum of 1.25µs time should be allowed for Fin=4 kHz at 16-bit differential mode. Recommended ADC setting is: ADLSMP=1, ADLSTS=2 at 8 MHz ADC clock.
- 7. ADC clock = 18 MHz, ADLSMP = 1, ADLST = 00, ADHSC = 1
- 8. ADC clock = 12 MHz, ADLSMP = 1, ADLST = 01, ADHSC = 1

6.6.1.4 16-bit ADC with PGA characteristics with Chop enabled (ADC PGA[PGACHPb] =0)

Table 29. 16-bit ADC with PGA characteristics

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
I _{DDA_PGA}	Supply current	Low power (ADC_PGA[PGALPb]=0)	_	420	644	μA	2
I _{DC_PGA}	Input DC current		$\frac{2}{R_{\rm PGAD}} \left(\frac{(V_{\rm REFPGA} \times 0.583) - V_{\rm CM}}{({\rm Gain}+1)} \right)$			A	3
		Gain =1, V_{REFPGA} =1.2V, V_{CM} =0.5V	_	1.54	_	μA	
		Gain =64, V_{REFPGA} =1.2V, V_{CM} =0.1V		0.57	_	μA	



3. 1 LSB = V_{reference}/64

Symbol	Description	Min.	Тур.	Max.	Unit
V _{CMPOh}	Output high	V _{DD} – 0.5	_	—	V
V _{CMPOI}	Output low		_	0.5	V
t _{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
t _{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay ²	_	_	40	μs
I _{DAC6b}	6-bit DAC current adder (enabled)	_	7	—	μA
INL	6-bit DAC integral non-linearity	-0.5	_	0.5	LSB ³
DNL	6-bit DAC differential non-linearity	-0.3		0.3	LSB

Table 30. Comparator and 6-bit DAC electrical specifications (continued)

- 1. Typical hysteresis is measured with input voltage range limited to 0.6 to V_{DD} -0.6V.
- 2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
 - 0.08 0.07 0.06 HYSTCTR 0.05 <u>Setting</u> CMP Hystereris (V) -00 0.04 -01 **____** 10 ×11 0.03 0.02 0.01 0 1.6 1.9 Vin level (V) 0.1 0.4 0.7 1 1.3 2.2 2.5 2.8 3.1
 - Figure 17. Typical hysteresis vs. Vin level (VDD=3.3V, PMODE=0)



Symbol	Description	Min.	Тур.	Max.	Unit	Notes
V _{out}	Voltage reference output with factory trim at nominal V_{DDA} and temperature=25C	1.1915	1.195	1.1977	V	
V _{out}	Voltage reference output — factory trim	1.1584	—	1.2376	V	
V _{out}	Voltage reference output — user trim	1.193	—	1.197	V	
V _{step}	Voltage reference trim step	—	0.5	—	mV	
V _{tdrift}	Temperature drift (Vmax -Vmin across the full temperature range)	—	_	80	mV	
I _{bg}	Bandgap only current	—	—	80	μA	1
I _{lp}	Low-power buffer current	—	—	360	uA	1
I _{hp}	High-power buffer current	_	—	1	mA	1
ΔV_{LOAD}	Load regulation				μV	1, 2
	• current = ± 1.0 mA	—	200	_		
T _{stup}	Buffer startup time	—	—	100	μs	
V _{vdrift}	Voltage drift (Vmax -Vmin across the full voltage range)	_	2		mV	1

Table 34. VREF full-range operating behaviors

1. See the chip's Reference Manual for the appropriate settings of the VREF Status and Control register.

2. Load regulation voltage is the difference between the VREF_OUT voltage with no load vs. voltage with defined load

Table 35. VREF limited-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T _A	Temperature	0	50	°C	

Table 36. VREF limited-range operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V _{out}	Voltage reference output with factory trim	1.173	1.225	V	

6.7 Timers

See General switching specifications.

6.8 Communication interfaces



Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation		12.5	MHz
DS9	DSPI_SCK input cycle time	4 x t _{BUS}	_	ns
DS10	DSPI_SCK input high/low time	(t _{SCK} /2) – 2	(t _{SCK} /2) + 2	ns
DS11	DSPI_SCK to DSPI_SOUT valid		10	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	_	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	_	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	_	ns
DS15	DSPI_SS active to DSPI_SOUT driven		14	ns
DS16	DSPI_SS inactive to DSPI_SOUT not driven		14	ns

Table 38. Slave mode DSPI timing (limited voltage range)



Figure 22. DSPI classic SPI timing — slave mode

6.8.3 DSPI switching specifications (full voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	1
	Frequency of operation	—	12.5	MHz	
DS1	DSPI_SCK output cycle time	4 x t _{BUS}		ns	

Table 39. Master mode DSPI timing (full voltage range)



80 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
73	PTD0/ LLWU_P12	DISABLED		PTD0/ LLWU_P12	SPI0_PCS0	UART2_RTS_b		FB_ALE/ FB_CS1_b/ FB_TS_b			
74	PTD1	ADC0_SE5b	ADC0_SE5b	PTD1	SPI0_SCK	UART2_CTS_b		FB_CS0_b			
75	PTD2/ LLWU_P13	DISABLED		PTD2/ LLWU_P13	SPI0_SOUT	UART2_RX		FB_AD4			
76	PTD3	DISABLED		PTD3	SPI0_SIN	UART2_TX		FB_AD3			
77	PTD4/ LLWU_P14	DISABLED		PTD4/ LLWU_P14	SPI0_PCS1	UART0_RTS_b	FTM0_CH4	FB_AD2	EWM_IN		
78	PTD5	ADC0_SE6b	ADC0_SE6b	PTD5	SPI0_PCS2	UART0_CTS_ b/ UART0_COL_b	FTM0_CH5	FB_AD1	EWM_OUT_b		
79	PTD6/ LLWU_P15	ADC0_SE7b	ADC0_SE7b	PTD6/ LLWU_P15	SPI0_PCS3	UART0_RX	FTM0_CH6	FB_AD0	FTM0_FLT0		
80	PTD7	DISABLED		PTD7	CMT_IRO	UART0_TX	FTM0_CH7		FTM0_FLT1		

8.2 K10 Pinouts

The below figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.



Rev. No.	Date	Substantial Changes
1	3/2012	Initial public release
2	4/2012	 Replaced TBDs throughout. Updated "Power consumption operating behaviors" table. Updated "ADC electrical specifications" section. Updated "VREF full-range operating behaviors" table. Updated "I2S/SAI Switching Specifications" section. Updated "TSI electrical specifications" table.
3	11/2012	 Updated orderable part numbers. Updated the maximum input voltage (V_{ADIN}) specification in the "16-bit ADC operating conditions" section.