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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

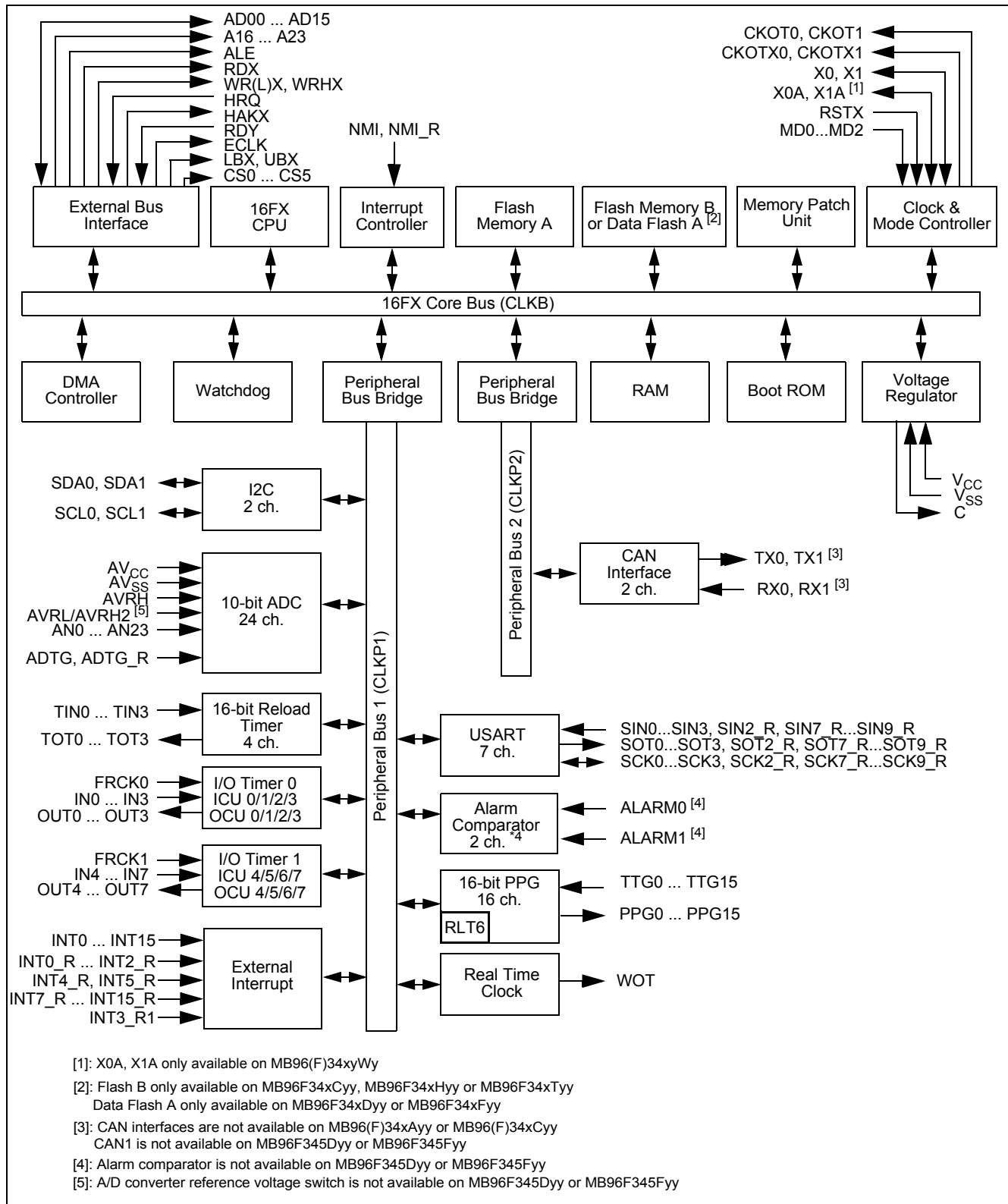
Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	F ² MC-16FX
Core Size	16-Bit
Speed	56MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, LVR, POR, PWM, WDT
Number of I/O	82
Program Memory Size	288KB (288K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f346asbpmc-gse2

2. Block Diagram

Figure 1. Block diagram of MB96(F)34x



8. User ROM Memory Map For Flash Devices

MB96F345D MB96F345F					
Alternative mode CPU address	Flash memory mode address	Flash size 160kByte +64KByte Data Flash			
FF:FFFF _H FF:0000 _H	3F:FFFF _H 3F:0000 _H	S39 - 64K	Flash A		
FE:FFFF _H FE:0000 _H	3E:FFFF _H 3E:0000 _H	S38 - 64K			
FD:FFFF _H FD:0000 _H	3D:FFFF _H 3D:0000 _H	External bus			
FC:FFFF _H FC:0000 _H	3C:FFFF _H 3C:0000 _H				
FB:FFFF _H FB:0000 _H	3B:FFFF _H 3B:0000 _H				
FA:FFFF _H FA:0000 _H	3A:FFFF _H 3A:0000 _H				
F9:FFFF _H F9:0000 _H	39:FFFF _H 39:0000 _H				
F8:FFFF _H F8:0000 _H	38:FFFF _H 38:0000 _H				
F7:FFFF _H F7:0000 _H	37:FFFF _H 37:0000 _H				
F6:FFFF _H F6:0000 _H	36:FFFF _H 36:0000 _H				
F5:FFFF _H F5:0000 _H	35:FFFF _H 35:0000 _H				
F4:FFFF _H F4:0000 _H	34:FFFF _H 34:0000 _H				
F3:FFFF _H F3:0000 _H	33:FFFF _H 33:0000 _H				
F2:FFFF _H F2:0000 _H	32:FFFF _H 32:0000 _H				
F1:FFFF _H F1:0000 _H	31:FFFF _H 31:0000 _H				
F0:FFFF _H F0:0000 _H	30:FFFF _H 30:0000 _H				
E0:FFFF _H E0:0000 _H					
DF:FFFF _H DF:8000 _H				Reserved	
DF:7FFF _H DF:6000 _H	1F:7FFF _H 1F:6000 _H			SA3 - 8K	Flash A
DF:5FFF _H DF:4000 _H	1F:5FFF _H 1F:4000 _H			SA2 - 8K	
DF:3FFF _H DF:2000 _H	1F:3FFF _H 1F:2000 _H			SA1 - 8K	
DF:1FFF _H DF:0000 _H	1F:1FFF _H 1F:0000 _H			SA0 - 8K ^[1]	
DE:FFFF _H DE:0000 _H				Reserved	
0E:FFFF _H 0E:FF00 _H	(0E:FFFF _H) (0E:FF00 _H)			SDA0-256 ^[2]	Data Flash A
0E:FEFF _H 0E:0000 _H				Reserved	
0D:FFFF _H 0D:C000 _H	(0F:FFFF _H) (0F:C000 _H)			SDA4-16K	Data Flash A
0D:BFFF _H 0D:8000 _H	(0F:BFFF _H) (0F:8000 _H)			SDA3-16K	
0D:7FFF _H 0D:4000 _H	(0F:7FFF _H) (0F:4000 _H)			SDA2-16K	
0D:3FFF _H 0D:0000 _H	(0F:3FFF _H) (0F:0000 _H)			SDA1-16K	
0C:FFFF _H 0C:0000 _H				Reserved	

[1]: Sector SA0 contains the ROM Configuration Block RCBA at CPU address DF:0000_H - DF:007F_H

[2]: Sector SDA0 contains the ROM Configuration Block RCBDA at CPU address DE:FF00_H - DE:FF2F_H

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000407 _H	PLL Control register High	PLLCRH		R/W
000408 _H	RC clock timer control register	RCTCR		R/W
000409 _H	Main clock timer control register	MCTCR		R/W
00040A _H	Sub clock timer control register	SCTCR		R/W
00040B _H	Reset cause and clock status register with clear function	RCCSRC		R
00040C _H	Reset configuration register	RCR		R/W
00040D _H	Reset cause and clock status register	RCCSR		R
00040E _H	Watch dog timer configuration register	WDTC		R/W
00040F _H	Watch dog timer clear pattern register	WDTCP		W
000410 _H -000414 _H	Reserved			-
000415 _H	Clock output activation register	COAR		R/W
000416 _H	Clock output configuration register 0	COCR0		R/W
000417 _H	Clock output configuration register 1	COCR1		R/W
000418 _H	Clock Modulator control register	CMCR		R/W
000419 _H	Reserved			-
00041A _H	Clock Modulator Parameter register Low	CMPRL	CMPR	R/W
00041B _H	Clock Modulator Parameter register High	CMPRH		R/W
00041C _H -00042B _H	Reserved			-
00042C _H	Voltage Regulator Control register	VRCR		R/W
00042D _H	Clock Input and LVD Control Register	CILCR		R/W
00042E _H -00042F _H	Reserved			-
000430 _H	I/O Port P00 - Data Direction Register	DDR00		R/W
000431 _H	I/O Port P01 - Data Direction Register	DDR01		R/W
000432 _H	I/O Port P02 - Data Direction Register	DDR02		R/W
000433 _H	I/O Port P03 - Data Direction Register	DDR03		R/W
000434 _H	I/O Port P04 - Data Direction Register	DDR04		R/W
000435 _H	I/O Port P05 - Data Direction Register	DDR05		R/W
000436 _H	I/O Port P06 - Data Direction Register	DDR06		R/W
000437 _H	I/O Port P07 - Data Direction Register	DDR07		R/W
000438 _H	I/O Port P08 - Data Direction Register	DDR08		R/W
000439 _H	I/O Port P09 - Data Direction Register	DDR09		R/W
00043A _H	I/O Port P10 - Data Direction Register	DDR10		R/W

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00043B _H -000443 _H	Reserved			-
000444 _H	I/O Port P00 - Port Input Enable Register	PIER00		R/W
000445 _H	I/O Port P01 - Port Input Enable Register	PIER01		R/W
000446 _H	I/O Port P02 - Port Input Enable Register	PIER02		R/W
000447 _H	I/O Port P03 - Port Input Enable Register	PIER03		R/W
000448 _H	I/O Port P04 - Port Input Enable Register	PIER04		R/W
000449 _H	I/O Port P05 - Port Input Enable Register	PIER05		R/W
00044A _H	I/O Port P06 - Port Input Enable Register	PIER06		R/W
00044B _H	I/O Port P07 - Port Input Enable Register	PIER07		R/W
00044C _H	I/O Port P08 - Port Input Enable Register	PIER08		R/W
00044D _H	I/O Port P09 - Port Input Enable Register	PIER09		R/W
00044E _H	I/O Port P10 - Port Input Enable Register	PIER10		R/W
00044F _H -000457 _H	Reserved			-
000458 _H	I/O Port P00 - Port Input Level Register	PILR00		R/W
000459 _H	I/O Port P01 - Port Input Level Register	PILR01		R/W
00045A _H	I/O Port P02 - Port Input Level Register	PILR02		R/W
00045B _H	I/O Port P03 - Port Input Level Register	PILR03		R/W
00045C _H	I/O Port P04 - Port Input Level Register	PILR04		R/W
00045D _H	I/O Port P05 - Port Input Level Register	PILR05		R/W
00045E _H	I/O Port P06 - Port Input Level Register	PILR06		R/W
00045F _H	I/O Port P07 - Port Input Level Register	PILR07		R/W
000460 _H	I/O Port P08 - Port Input Level Register	PILR08		R/W
000461 _H	I/O Port P09 - Port Input Level Register	PILR09		R/W
000462 _H	I/O Port P10 - Port Input Level Register	PILR10		R/W
000463 _H -00046B _H	Reserved			-
00046C _H	I/O Port P00 - Extended Port Input Level Register	EPILR00		R/W
00046D _H	I/O Port P01 - Extended Port Input Level Register	EPILR01		R/W
00046E _H	I/O Port P02 - Extended Port Input Level Register	EPILR02		R/W
00046F _H	I/O Port P03 - Extended Port Input Level Register	EPILR03		R/W
000470 _H	I/O Port P04 - Extended Port Input Level Register	EPILR04		R/W
000471 _H	I/O Port P05 - Extended Port Input Level Register	EPILR05		R/W
000472 _H	I/O Port P06 - Extended Port Input Level Register	EPILR06		R/W

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00056D _H	PPG7 - Timer register			R
00056E _H	PPG7 - Period setting register		PCSR7	W
00056F _H	PPG7 - Period setting register			W
000570 _H	PPG7 - Duty cycle register		PDUT7	W
000571 _H	PPG7 - Duty cycle register			W
000572 _H	PPG7 - Control status register Low	PCNL7	PCN7	R/W
000573 _H	PPG7 - Control status register High	PCNH7		R/W
000574 _H	PPG11-PPG8 - General Control register 1 Low	GCN1L2	GCN12	R/W
000575 _H	PPG11-PPG8 - General Control register 1 High	GCN1H2		R/W
000576 _H	PPG11-PPG8 - General Control register 2 Low	GCN2L2	GCN22	R/W
000577 _H	PPG11-PPG8 - General Control register 2 High	GCN2H2		R/W
000578 _H	PPG8 - Timer register		PTMR8	R
000579 _H	PPG8 - Timer register			R
00057A _H	PPG8 - Period setting register		PCSR8	W
00057B _H	PPG8 - Period setting register			W
00057C _H	PPG8 - Duty cycle register		PDUT8	W
00057D _H	PPG8 - Duty cycle register			W
00057E _H	PPG8 - Control status register Low	PCNL8	PCN8	R/W
00057F _H	PPG8 - Control status register High	PCNH8		R/W
000580 _H	PPG9 - Timer register		PTMR9	R
000581 _H	PPG9 - Timer register			R
000582 _H	PPG9 - Period setting register		PCSR9	W
000583 _H	PPG9 - Period setting register			W
000584 _H	PPG9 - Duty cycle register		PDUT9	W
000585 _H	PPG9 - Duty cycle register			W
000586 _H	PPG9 - Control status register Low	PCNL9	PCN9	R/W
000587 _H	PPG9 - Control status register High	PCNH9		R/W
000588 _H	PPG10 - Timer register		PTMR10	R
000589 _H	PPG10 - Timer register			R
00058A _H	PPG10 - Period setting register		PCSR10	W
00058B _H	PPG10 - Period setting register			W
00058C _H	PPG10 - Duty cycle register		PDUT10	W

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000715 _H	CAN0 - IF1 Mask 1 Register High	IF1MSK1H0		R/W
000716 _H	CAN0 - IF1 Mask 2 Register Low	IF1MSK2L0	IF1MSK20	R/W
000717 _H	CAN0 - IF1 Mask 2 Register High	IF1MSK2H0		R/W
000718 _H	CAN0 - IF1 Arbitration 1 Register Low	IF1ARB1L0	IF1ARB10	R/W
000719 _H	CAN0 - IF1 Arbitration 1 Register High	IF1ARB1H0		R/W
00071A _H	CAN0 - IF1 Arbitration 2 Register Low	IF1ARB2L0	IF1ARB20	R/W
00071B _H	CAN0 - IF1 Arbitration 2 Register High	IF1ARB2H0		R/W
00071C _H	CAN0 - IF1 Message Control Register Low	IF1MCTRL0	IF1MCTR0	R/W
00071D _H	CAN0 - IF1 Message Control Register High	IF1MCTRH0		R/W
00071E _H	CAN0 - IF1 Data A1 Low	IF1DTA1L0	IF1DTA10	R/W
00071F _H	CAN0 - IF1 Data A1 High	IF1DTA1H0		R/W
000720 _H	CAN0 - IF1 Data A2 Low	IF1DTA2L0	IF1DTA20	R/W
000721 _H	CAN0 - IF1 Data A2 High	IF1DTA2H0		R/W
000722 _H	CAN0 - IF1 Data B1 Low	IF1DTB1L0	IF1DTB10	R/W
000723 _H	CAN0 - IF1 Data B1 High	IF1DTB1H0		R/W
000724 _H	CAN0 - IF1 Data B2 Low	IF1DTB2L0	IF1DTB20	R/W
000725 _H	CAN0 - IF1 Data B2 High	IF1DTB2H0		R/W
000726 _H -00073F _H	Reserved			-
000740 _H	CAN0 - IF2 Command request register Low	IF2CREQL0	IF2CREQ0	R/W
000741 _H	CAN0 - IF2 Command request register High	IF2CREQH0		R/W
000742 _H	CAN0 - IF2 Command Mask register Low	IF2CMSKL0	IF2CMSK0	R/W
000743 _H	CAN0 - IF2 Command Mask register High (reserved)	IF2CMSKH0		R
000744 _H	CAN0 - IF2 Mask 1 Register Low	IF2MSK1L0	IF2MSK10	R/W
000745 _H	CAN0 - IF2 Mask 1 Register High	IF2MSK1H0		R/W
000746 _H	CAN0 - IF2 Mask 2 Register Low	IF2MSK2L0	IF2MSK20	R/W
000747 _H	CAN0 - IF2 Mask 2 Register High	IF2MSK2H0		R/W
000748 _H	CAN0 - IF2 Arbitration 1 Register Low	IF2ARB1L0	IF2ARB10	R/W
000749 _H	CAN0 - IF2 Arbitration 1 Register High	IF2ARB1H0		R/W
00074A _H	CAN0 - IF2 Arbitration 2 Register Low	IF2ARB2L0	IF2ARB20	R/W
00074B _H	CAN0 - IF2 Arbitration 2 Register High	IF2ARB2H0		R/W
00074C _H	CAN0 - IF2 Message Control Register Low	IF2MCTRL0	IF2MCTR0	R/W
00074D _H	CAN0 - IF2 Message Control Register High	IF2MCTRH0		R/W

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Permitted Power dissipation (Mask ROM devices) ^[4]	P_D	-	350	mW	$T_A=105^{\circ}\text{C}$
		-	360	mW	$T_A=125^{\circ}\text{C}$ [6]
Operating ambient temperature	T_A	0	+70	$^{\circ}\text{C}$	MB96V300B
		-40	+105		
		-40	+125		[6]
Storage temperature	T_{STG}	-55	+150	$^{\circ}\text{C}$	

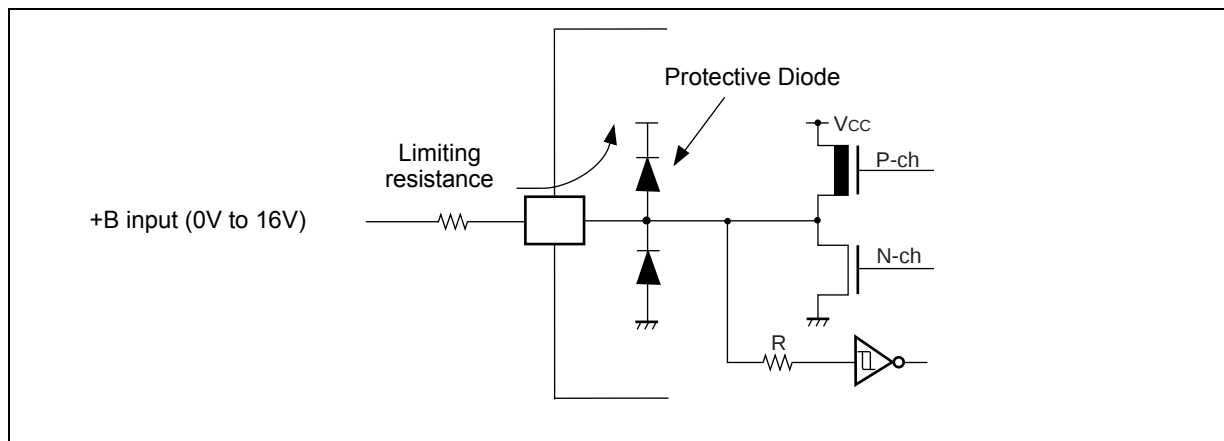
[1]: AV_{CC} and V_{CC} must be set to the same voltage. It is required that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} neither when the power is switched on.

[2]: V_I and V_O should not exceed $V_{CC} + 0.3\text{ V}$. V_I should also not exceed the specified ratings. However if the maximum current to/from a input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating. Input/output voltages of standard ports depend on V_{CC} .

[3]:

- Applicable to all general purpose I/O pins (Pnn_m)
- Use within recommended operating conditions.
- Use at DC voltage (current)
- The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the Power reset (except devices with persistent low voltage reset in internal vector mode).

Sample recommended circuits:



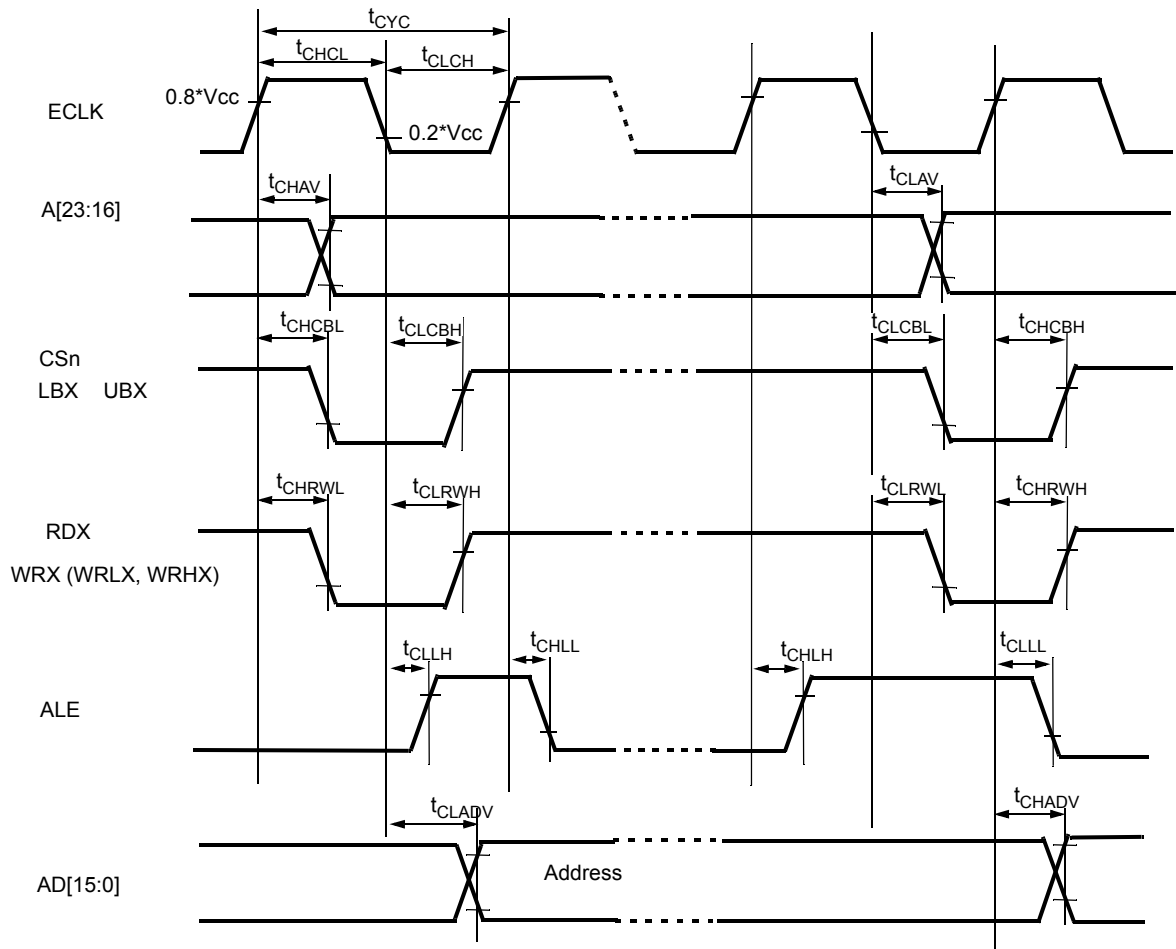
14.3 DC characteristics

($T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = 0\text{V}$)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input H voltage	V_{IH}	Port inputs Pnn_m	CMOS Hysteresis 0.8/0.2 input selected	$0.8 V_{CC}$	-	$V_{CC} + 0.3$	V	
			CMOS Hysteresis 0.7/0.3 input selected	$0.7 V_{CC}$	-	$V_{CC} + 0.3$	V	$V_{CC} \geq 4.5\text{V}$
			AUTOMOTIVE Hys- teresis input selected	$0.74 V_{CC}$	-	$V_{CC} + 0.3$	V	$V_{CC} < 4.5\text{V}$
			TTL input selected	2.0	-	$V_{CC} + 0.3$	V	
	V_{IHX0F}	X0	External clock in "Fast Clock Input mode"	$0.8 V_{CC}$	-	$V_{CC} + 0.3$	V	Not available in MB96F34xY/R/AxA
	V_{IHX0S}	X0,X1, X0A,X1A	External clock in "oscil- lation mode"	2.5	-	$V_{CC} + 0.3$	V	
	V_{IHR}	RSTX	-	$0.8 V_{CC}$	-	$V_{CC} + 0.3$	V	CMOS Hysteresis input
	V_{IHM}	MD2-MD0	-	$V_{CC} - 0.3$	-	$V_{CC} + 0.3$	V	
Input L voltage	V_{IL}	Port inputs Pnn_m	CMOS Hysteresis 0.8/0.2 input selected	$V_{SS} - 0.3$	-	$0.2 V_{CC}$	V	
			CMOS Hysteresis 0.7/0.3 input selected	$V_{SS} - 0.3$	-	$0.3 V_{CC}$	V	
			AUTOMOTIVE Hys- teresis input selected	$V_{SS} - 0.3$	-	$0.5 V_{CC}$	V	$V_{CC} \geq 4.5\text{V}$
			TTL input selected	$V_{SS} - 0.3$	-	0.8	V	$V_{CC} < 4.5\text{V}$
	V_{ILX0F}	X0	External clock in "Fast Clock Input mode"	$V_{SS} - 0.3$	-	$0.2 V_{CC}$	V	Not available in MB96F34xY/R/AxA
	V_{ILX0S}	X0,X1, X0A,X1A	External clock in "oscillation mode"	$V_{SS} - 0.3$	-	0.4	V	
	V_{ILR}	RSTX	-	$V_{SS} - 0.3$	-	$0.2 V_{CC}$	V	CMOS Hysteresis input
	V_{ILM}	MD2-MD0	-	$V_{SS} - 0.3$	-	$V_{SS} + 0.3$	V	
Output H voltage	V_{OH2}	Normal outputs	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $I_{OH} = -2\text{mA}$	$V_{CC} - 0.5$	-	-	V	Driving strength set to 2mA
			$3.0\text{V} \leq V_{CC} < 4.5\text{V}$ $I_{OH} = -1.6\text{mA}$					
	V_{OH5}	Normal outputs	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $I_{OH} = -5\text{mA}$	$V_{CC} - 0.5$	-	-	V	Driving strength set to 5mA
			$3.0\text{V} \leq V_{CC} < 4.5\text{V}$ $I_{OH} = -3\text{mA}$					
	V_{OH3}	3mA outputs	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $I_{OH} = -3\text{mA}$	$V_{CC} - 0.5$	-	-	V	
			$3.0\text{V} \leq V_{CC} < 4.5\text{V}$ $I_{OH} = -2\text{mA}$					

($T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = 0\text{V}$)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Output L voltage	V_{OL2}	Normal outputs	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $I_{OL} = +2\text{mA}$	-	-	0.4	V	Driving strength set to 2mA
			$3.0\text{V} \leq V_{CC} < 4.5\text{V}$ $I_{OL} = +1.6\text{mA}$					
	V_{OL5}	Normal outputs	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $I_{OL} = +5\text{mA}$	-	-	0.4	V	Driving strength set to 5mA
			$3.0\text{V} \leq V_{CC} < 4.5\text{V}$ $I_{OL} = +3\text{mA}$					
	V_{OL3}	3mA outputs	$3.0\text{V} \leq V_{CC} \leq 5.5\text{V}$ $I_{OL} = +3\text{mA}$	-	-	0.4	V	
Input leak current	I_{IL}	Pnn_m	$V_{SS} < V_I < V_{CC}$ $AV_{SS}, AVR_L < V_I < AV_{CC}, AVR_H$	-1	-	+1	μA	Single port pin
Pull-up resistance	R_{UP}	Pnn_m, RSTX	$V_{CC} = 3.3\text{V} \pm 10\%$	40	100	160	$\text{k}\Omega$	
			$V_{CC} = 5.0\text{V} \pm 10\%$	25	50	100	$\text{k}\Omega$	



Refer to the Hardware Manual for detailed Timing Charts

14.4.8 Bus Timing (Read)

($T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $I_{Odrive} = 5\text{mA}$, $C_L = 50\text{pF}$)

Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
ALE pulse width	t _{LHLL}	ALE	EACL:STS=0 and EACL:ACE=0	t _{CYC} /2 – 5	-	ns	
			EACL:STS=1	t _{CYC} – 5	-		
			EACL:STS=0 and EACL:ACE=1	3t _{CYC} /2 – 5	-		
Valid address ⇒ ALE ↓ time	t _{AVLL}	ALE, A[23:16],	EACL:STS=0 and EACL:ACE=0	t _{CYC} – 15	-	ns	
			EACL:STS=1 and EACL:ACE=0	3t _{CYC} /2 – 15	-		
			EACL:STS=0 and EACL:ACE=1	2t _{CYC} – 15	-		
			EACL:STS=1 and EACL:ACE=1	5t _{CYC} /2 – 15	-		
	t _{ADVLL}	ALE,AD[15:0]	EACL:STS=0 and EACL:ACE=0	t _{CYC} /2 – 15	-	ns	
			EACL:STS=1 and EACL:ACE=0	t _{CYC} – 15	-		
			EACL:STS=0 and EACL:ACE=1	3t _{CYC} /2 – 15	-		
			EACL:STS=1 and EACL:ACE=1	2t _{CYC} – 15	-		
ALE ↓ ⇒ Address valid time	t _{LLAX}	ALE, AD[15:0]	EACL:STS=0	t _{CYC} /2 – 15	-	ns	
			EACL:STS=1	-15	-		
Valid address ⇒ RDX ↓ time	t _{AVRL}	RDX, A[23:16]	EACL:ACE=0	3t _{CYC} /2 – 15	-	ns	
			EACL:ACE=1	5t _{CYC} /2 – 15	-		
	t _{ADVRL}	RDX, AD[15:0]	EACL:ACE=0	t _{CYC} – 15	-	ns	
			EACL:ACE=1	2t _{CYC} – 15	-		
Valid address ⇒ Valid data input	t _{AVDV}	A[23:16], AD[15:0]	EACL:ACE=0	-	3t _{CYC} – 55	ns	w/o cycle extension
			EACL:ACE=1	-	4t _{CYC} – 55		
	t _{ADV DV}	AD[15:0]	EACL:ACE=0	-	5t _{CYC} /2 – 55	ns	w/o cycle extension
			EACL:ACE=1	-	7t _{CYC} /2 – 55		
RDX pulse width	t _{RLRH}	RDX	-	3 t _{CYC} /2 – 5	-	ns	w/o cycle extension
RDX ↓ ⇒ Valid data input	t _{RLDV}	RDX, AD[15:0]	-	-	3 t _{CYC} /2 – 50	ns	w/o cycle extension
RDX ↑ ⇒ Data hold time	t _{RHDX}	RDX, AD[15:0]	-	0	-	ns	
Address valid ⇒ Data hold time	t _{AXDX}	A[23:16], AD[15:0]	-	0	-	ns	

($T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $I_{Odrive} = 5\text{ mA}$, $C_L = 50\text{ pF}$)

Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
RDX $\uparrow \Rightarrow$ ALE $\uparrow$ time	t_{RHLH}	RDX, ALE	EACL:STS=1 and EACL:ACE=1	$3t_{CYC}/2 - 10$	-	ns	
			other ECL:STS, EACL:ACE setting	$t_{CYC}/2 - 10$	-		
Valid address $\Rightarrow$ ECLK $\uparrow$ time	t_{AVCH}	A[23:16], ECLK	-	$t_{CYC} - 15$	-	ns	
	t_{ADVCH}	AD[15:0], ECLK		$t_{CYC}/2 - 15$	-		
RDX $\downarrow \Rightarrow$ ECLK $\uparrow$ time	t_{RLCH}	RDX, ECLK	-	$t_{CYC}/2 - 10$	-	ns	
ALE $\downarrow \Rightarrow$ RDX $\downarrow$ time	t_{LLRL}	ALE, RDX	EACL:STS=0	$t_{CYC}/2 - 10$	-	ns	
			EACL:STS=1	- 10	-		
ECLK $\uparrow \Rightarrow$ Valid data input	t_{CHDV}	AD[15:0], ECLK	-	-	$t_{CYC} - 50$	ns	

($T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 3.0$ to 4.5 V , $V_{SS} = 0.0\text{ V}$, $I_{Odrive} = 5\text{ mA}$, $C_L = 50\text{ pF}$)

Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
ALE pulse width	t _{LHLL}	ALE	EACL:STS=0 and EACL:ACE=0	t _{CYC} /2 – 8	-	ns	
			EACL:STS=1	t _{CYC} – 8	-		
			EACL:STS=0 and EACL:ACE=1	3t _{CYC} /2 – 8	-		
Valid address ⇒ ALE ↓ time	t _{AVLL}	ALE, A[23:16],	EACL:STS=0 and EACL:ACE=0	t _{CYC} – 20	-	ns	
			EACL:STS=1 and EACL:ACE=0	3t _{CYC} /2 – 20	-		
			EACL:STS=0 and EACL:ACE=1	2t _{CYC} – 20	-		
			EACL:STS=1 and EACL:ACE=1	5t _{CYC} /2 – 20	-		
	t _{ADVLL}	ALE, AD[15:0]	EACL:STS=0 and EACL:ACE=0	t _{CYC} /2 – 20	-	ns	
			EACL:STS=1 and EACL:ACE=0	t _{CYC} – 20	-		
			EACL:STS=0 and EACL:ACE=1	3t _{CYC} /2 – 20	-		
			EACL:STS=1 and EACL:ACE=1	2t _{CYC} – 20	-		
ALE ↓ ⇒ Address valid time	t _{LLAX}	ALE, AD[15:0]	EACL:STS=0	t _{CYC} /2 – 20	-	ns	
			EACL:STS=1	-20	-		
Valid address ⇒ RDX ↓ time	t _{AVRL}	RDX, A[23:16]	EACL:ACE=0	3t _{CYC} /2 – 20	-	ns	
			EACL:ACE=1	5t _{CYC} /2 – 20	-		
	t _{ADVRL}	RDX, AD[15:0]	EACL:ACE=0	t _{CYC} – 20	-	ns	
			EACL:ACE=1	2t _{CYC} – 20	-		

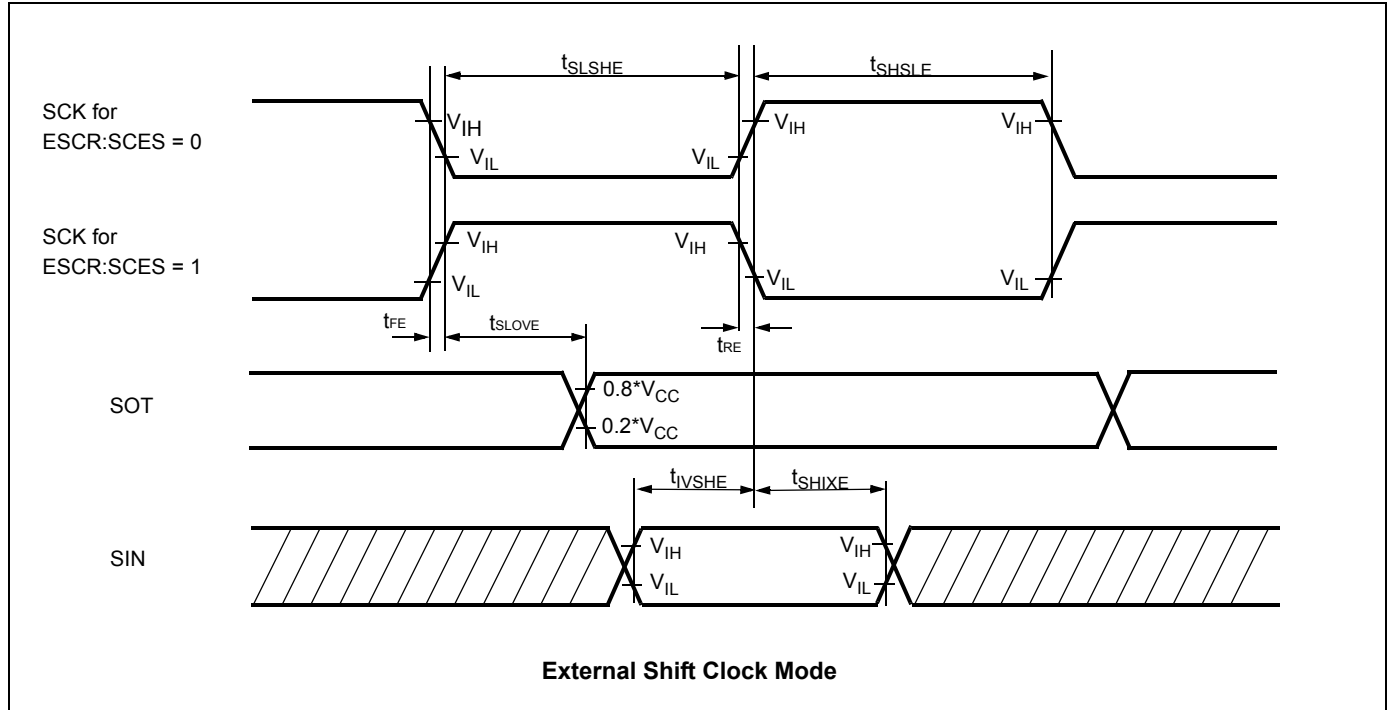
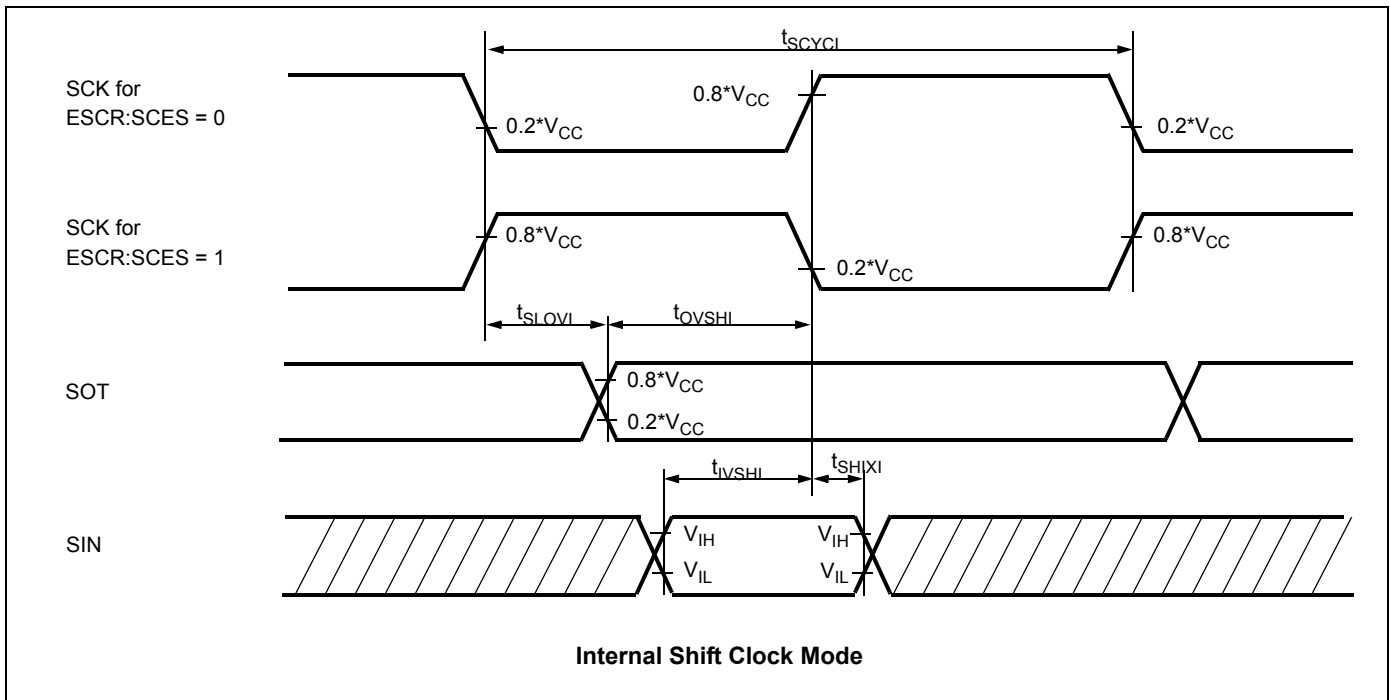
14.4.9 Bus Timing (Write)

($T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $I_{Odrive} = 5\text{mA}$, $C_L = 50\text{pF}$)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Valid address $\Rightarrow$ WRX $\downarrow$ time	t_{AVWL}	WRX, WRLX, WRHX, A[23:16]	EACL:ACE=0	$3t_{CYC}/2 - 15$	-	ns	
			EACL:ACE=1	$5t_{CYC}/2 - 15$	-		
	t_{ADVWL}	WRX, WRLX, WRHX, AD[15:0]	EACL:ACE=0	$t_{CYC} - 15$	-	ns	
			EACL:ACE=1	$2t_{CYC} - 15$	-		
WRX pulse width	t_{WLWH}	WRX, WRLX, WRHX	-	$t_{CYC} - 5$	-	ns	w/o cycle extension
Valid data output $\Rightarrow$ WRX $\uparrow$ time	t_{DVWH}	WRX, WRLX, WRHX, AD[15:0]	-	$t_{CYC} - 20$	-	ns	w/o cycle extension
WRX $\uparrow \Rightarrow$ Data hold time	t_{WHDX}	WRX, WRLX, WRHX, AD[15:0]	-	$t_{CYC}/2 - 15$	-	ns	
WRX $\uparrow \Rightarrow$ Address valid time	t_{WHAX}	WRX, WRLX, WRHX, A[23:16]	-	$t_{CYC}/2 - 15$	-	ns	
WRX $\uparrow \Rightarrow$ ALE $\uparrow$ time	t_{WHLH}	WRX, WRLX, WRHX, ALE	EBM:ACE=1 and EACL:STS=1	$2t_{CYC} - 10$	-	ns	
			other EBM:ACE and EACL:STS setting	$t_{CYC} - 10$	-		
WRX $\downarrow \Rightarrow$ ECLK $\uparrow$ time	t_{WLCH}	WRX, WRLX, WRHX, ECLK	-	$t_{CYC}/2 - 10$	-	ns	
CSn $\Rightarrow$ WRX time	t_{CSLWL}	WRX, WRLX, WRHX, CSn	EACL:ACE=0	-	$3t_{CYC}/2 - 15$	ns	
			EACL:ACE=1	-	$5t_{CYC}/2 - 15$		
WRX $\Rightarrow$ CSn time	t_{WHCSH}	WRX, WRLX, WRHX, CSn	-	$t_{CYC}/2 - 15$	-	ns	

($T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 3.0$ to 4.5V , $V_{SS} = 0.0\text{ V}$, $I_{Odrive} = 5\text{mA}$, $C_L = 50\text{pF}$)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Valid address $\Rightarrow$ WRX $\downarrow$ time	t_{AVWL}	WRX, WRLX, WRHX, A[23:16]	EACL:ACE=0	$3t_{CYC}/2 - 20$	-	ns	
			EACL:ACE=1	$5t_{CYC}/2 - 20$	-		
	t_{ADVWL}	WRX, WRLX, WRHX, AD[15:0]	EACL:ACE=0	$t_{CYC} - 20$	-	ns	
			EACL:ACE=1	$2t_{CYC} - 20$	-		



14.5 Analog Digital Converter

($T_A = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$, $3.0\text{ V} \leq \text{AVRH} - \text{AVRL}$, $V_{CC} = \text{AV}_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = \text{AV}_{SS} = 0\text{V}$)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	10	bit	
Total error	-	-	-3	-	+3	LSB	
Nonlinearity error	-	-	-2.5	-	+2.5	LSB	
Differential nonlinearity error	-	-	-1.9	-	+1.9	LSB	
Zero reading voltage	V_{OT}	ANn	$\text{AVRL} - 1.5\text{ LSB}$	$\text{AVRL} + 0.5\text{ LSB}$	$\text{AVRL} + 2.5\text{ LSB}$	V	
Full scale reading voltage	V_{FST}	ANn	$\text{AVRH} - 3.5\text{ LSB}$	$\text{AVRH} - 1.5\text{ LSB}$	$\text{AVRH} + 0.5\text{ LSB}$	V	
Compare time	-	-	1.0	-	16,500	μs	$4.5\text{V} \leq \text{AV}_{CC} \leq 5.5\text{V}$
			2.0	-	-	μs	$3.0\text{V} \leq \text{AV}_{CC} < 4.5\text{V}$
Sampling time	-	-	0.5	-	-	μs	$4.5\text{V} \leq \text{AV}_{CC} \leq 5.5\text{V}$
			1.2	-	-	μs	$3.0\text{V} \leq \text{AV}_{CC} < 4.5\text{V}$
Analog port input curren	I_{AIN}	ANn	-3	-	+3	μA	AV_{SS} , $\text{AVRL} < V_I < \text{AV}_{CC}$, AVRH
Analog port input curren	I_{AIN}	ANn	-1	-	+1	μA	$T_A = 25\text{ }^{\circ}\text{C}$, AV_{SS} , $\text{AVRL} < V_I < \text{AV}_{CC}$, AVRH
			-3	-	+3	μA	$T_A = 125\text{ }^{\circ}\text{C}$, AV_{SS} , $\text{AVRL} < V_I < \text{AV}_{CC}$, AVRH
Analog input voltage range	V_{AIN}	ANn	AVRL	-	AVRH	V	
Reference voltage range	AVRH	AVRH/ AVRL 2	0.75 AV_{CC}	-	AV_{CC}	V	
	AVRL	AVRL	AV_{SS}	-	0.25 AV_{CC}	V	
Power supply current	I_A	AV_{CC}	-	2.5	5	mA	A/D Converter active
	I_{AH}	AV_{CC}	-	-	5	μA	A/D Converter not operated
Reference voltage current	I_R	AVRH/ AVRL	-	0.7	1	mA	A/D Converter active
	I_{RH}	AVRH/ AVRL	-	-	5	μA	A/D Converter not operated
Offset between input channels	-	ANn	-	-	4	LSB	

Note: The accuracy gets worse as $|\text{AVRH} - \text{AVRL}|$ becomes smaller.

14.7 Low Voltage Detector Characteristics

($T_A = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$, $V_{CC} = AV_{CC} = 3.0\text{V} - 5.5\text{V}$, $V_{SS} = AV_{SS} = 0\text{V}$)

Parameter	Symbol	Value [1]		Value [2]		Unit	Remarks
		Min	Max	Min	Max		
Stabilization time	$T_{LVDSTAB}$	-	75	-	110	μs	After power-up or change of detection level
Level 0	V_{DL0}	2.7	2.9	2.65	2.95	V	CILCR:LVL[3:0]="0000"
Level 1	V_{DL1}	2.9	3.1	2.85	3.2	V	CILCR:LVL[3:0]="0001"
Level 2	V_{DL2}	3.1	3.3	3.05	3.4	V	CILCR:LVL[3:0]="0010"
Level 3	V_{DL3}	3.5	3.75	3.45	3.85	V	CILCR:LVL[3:0]="0011"
Level 4	V_{DL4}	3.6	3.85	3.55	3.95	V	CILCR:LVL[3:0]="0100"
Level 5	V_{DL5}	3.7	3.95	3.65	4.1	V	CILCR:LVL[3:0]="0101"
Level 6	V_{DL6}	3.8	4.05	3.75	4.2	V	CILCR:LVL[3:0]="0110"
Level 7	V_{DL7}	3.9	4.15	3.85	4.3	V	CILCR:LVL[3:0]="0111"
Level 8	V_{DL8}	4.0	4.25	3.95	4.4	V	CILCR:LVL[3:0]="1000"
Level 9	V_{DL9}	4.1	4.35	4.05	4.5	V	CILCR:LVL[3:0]="1001"
Level 10	V_{DL10}	not used		not used			
Level 11	V_{DL11}	not used		not used			
Level 12	V_{DL12}	not used		not used			
Level 13	V_{DL13}	not used		not used			
Level 14	V_{DL14}	not used		not used			
Level 15	V_{DL15}	not used		not used			

[1]: valid for all devices except devices listed under "[2]"

[2]: valid for: MB96F345

CILCR:LVL[3:0] are the low voltage detector level select bits of the CILCR register.

Levels 10 to 15 are not used in this device.

For correct detection, the slope of the voltage level must satisfy $\left| \frac{dV}{dt} \right| \leq 0.004 \frac{V}{\mu\text{s}}$.

Faster variations are regarded as noise and may not be detected.

The functional operation of the MCU is guaranteed down to the minimum low voltage detection level of $V_{CC} = 2.7\text{V}$. The electrical characteristics however are only valid in the specified range (usually down to 3.0V).

14.7.1 Low Voltage Detector Operation

In the following figure, the occurrence of a low voltage condition is illustrated. For a detailed description of the reset and startup behavior, please refer to the corresponding hardware manual chapter.

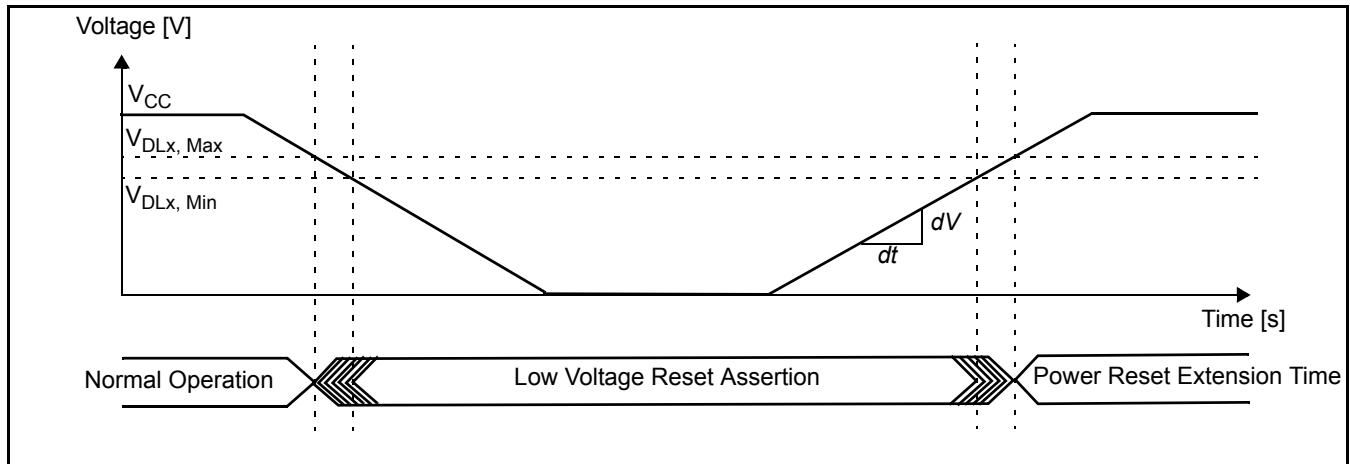
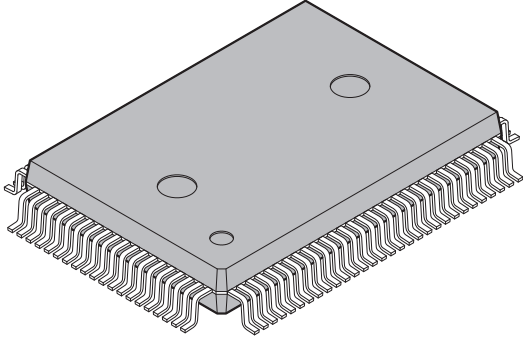
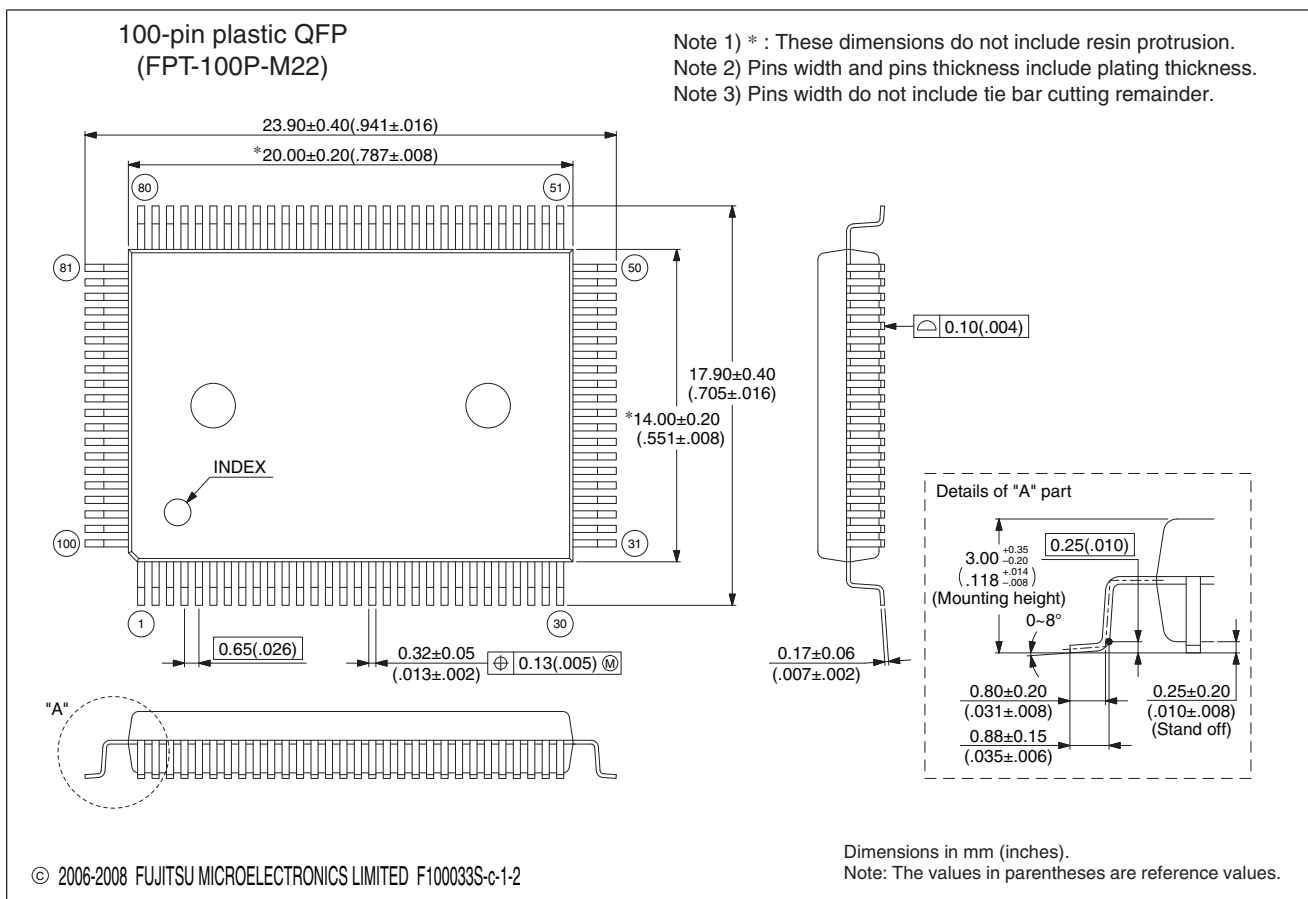


Table 6: Used settings

Mode	Selected Source Clock	Clock/Regulator Settings
Timer mode	PLL	CLKMC = 4 MHz, CLKPLL = 56 MHz (System clocks are stopped in this mode) Regulator in High Power Mode, Core Voltage = 1.9 V
	Main osc.	CLKMC = 4 MHz (System clocks are stopped in this mode) Regulator in High Power Mode, Core Voltage = 1.8 V
	RC clock fast	CLKRC = 2 MHz (System clocks are stopped in this mode) Regulator in High Power Mode, Core Voltage = 1.8 V
	RC clock slow	CLKRC = 100 kHz (System clocks are stopped in this mode) Regulator in High Power Mode, Core Voltage = 1.8 V
	Sub osc.	CLKSC = 100 kHz (System clocks are stopped in this mode) Regulator in Low Power Mode A, Core Voltage = 1.8 V
Stop mode	stopped	(All clocks are stopped in this mode) Regulator in Low Power Mode B, Core Voltage = 1.8 V

17. Package Dimension MB96(F)34x QFP 100P

100-pin plastic QFP  (FPT-100P-M22)	Lead pitch	0.65 mm
	Package width × package length	14.00 mm × 20.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	3.35 mm MAX
	Code (Reference)	P-QFP100-14×20-0.65



20. Main Changes in this Edition

Page	Section	Change Results
89	Electrical Characteristics 14.5. Analog Digital Converter	Corrected "Value" and "Unit" of Zero reading voltage. (AVRL - 1.5 → AVRL - 1.5 LSB AVRL + 0.5 → AVRL + 0.5 LSB AVRL + 2.5 → AVRL + 2.5 LSB LSB → V) Corrected "Value" and "Unit" of Full scale reading voltage. (AVRH - 3.5 → AVRH - 3.5 LSB AVRH - 1.5 → AVRH - 1.5 LSB AVRH + 0.5 → AVRH + 0.5 LSB LSB → V)

NOTE: Please see "Document History" for later revised information.

Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	—	AKIH	06/17/2009	Migrated to Cypress and assigned document number 002-04579. No change to document contents or format.
*A	5198948	AKIH	04/04/2016	Updated to Cypress template