Infineon Technologies - MB96F346ASBPMCR-GSE2 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	56MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, LVR, POR, PWM, WDT
Number of I/O	82
Program Memory Size	288KB (288K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f346asbpmcr-gse2

Features

Feature	Description
Technology	■ 0.18μm CMOS
CPU	■ F^{2}MC-16FX CPU ■ Up to 56 MHz internal, 17.8 ns instruction cycle time ■ Optimized instruction set for controller applications (bit, byte, word and long-word data types; 23 different addressing modes; barrel shift; variety of pointers) ■ 8-byte instruction execution queue ■ Signed multiply (16-bit × 16-bit) and divide (32-bit/16-bit) instructions available
System clock	■ On-chip PLL clock multiplier (x1 - x25, x1 when PLL stop) ■ 3 MHz - 16 MHz external crystal oscillator clock (maximum frequency when using ceramic resonator depends on Q-factor). ■ Up to 56 MHz external clock for devices with fast clock input feature ■ 32-100 kHz subsystem quartz clock ■ 100kHz/2MHz internal RC clock for quick and safe startup, oscillator stop detection, watchdog ■ Clock source selectable from main- and subclock oscillator (part number suffix “W”) and on-chip RC oscillator, independently for CPU and 2 clock domains of peripherals. ■ Low Power Consumption - 13 operating modes : (different Run, Sleep, Timer modes, Stop mode) ■ Clock modulator
On-chip voltage regulator	■ Internal voltage regulator supports reduced internal MCU voltage, offering low EMI and low power consumption figures
Low voltage reset	■ Reset is generated when supply voltage is below minimum.
Code Security	■ Protects ROM content from unintended read-out
Memory Patch Function	■ Replaces ROM content ■ Can also be used to implement embedded debug support
DMA	■ Automatic transfer function independent of CPU, can be assigned freely to resources
Interrupts	■ Fast Interrupt processing ■ 8 programmable priority levels ■ Non-Maskable Interrupt (NMI)
Timers	■ Three independent clock timers (23-bit RC clock timer, 23-bit Main clock timer, 17-bit Sub clock timer) ■ Watchdog Timer
CAN	■ Supports CAN protocol version 2.0 part A and B ■ ISO16845 certified ■ Bit rates up to 1 Mbit/s ■ 32 message objects ■ Each message object has its own identifier mask ■ Programmable FIFO mode (concatenation of message objects) ■ Maskable interrupt ■ Disabled Automatic Retransmission mode for Time Triggered CAN applications ■ Programmable loop-back mode for self-test operation
USART	■ Full duplex USARTs (SCI/LIN) ■ Wide range of baud rate settings using a dedicated reload timer ■ Special synchronous options for adapting to different synchronous serial protocols ■ LIN functionality working either as master or slave LIN device

Feature	Description
Alarm comparator	■ Monitors an external voltage and generates an interrupt in case of a voltage lower or higher than the defined thresholds ■ Threshold voltages defined externally or generated internally ■ Status is readable, interrupts can be masked separately
I/O Ports	■ Virtually all external pins can be used as general purpose I/O ■ All push-pull outputs (except when used as I2C SDA/SCL line) ■ Bit-wise programmable as input/output or peripheral signal ■ Bit-wise programmable input enable ■ Bit-wise programmable input levels: Automotive / CMOS-Schmitt trigger / TTL (TTL levels not supported by all devices) ■ Bit-wise programmable pull-up resistor ■ Bit-wise programmable output driving strength for EMI optimization
Packages	■ 100-pin plastic QFP and LQFP
Flash Memory	■ Supports automatic programming, Embedded Algorithm ■ Write/Erase/Erase-Suspend/Resume commands ■ A flag indicating completion of the algorithm ■ Number of erase cycles: 10,000 times ■ Data retention time: 20 years ■ Erase can be performed on each sector individually ■ Sector protection ■ Flash Security feature to protect the content of the Flash ■ Low voltage detection during Flash erase

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5. Pin Circuit Type

Table 2: Pin circuit types

FPT-100P-M20		FPT-100P-M22	
Pin no.	Circuit type [1]	Pin no.	Circuit type [1]
1-10	H	1-12	H
11,12	B [2]	13, 14	B [2]
11,12	H [3]	13, 14	H [3]
13,14	Supply	15,16	Supply
15	F	17	F
16,17	H	18,19	H
18-21	N	20-23	N
22-29	I	24-31	I
30	Supply	32	Supply
31-32	G	33-34	G
33	Supply	35	Supply
34 to 41	I	36 to 43	I
42	Supply	44	Supply
43 to 48	I	45 to 50	I
49 to 51	C	51 to 53	C
52	E	54	E
53 to 54	I	55 to 56	I
55 to 62	H	57 to 64	H
63, 64	Supply	65, 66	Supply
65 to 87	H	67 to 89	H
88,89	Supply	90, 91	Supply
90, 91	A	92, 93	A
92-100	H	94 to 100	H

[1]: Please refer to “ I/O Circuit Type” for details on the I/O circuit types
[2]: Devices with suffix ”W”
[3]: Devices without suffix ”W”

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000081_H	PPG1 - Timer register			R
000082_H	PPG1 - Period setting register		PCSR1	W
000083_H	PPG1 - Period setting register			W
000084_H	PPG1 - Duty cycle register		PDUT1	W
000085_H	PPG1 - Duty cycle register			W
000086_H	PPG1 - Control status register Low	PCNL1	PCN1	R/W
000087_H	PPG1 - Control status register High	PCNH1		R/W
000088_H	PPG2 - Timer register		PTMR2	R
000089_H	PPG2 - Timer register			R
$00008A_H$	PPG2 - Period setting register		PCSR2	W
$00008B_H$	PPG2 - Period setting register			W
$00008C_H$	PPG2 - Duty cycle register		PDUT2	W
$00008D_H$	PPG2 - Duty cycle register			W
$00008E_H$	PPG2 - Control status register Low	PCNL2	PCN2	R/W
$00008F_H$	PPG2 - Control status register High	PCNH2		R/W
000090_H	PPG3 - Timer register		PTMR3	R
000091_H	PPG3 - Timer register			R
000092_H	PPG3 - Period setting register		PCSR3	W
000093_H	PPG3 - Period setting register			W
000094_H	PPG3 - Duty cycle register		PDUT3	W
000095_H	PPG3 - Duty cycle register			W
000096_H	PPG3 - Control status register Low	PCNL3	PCN3	R/W
000097_H	PPG3 - Control status register High	PCNH3		R/W
000098_H	PPG7-PPG4 - General Control register 1 Low	GCN1L1	GCN11	R/W
000099_H	PPG7-PPG4 - General Control register 1 High	GCN1H1		R/W
$00009A_H$	PPG7-PPG4 - General Control register 2 Low	GCN2L1	GCN21	R/W
$00009B_H$	PPG7-PPG4 - General Control register 2 High	GCN2H1		R/W
$00009C_H$	PPG4 - Timer register		PTMR4	R
$00009D_H$	PPG4 - Timer register			R
$00009E_H$	PPG4 - Period setting register		PCSR4	W
$00009F_H$	PPG4 - Period setting register			W
$0000A0_H$	PPG4 - Duty cycle register		PDUT4	W

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$00043B_H$-000443_H	Reserved			-
000444_H	I/O Port P00 - Port Input Enable Register	PIER00		R/W
000445_H	I/O Port P01 - Port Input Enable Register	PIER01		R/W
000446_H	I/O Port P02 - Port Input Enable Register	PIER02		R/W
000447_H	I/O Port P03 - Port Input Enable Register	PIER03		R/W
000448_H	I/O Port P04 - Port Input Enable Register	PIER04		R/W
000449_H	I/O Port P05 - Port Input Enable Register	PIER05		R/W
$00044A_H$	I/O Port P06 - Port Input Enable Register	PIER06		R/W
$00044B_H$	I/O Port P07 - Port Input Enable Register	PIER07		R/W
$00044C_H$	I/O Port P08 - Port Input Enable Register	PIER08		R/W
$00044D_H$	I/O Port P09 - Port Input Enable Register	PIER09		R/W
$00044E_H$	I/O Port P10 - Port Input Enable Register	PIER10		R/W
$00044F_H$-000457_H	Reserved			-
000458_H	I/O Port P00 - Port Input Level Register	PILR00		R/W
000459_H	I/O Port P01 - Port Input Level Register	PILR01		R/W
$00045A_H$	I/O Port P02 - Port Input Level Register	PILR02		R/W
$00045B_H$	I/O Port P03 - Port Input Level Register	PILR03		R/W
$00045C_H$	I/O Port P04 - Port Input Level Register	PILR04		R/W
$00045D_H$	I/O Port P05 - Port Input Level Register	PILR05		R/W
$00045E_H$	I/O Port P06 - Port Input Level Register	PILR06		R/W
$00045F_H$	I/O Port P07 - Port Input Level Register	PILR07		R/W
000460_H	I/O Port P08 - Port Input Level Register	PILR08		R/W
000461_H	I/O Port P09 - Port Input Level Register	PILR09		R/W
000462_H	I/O Port P10 - Port Input Level Register	PILR10		R/W
000463_H-$00046B_H$	Reserved			-
$00046C_H$	I/O Port P00 - Extended Port Input Level Register	EPILR00		R/W
$00046D_H$	I/O Port P01 - Extended Port Input Level Register	EPILR01		R/W
$00046E_H$	I/O Port P02 - Extended Port Input Level Register	EPILR02		R/W
$00046F_H$	I/O Port P03 - Extended Port Input Level Register	EPILR03		R/W
000470_H	I/O Port P04 - Extended Port Input Level Register	EPILR04		R/W
000471_H	I/O Port P05 - Extended Port Input Level Register	EPILR05		R/W
000472_H	I/O Port P06 - Extended Port Input Level Register	EPILR06		R/W

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$00058D_H$	PPG10 - Duty cycle register			W
$00058E_H$	PPG10 - Control status register Low	PCNL10	PCN10	R/W
$00058F_H$	PPG10 - Control status register High	PCNH10		R/W
000590_H	PPG11 - Timer register		PTMR11	R
000591_H	PPG11 - Timer register			R
000592_H	PPG11 - Period setting register		PCSR11	W
000593_H	PPG11 - Period setting register			W
000594_H	PPG11 - Duty cycle register		PDUT11	W
000595_H	PPG11 - Duty cycle register			W
000596_H	PPG11 - Control status register Low	PCNL11	PCN11	R/W
000597_H	PPG11 - Control status register High	PCNH11		R/W
000598_H	PPG15-PPG12 - General Control register 1 Low	GCN1L3	GCN13	R/W
000599_H	PPG15-PPG12 - General Control register 1 High	GCN1H3		R/W
$00059A_H$	PPG15-PPG12 - General Control register 2 Low	GCN2L3	GCN23	R/W
$00059B_H$	PPG15-PPG12 - General Control register 2 High	GCN2H3		R/W
$00059C_H$	PPG12 - Timer register		PTMR12	R
$00059D_H$	PPG12 - Timer register			R
$00059E_H$	PPG12 - Period setting register		PCSR12	W
$00059F_H$	PPG12 - Period setting register			W
$0005A0_H$	PPG12 - Duty cycle register		PDUT12	W
$0005A1_H$	PPG12 - Duty cycle register			W
$0005A2_H$	PPG12 - Control status register Low	PCNL12	PCN12	R/W
$0005A3_H$	PPG12 - Control status register High	PCNH12		R/W
$0005A4_H$	PPG13 - Timer register		PTMR13	R
$0005A5_H$	PPG13 - Timer register			R
$0005A6_H$	PPG13 - Period setting register		PCSR13	W
$0005A7_H$	PPG13 - Period setting register			W
$0005A8_H$	PPG13 - Duty cycle register		PDUT13	W
$0005A9_H$	PPG13 - Duty cycle register			W
$0005AA_H$	PPG13 - Control status register Low	PCNL13	PCN13	R/W
$0005AB_H$	PPG13 - Control status register High	PCNH13		R/W
$0005AC_H$	PPG14 - Timer register		PTMR14	R

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000884_H-$00088F_H$	Reserved			-
000890_H	CAN1 - New Data 1 Register Low	NEWDT1L1	NEWDT11	R
000891_H	CAN1 - New Data 1 Register High	NEWDT1H1		R
000892_H	CAN1 - New Data 2 Register Low	NEWDT2L1	NEWDT21	R
000893_H	CAN1 - New Data 2 Register High	NEWDT2H1		R
000894_H-$00089F_H$	Reserved			-
$0008A0_H$	CAN1 - Interrupt Pending 1 Register Low	INTPND1L1	INTPND11	R
$0008A1_H$	CAN1 - Interrupt Pending 1 Register High	INTPND1H1		R
$0008A2_H$	CAN1 - Interrupt Pending 2 Register Low	INTPND2L1	INTPND21	R
$0008A3_H$	CAN1 - Interrupt Pending 2 Register High	INTPND2H1		R
$0008A4_H$-$0008AF_H$	Reserved			-
$0008B0_H$	CAN1 - Message Valid 1 Register Low	MSGVAL1L1	MSGVAL11	R
$0008B1_H$	CAN1 - Message Valid 1 Register High	MSGVAL1H1		R
$0008B2_H$	CAN1 - Message Valid 2 Register Low	MSGVAL2L1	MSGVAL21	R
$0008B3_H$	CAN1 - Message Valid 2 Register High	MSGVAL2H1		R
$0008B4_H$-$0008CD_H$	Reserved			-
$0008CE_H$	CAN1 - Output enable register	COER1		R/W
$0008CF_H$-$0009FF_H$	Reserved			-
$000A00_H$	DMA - IO address block register 0	IOABK0		R/W
$000A01_H$	DMA - IO address block register 1	IOABK1		R/W
$000A02_H$	DMA - IO address block register 2	IOABK2		R/W
$000A03_H$	DMA - IO address block register 3	IOABK3		R/W
$000A04_H$	DMA - IO address block register 4	IOABK4		R/W
$000A05_H$	DMA - IO address block register 5	IOABK5		R/W
$000A06_H$-$000BFF_H$	Reserved			-

Note: Any write access to reserved addresses in the I/O map should not be performed. A read access to a reserved address results in reading ‘X’.Registers of resources which are described in this table, but which are not supported by the device, should also be handled as “Reserved”.

12. Interrupt Vector Table

Table 5: Interrupt vector table MB96(F)34x

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
0	$3FC_H$	CALLV0	No	-	
1	$3F8_H$	CALLV1	No	-	
2	$3F4_H$	CALLV2	No	-	
3	$3F0_H$	CALLV3	No	-	
4	$3EC_H$	CALLV4	No	-	
5	$3E8_H$	CALLV5	No	-	
6	$3E4_H$	CALLV6	No	-	
7	$3E0_H$	CALLV7	No	-	
8	$3DC_H$	RESET	No	-	
9	$3D8_H$	INT9	No	-	
10	$3D4_H$	EXCEPTION	No	-	
11	$3D0_H$	NMI	No	-	Non-Maskable Interrupt
12	$3CC_H$	DLY	No	12	Delayed Interrupt
13	$3C8_H$	RC_TIMER	No	13	RC Timer
14	$3C4_H$	MC_TIMER	No	14	Main Clock Timer
15	$3C0_H$	SC_TIMER	No	15	Sub Clock Timer
16	$3BC_H$	RESERVED	No	16	Reserved
17	$3B8_H$	EXTINT0	Yes	17	External Interrupt 0
18	$3B4_H$	EXTINT1	Yes	18	External Interrupt 1
19	$3B0_H$	EXTINT2	Yes	19	External Interrupt 2
20	$3AC_H$	EXTINT3	Yes	20	External Interrupt 3
21	$3A8_H$	EXTINT4	Yes	21	External Interrupt 4
22	$3A4_H$	EXTINT5	Yes	22	External Interrupt 5
23	$3A0_H$	EXTINT6	Yes	23	External Interrupt 6
24	$39C_H$	EXTINT7	Yes	24	External Interrupt 7
25	398_H	EXTINT8	Yes	25	External Interrupt 8
26	394_H	EXTINT9	Yes	26	External Interrupt 9
27	390_H	EXTINT10	Yes	27	External Interrupt 10
28	$38C_H$	EXTINT11	Yes	28	External Interrupt 11
29	388_H	EXTINT12	Yes	29	External Interrupt 12

Table 5: Interrupt vector table MB96(F)34x

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
30	384_H	EXTINT13	Yes	30	External Interrupt 13
31	380_H	EXTINT14	Yes	31	External Interrupt 14
32	$37C_H$	EXTINT15	Yes	32	External Interrupt 15
33	378_H	CAN0	No	33	CAN Controller 0 (except MB96(F)34xAyy or MB96(F)34xCyy)
34	374_H	CAN1	No	34	CAN Controller 1 (except MB96(F)34xAyy, MB96(F)34xCyy, MB96F345Dyy or MB96F345Fyy)
35	370_H	PPG0	Yes	35	Programmable Pulse Generator 0
36	$36C_H$	PPG1	Yes	36	Programmable Pulse Generator 1
37	368_H	PPG2	Yes	37	Programmable Pulse Generator 2
38	364_H	PPG3	Yes	38	Programmable Pulse Generator 3
39	360_H	PPG4	Yes	39	Programmable Pulse Generator 4
40	$35C_H$	PPG5	Yes	40	Programmable Pulse Generator 5
41	358_H	PPG6	Yes	41	Programmable Pulse Generator 6
42	354_H	PPG7	Yes	42	Programmable Pulse Generator 7
43	350_H	PPG8	Yes	43	Programmable Pulse Generator 8
44	$34C_H$	PPG9	Yes	44	Programmable Pulse Generator 9
45	348_H	PPG10	Yes	45	Programmable Pulse Generator 10
46	344_H	PPG11	Yes	46	Programmable Pulse Generator 11
47	340_H	PPG12	Yes	47	Programmable Pulse Generator 12
48	$33C_H$	PPG13	Yes	48	Programmable Pulse Generator 13
49	338_H	PPG14	Yes	49	Programmable Pulse Generator 14
50	334_H	PPG15	Yes	50	Programmable Pulse Generator 15
51	330_H	RLT0	Yes	51	Reload Timer 0
52	$32C_H$	RLT1	Yes	52	Reload Timer 1
53	328_H	RLT2	Yes	53	Reload Timer 2
54	324_H	RLT3	Yes	54	Reload Timer 3
55	320_H	PPGRLT	Yes	55	Reload Timer 6 - dedicated for PPG
56	$31C_H$	ICU0	Yes	56	Input Capture Unit 0
57	318_H	ICU1	Yes	57	Input Capture Unit 1
58	314_H	ICU2	Yes	58	Input Capture Unit 2
59	310_H	ICU3	Yes	59	Input Capture Unit 3

Table 5: Interrupt vector table MB96(F)34x

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
60	$30C_H$	ICU4	Yes	60	Input Capture Unit 4
61	308_H	ICU5	Yes	61	Input Capture Unit 5
62	304_H	ICU6	Yes	62	Input Capture Unit 6
63	300_H	ICU7	Yes	63	Input Capture Unit 7
64	$2FC_H$	OCU0	Yes	64	Output Compare Unit 0
65	$2F8_H$	OCU1	Yes	65	Output Compare Unit 1
66	$2F4_H$	OCU2	Yes	66	Output Compare Unit 2
67	$2F0_H$	OCU3	Yes	67	Output Compare Unit 3
68	$2EC_H$	OCU4	Yes	68	Output Compare Unit 4
69	$2E8_H$	OCU5	Yes	69	Output Compare Unit 5
70	$2E4_H$	OCU6	Yes	70	Output Compare Unit 6
71	$2E0_H$	OCU7	Yes	71	Output Compare Unit 7
72	$2DC_H$	FRT0	Yes	72	Free Running Timer 0
73	$2D8_H$	FRT1	Yes	73	Free Running Timer 1
74	$2D4_H$	IIC0	Yes	74	I2C interface
75	$2D0_H$	IIC1	Yes	75	I2C interface
76	$2CC_H$	ADC0	Yes	76	A/D Converter
77	$2C8_H$	ALARM0	No	77	Alarm Comparator 0 (except MB96F345Dyy or MB96F345Fyy)
78	$2C4_H$	ALARM1	No	78	Alarm Comparator 1 (except MB96F345Dyy or MB96F345Fyy)
79	$2C0_H$	LINR0	Yes	79	LIN USART 0 RX
80	$2BC_H$	LINT0	Yes	80	LIN USART 0 TX
81	$2B8_H$	LINR1	Yes	81	LIN USART 1 RX
82	$2B4_H$	LINT1	Yes	82	LIN USART 1 TX
83	$2B0_H$	LINR2	Yes	83	LIN USART 2 RX
84	$2AC_H$	LINT2	Yes	84	LIN USART 2 TX
85	$2A8_H$	LINR3	Yes	85	LIN USART 3 RX
86	$2A4_H$	LINT3	Yes	86	LIN USART 3 TX
87	$2A0_H$	FLASH_A	No	87	Flash memory A (only Flash devices)
88	$29C_H$	FLASH_B	No	88	Flash memory B (only MB96F348T/H/C)
89	298_H	LINR7	Yes	89	LIN USART 7 RX

Table 5: Interrupt vector table MB96(F)34x

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
90	294_H	LINT7	Yes	90	LIN USART 7 TX
91	290_H	LINR8	Yes	91	LIN USART 8 RX
92	$28C_H$	LINT8	Yes	92	LIN USART 8 TX
93	288_H	LINR9	Yes	93	LIN USART 9 RX
94	284_H	LINT9	Yes	94	LIN USART 9 TX
95	280_H	RTC0	No	95	Real Timer Clock
96	$27C_H$	CAL0	No	96	Clock Calibration Unit
97	278_H	DFLASH_A	Yes	97	Data Flash A (only MB96F345Dyy, MB96F345Fyy)

14. Electrical Characteristics

14.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	V_{SS} - 0.3	V_{SS} + 6.0	V	
	AV_{CC}	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_{CC} = AV_{CC}$ [1]
AD Converter voltage references	AVRH, AVRL	V_{SS} - 0.3	V_{SS} + 6.0	V	$AV_{CC} \geq AVRH$, $AV_{CC} \geq AVRL$, $AVRH > AVRL$, $AVRL \geq AV_{SS}$
Input voltage	V_I	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_I \leq V_{CC}$ + 0.3V [2]
Output voltage	V_O	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_O \leq V_{CC}$ + 0.3V [2]
Maximum Clamp Current	I_{CLAMP}	-4.0	+4.0	mA	Applicable to general purposeI/O pins [3]
Total Maximum Clamp Current	$\Sigma\|I_{CLAMP}\|$	-	40	mA	Applicable to general purposeI/O pins [3]
“L” level maximum output current	I_{OL1}	-	15	mA	Normal outputs with driving strength set to 5mA
“L” level average output current	I_{OLAV1}	-	5	mA	Normal outputs with driving strength set to 5mA
“L” level maximum overall output current	ΣI_{OL1}	-	100	mA	Normal outputs
“L” level average overall output current	ΣI_{OLAV1}	-	50	mA	Normal outputs
”H” level maximum output current	I_{OH1}	-	-15	mA	Normal outputs with driving strength set to 5mA
”H” level average output current	I_{OHAV1}	-	-5	mA	Normal outputs with driving strength set to 5mA
”H” level maximum overall output current	ΣI_{OH1}	-	-100	mA	Normal outputs
”H” level average overall output current	ΣI_{OHAV1}	-	-50	mA	Normal outputs
Permitted Power dissipation (Flash devices in QFP package) [4]	P_D	-	430[5]	mW	T_A=105°C
		-	750[5]	mW	T_A=90°C
		-	540[5]	mW	T_A=125°C, no Flash program/erase [6]
Permitted Power dissipation (MB96F346/F347/F348 in LQFP package) [4]	P_D	-	375[5]	mW	T_A=105°C
		-	750[5]	mW	T_A=85°C
		-	470[5]	mW	T_A=125°C, no Flash program/erase [6]
		-	560[5]	mW	T_A=120°C, no Flash program/erase [6]
Permitted Power dissipation (MB96F345 in LQFP package) [4]	P_D	-	335[5]	mW	T_A=105°C
		-	670[5]	mW	T_A=85°C
		-	840[5]	mW	T_A=75°C
		-	420[5]	mW	T_A=125°C, no Flash program/erase [6]
		-	590[5]	mW	T_A=115°C, no Flash program/erase [6]

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Run modes[1]	I_{CCPLL}	PLL Run mode with CLKS1/2 = 48MHz, CLKB = CLKP1/2 = 24MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	35	44	mA	Flash devices at 0 Flash wait states
			+125°C	36	47		
			+25°C	17	23	mA	MB96345/346 at 0 ROM wait states
			+125°C	18	25		
		PLL Run mode with CLKS1/2 = CLKB = CLKP1= 56MHz,CLKP2 = 28MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	44	57	mA	MB96F346/F347/F348 at 2 Flash wait states
			+125°C	45	60		
			+25°C	25	35	mA	MB96345/346 at 2 ROM wait states
			+125°C	26	37		
		PLL Run mode with CLKS1/2 = 72MHz, CLKB = CLKP1 = 36MHz, CLKP2 = 18MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	38	50	mA	MB96F346/F347/F348Y/R/Ayy at 1 Flash wait state
			+125°C	39	53		
		PLL Run mode with CLKS1/2 = 80MHz, CLKB = CLKP1 = 40MHz, CLKP2 = 20MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	TBD	TBD	mA	MB96F345 at 1 Flash wait state
			+125°C	TBD	TBD		
		PLL Run mode with CLKS1/2 = 96MHz, CLKB = CLKP1= 48MHz, CLKP2 = 24MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	49	62	mA	MB96F348T/H/CyB/C at 1 Flash wait state
			+125°C	50	65		
			+25°C	26	36	mA	MB96345/346 at 1 ROM wait state
			+125°C	27	38		
	I_{CCMAIN}	Main Run mode with CLKS1/2 = CLKB = CLKP1/2 = 4MHz (CLKPLL, CLKSC and CLKRC stopped)	+25°C	4.5	5.5	mA	Flash devices at 1 Flash wait state
			+125°C	5.1	8.5		
			+25°C	2.5	3.5	mA	MB96345/346 at 1 ROM wait state
			+125°C	3.1	5.5		

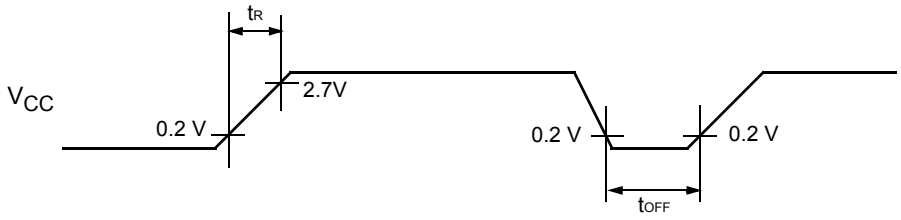
(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Timer modes[1]	I_{CCTRCL}	RC Timer mode with CLKRC = 100kHz, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)	+25°C	0.3	0.45	mA	MB96F346/F347/F348
			+125°C	0.8	3.2		
			+25°C	0.08	0.15	mA	MB96F345
			+125°C	0.58	2.95		
			+25°C	0.3	0.45	mA	MB96345/346
			+125°C	0.8	2.2		
		RC Timer mode with CLKRC = 100kHz, SMCR:LPMSS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode)	+25°C	0.05	0.1	mA	Flash devices
			+125°C	0.55	2.85		
			+25°C	0.05	0.1	mA	MB96345/346
			+125°C	0.55	1.85		
	I_{CCTSUB}	Sub Timer mode with CLKSC = 32kHz (CLKMC, CLKPLL and CLKRC stopped)	+25°C	0.03	0.1	mA	Flash devices
			+125°C	0.53	2.85		
			+25°C	0.03	0.1	mA	MB96345/346
			+125°C	0.53	1.85		
Power supply current in Stop Mode	I_{CCH}	VRCR:LPMB[2:0] = 110_B (Core voltage at 1.8V)	+25°C	0.02	0.08	mA	Flash devices
			+125°C	0.52	2.8		
			+25°C	0.02	0.08	mA	MB96345/346
			+125°C	0.52	1.8		
		VRCR:LPMB[2:0] = 000_B (Core voltage at 1.2V)	+25°C	0.015	0.06	mA	Flash devices
			+125°C	0.4	2.3		
			+25°C	0.015	0.06	mA	MB96345/346
			+125°C	0.4	1.4		
Power supply current for active Low Voltage detector	I_{CCLVD}	Low voltage detector enabled (RCR:LVDE = 1)	-	5	10	µA	MB96F345 Must be added to all current above
			+25°C	90	140	µA	Other devices Must be added to all current above
			+125°C	100	150		

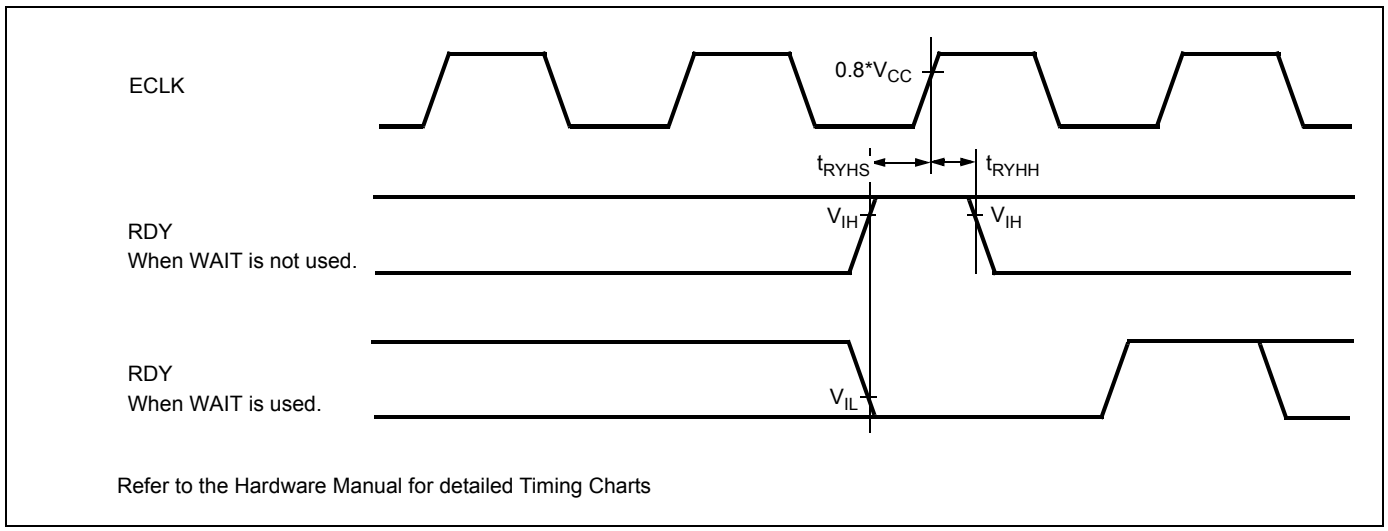
14.4.4 Power On Reset timing

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Power on rise time	t_R	Vcc	0.05	-	30	ms	
Power off time	t_{OFF}	Vcc	1	-	-	ms	



If the power supply is changed too rapidly, a power-on reset may occur.
We recommend a smooth startup by restraining voltages when changing the power supply voltage during operation, as shown in the figure below.



Refer to the Hardware Manual for detailed Timing Charts

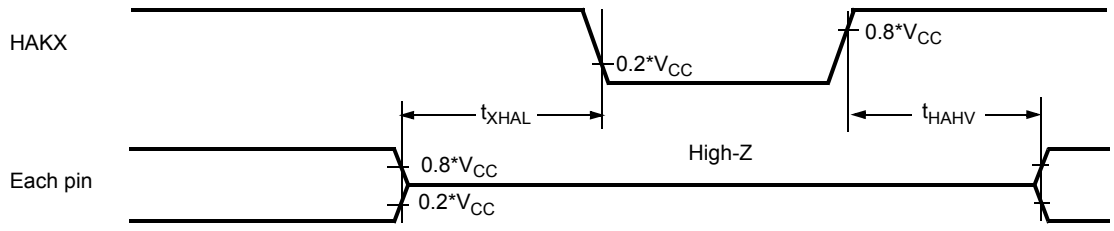
14.4.11 Hold Timing

(T_A = –40°C to +125°C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min	Max		
Pin floating ⇒ HAKX ↓ time	t_{XHAL}	HAKX	-	t_{CYC} – 20	t_{CYC} + 20	ns	
HAKX ↑ time ⇒ Pin valid time	t_{HAHV}	HAKX		t_{CYC} – 20	t_{CYC} + 20	ns	

(T_A = –40°C to +125°C, V_{CC} = 3.0 to 4.5V, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min	Max		
Pin floating ⇒ HAKX ↓ time	t_{XHAL}	HAKX	-	t_{CYC} – 25	t_{CYC} + 25	ns	
HAKX ↑ time ⇒ Pin valid time	t_{HAHV}	HAKX		t_{CYC} – 25	t_{CYC} + 25	ns	



Refer to the Hardware Manual for detailed Timing Charts

14.7 Low Voltage Detector Characteristics

(T_A = -40 °C to +125 °C, V_{cc} = AV_{cc} = 3.0V - 5.5V, V_{ss} = AV_{ss} = 0V)

Parameter	Symbol	Value [1]		Value [2]		Unit	Remarks
		Min	Max	Min	Max		
Stabilization time	$T_{LVDSTAB}$	-	75	-	110	µs	After power-up or change of detection level
Level 0	V_{DL0}	2.7	2.9	2.65	2.95	V	CILCR:LVL[3:0]="0000"
Level 1	V_{DL1}	2.9	3.1	2.85	3.2	V	CILCR:LVL[3:0]="0001"
Level 2	V_{DL2}	3.1	3.3	3.05	3.4	V	CILCR:LVL[3:0]="0010"
Level 3	V_{DL3}	3.5	3.75	3.45	3.85	V	CILCR:LVL[3:0]="0011"
Level 4	V_{DL4}	3.6	3.85	3.55	3.95	V	CILCR:LVL[3:0]="0100"
Level 5	V_{DL5}	3.7	3.95	3.65	4.1	V	CILCR:LVL[3:0]="0101"
Level 6	V_{DL6}	3.8	4.05	3.75	4.2	V	CILCR:LVL[3:0]="0110"
Level 7	V_{DL7}	3.9	4.15	3.85	4.3	V	CILCR:LVL[3:0]="0111"
Level 8	V_{DL8}	4.0	4.25	3.95	4.4	V	CILCR:LVL[3:0]="1000"
Level 9	V_{DL9}	4.1	4.35	4.05	4.5	V	CILCR:LVL[3:0]="1001"
Level 10	V_{DL10}	not used		not used			
Level 11	V_{DL11}	not used		not used			
Level 12	V_{DL12}	not used		not used			
Level 13	V_{DL13}	not used		not used			
Level 14	V_{DL14}	not used		not used			
Level 15	V_{DL15}	not used		not used			

[1]: valid for all devices except devices listed under "[2]"

[2]: valid for: MB96F345

CILCR:LVL[3:0] are the low voltage detector level select bits of the CILCR register.

Levels 10 to 15 are not used in this device.

For correct detection, the slope of the voltage level must satisfy $\left|\frac{dV}{dt}\right| \leq 0.004\frac{V}{\mu s}$.

Faster variations are regarded as noise and may not be detected.

The functional operation of the MCU is guaranteed down to the minimum low voltage detection level of Vcc = 2.7V. The electrical characteristics however are only valid in the specified range (usually down to 3.0V).

18.2 MCU without CAN Controller

Part number	Flash/ROM	Subclock	Package
MB96F346ASB PQC-GSE2	Flash A (288KB)	No	100 pin Plastic QFP (FPT-100P-M22)
MB96F346AWB PQC-GSE2		Yes	
MB96F346ASB PMC-GSE2		No	100 pin Plastic LQFP (FPT-100P-M20)
MB96F346AWB PMC-GSE2		Yes	
MB96F347ASB PQC-GSE2	Flash A (416KB)	No	100 pin Plastic QFP (FPT-100P-M22)
MB96F347AWB PQC-GSE2		Yes	
MB96F347ASB PMC-GSE2		No	100 pin Plastic LQFP (FPT-100P-M20)
MB96F347AWB PMC-GSE2		Yes	
MB96F348ASB PQC-GSE2	Flash A (544KB)	No	100 pin Plastic QFP (FPT-100P-M22)
MB96F348AWB PQC-GSE2		Yes	
MB96F348ASB PMC-GSE2		No	100 pin Plastic LQFP (FPT-100P-M20)
MB96F348AWB PMC-GSE2		Yes	
MB96F348CSC PQC-GSE2	Flash A (544KB) Flash B (32KB)	No	100 pin Plastic QFP (FPT-100P-M22)
MB96F348CWC PQC-GSE2		Yes	
MB96F348CSC PMC-GSE2		No	100 pin Plastic LQFP (FPT-100P-M20)
MB96F348CWC PMC-GSE2		Yes	

[1]: These devices are under development and specification is preliminary. These products under development may change its specification without notice.

This datasheet is also valid for the following outdated devices:

MB96F346YSA, MB96F346RSA, MB96F346YWA, MB96F346RWA,
MB96F347YSA, MB96F347RSA, MB96F347YWA, MB96F347RWA,
MB96F348YSA, MB96F348RSA, MB96F348YWA, MB96F348RWA,
MB96F348TSB, MB96F348HSB, MB96F348TWB, MB96F348HWB,
MB96F346ASA, MB96F346AWA,
MB96F347ASA, MB96F347AWA,
MB96F348ASA, MB96F348AWA,
MB96F348CSB, MB96F348CWB

20. Main Changes in this Edition

Page	Section	Change Results
89	Electrical Characteristics 14.5. Analog Digital Converter	Corrected "Value" and "Unit" of Zero reading voltage. (AVRL - 1.5 → AVRL - 1.5 LSB AVRL + 0.5 → AVRL + 0.5 LSB AVRL + 2.5 → AVRL + 2.5 LSB LSB → V) Corrected "Value" and "Unit" of Full scale reading voltage. (AVRH - 3.5 → AVRH - 3.5 LSB AVRH - 1.5 → AVRH - 1.5 LSB AVRH + 0.5 → AVRH + 0.5 LSB LSB → V)

NOTE: Please see "Document History" for later revised information.

Document History

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Document Title: MB96345/346, MB96F345, MB96F346/F347/F348, F^{2}MC-16FX, MB96340 Series, 16-bit Proprietary Microcontroller Datasheet **Document Number: 002-04579**				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	_	AKIH	06/17/2009	Migrated to Cypress and assigned document number 002-04579. No change to document contents or format.
*A	5198948	AKIH	04/04/2016	Updated to Cypress template