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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

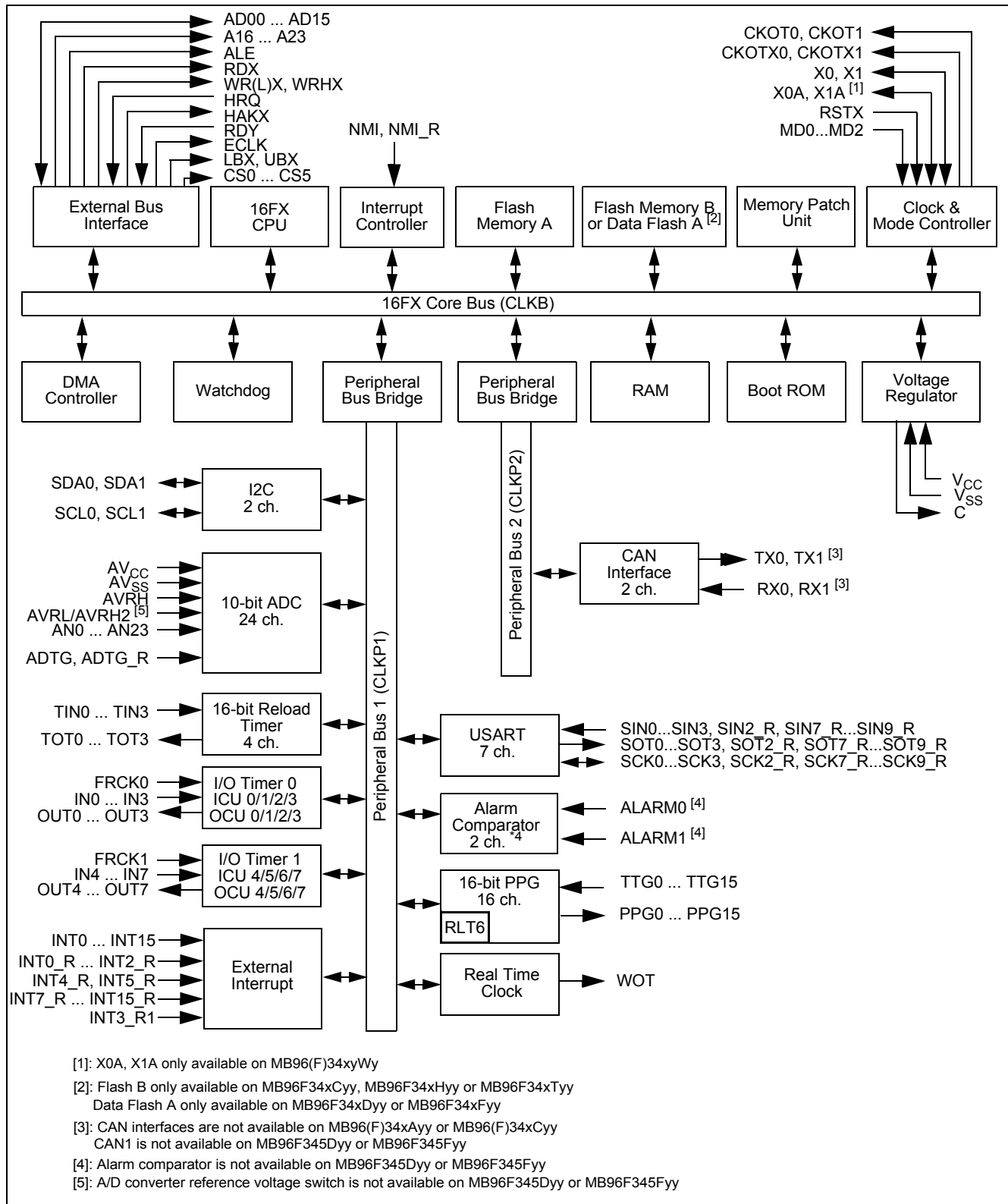
Product Status	Discontinued at Digi-Key
Core Processor	F ² MC-16FX
Core Size	16-Bit
Speed	56MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, LVR, POR, PWM, WDT
Number of I/O	82
Program Memory Size	288KB (288K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-PQFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f346rsapqcr-gse2

1. Product Lineup

Features		MB96V300B	MB96(F)34x
Product type		Evaluation sample	Flash product: MB96F34x Mask ROM product: MB9634x
Product options			
YS		NA	Low voltage reset persistently on / Single clock
RS			Low voltage reset can be disabled / Single clock
YW			Low voltage reset persistently on / Dual clock
RW			Low voltage reset can be disabled / Dual clock
TS			indep. 32KB Flash / Low voltage reset persistently on / Single clock
HS			indep. 32KB Flash / Low voltage reset can be disabled / Single clock
TW			indep. 32KB Flash / Low voltage reset persistently on / Dual clock
HW			indep. 32KB Flash / Low voltage reset can be disabled / Dual clock
FS			64KB Data Flash / Low voltage reset persistently on / Single clock
DS			64KB Data Flash / Low voltage reset can be disabled / Single clock
FW			64KB Data Flash / Low voltage reset persistently on / Dual clock
DW			64KB Data Flash / Low voltage reset can be disabled / Dual clock
AS			No CAN / Low voltage reset can be disabled / Single clock devices
CS			No CAN / indep. 32KB Flash / Low voltage reset can be disabled / Single clock
AW			No CAN / Low voltage reset can be disabled / Dual clock
CW			No CAN / indep. 32KB Flash / Low voltage reset can be disabled / Dual clock
Flash/ROM	RAM		
160KB	8KB	ROM/Flash memory emulation by external RAM, 92KB internal RAM	MB96345Y ^[1] , MB96345R ^[1]
224KB [Flash A: 160KB, Data Flash A: 64KB]	8KB		MB96F345F ^[1] , MB96F345D ^[1]
288KB	16KB		MB96F346Y, MB96346Y ^[1] , MB96F346R, MB96346R ^[1] , MB96F346A
416KB	16KB		MB96F347Y, MB96F347R, MB96F347A
544KB	24KB		MB96F348Y, MB96F348R, MB96F348A
576KB [Flash A: 544KB, Flash B: 32KB]	24KB		MB96F348T, MB96F348H, MB96F348C
Package		BGA416	FPT-100P-M20 FPT-100P-M22
DMA		16 channels	6 channels
USART		10 channels	7 channels

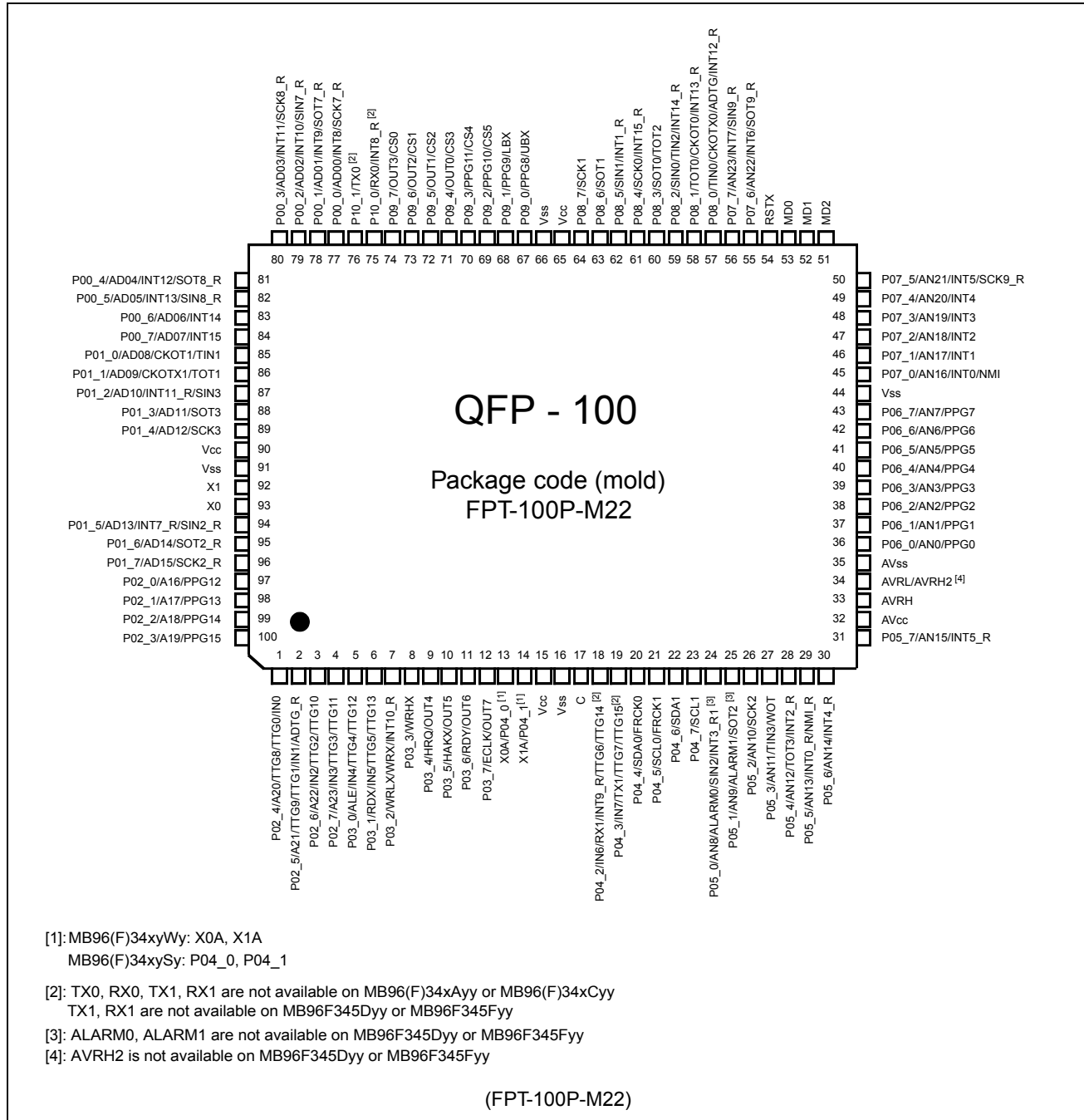
2. Block Diagram

Figure 1. Block diagram of MB96(F)34x



3. Pin Assignments

Figure 2. Pin assignment of MB96(F)34x (FPT-100P-M22)



[1]: MB96(F)34xyWy: X0A, X1A

MB96(F)34xySy: P04_0, P04_1

[2]: TX0, RX0, TX1, RX1 are not available on MB96(F)34xAyy or MB96(F)34xCyy
TX1, RX1 are not available on MB96F345Dyy or MB96F345Fyy

[3]: ALARM0, ALARM1 are not available on MB96F345Dyy or MB96F345Fyy

[4]: AVRH2 is not available on MB96F345Dyy or MB96F345Fyy

(FPT-100P-M22)

Remark:

MB96(F)34x products are pin-compatible to F²MC-16LX family MB90340 series.

7. Memory Map

MB96V300B			MB96(F)34x		
FF:FFFF _H	Emulation ROM		USER ROM / External Bus ^[4]		
DE:0000 _H					
	External Bus		External Bus		
10:0000 _H					
0F:E000 _H	Boot-ROM		Boot-ROM		
	Reserved	0F:0000 _H	Reserved		
0E:0000 _H			DATA FLASH / Reserved ^[4]		
	External RAM	0C:0000 _H	Reserved		
02:0000 _H			Reserved		
	Internal RAM bank 1	RAMEND1 ^[2] RAMSTART1 ^[2]	Internal RAM bank 1		RAM availability depending on the device
01:0000 _H			Reserved		
	ROM/RAM MIRROR		ROM/RAM MIRROR		
00:8000 _H					
	Internal RAM bank 0	RAMSTART0 ^[2]	Internal RAM bank 0		
			Reserved		
RAMSTART0 ^[3]			External Bus		External Bus end address ^[2]
00:0C00 _H	External Bus				
	Peripherals		Peripherals		
00:0380 _H					
00:0180 _H	GPR ^[1]		GPR ^[1]		
00:0100 _H	DMA		DMA		
00:00F0 _H	External Bus		External Bus		
00:0000 _H	Peripheral		Peripheral		

[1]: Unused GPR banks can be used as RAM area

[2]: For External Bus end address and RAMSTART/END addresses, please refer to the table on the next page.

[3]: For EVA device, RAMSTART0 depends on the configuration of the emulated device.

[4]: For details about USER ROM area or DATA FLASH area, see the [User ROM Memory Map For Flash Devices](#) and [User ROM Memory Map for Mask ROM Devices](#) on the following pages.

The External Bus area and DMA area are only available if the device contains the corresponding resource.

The available RAM and ROM area depends on the device.

8. User ROM Memory Map For Flash Devices

MB96F345D MB96F345F					
Alternative mode CPU address	Flash memory mode address	Flash size 160kByte +64KByte Data Flash			
FF:FFFF _H FF:0000 _H	3F:FFFF _H 3F:0000 _H	S39 - 64K	Flash A		
FE:FFFF _H FE:0000 _H	3E:FFFF _H 3E:0000 _H	S38 - 64K			
FD:FFFF _H FD:0000 _H	3D:FFFF _H 3D:0000 _H	External bus			
FC:FFFF _H FC:0000 _H	3C:FFFF _H 3C:0000 _H				
FB:FFFF _H FB:0000 _H	3B:FFFF _H 3B:0000 _H				
FA:FFFF _H FA:0000 _H	3A:FFFF _H 3A:0000 _H				
F9:FFFF _H F9:0000 _H	39:FFFF _H 39:0000 _H				
F8:FFFF _H F8:0000 _H	38:FFFF _H 38:0000 _H				
F7:FFFF _H F7:0000 _H	37:FFFF _H 37:0000 _H				
F6:FFFF _H F6:0000 _H	36:FFFF _H 36:0000 _H				
F5:FFFF _H F5:0000 _H	35:FFFF _H 35:0000 _H				
F4:FFFF _H F4:0000 _H	34:FFFF _H 34:0000 _H				
F3:FFFF _H F3:0000 _H	33:FFFF _H 33:0000 _H				
F2:FFFF _H F2:0000 _H	32:FFFF _H 32:0000 _H				
F1:FFFF _H F1:0000 _H	31:FFFF _H 31:0000 _H				
F0:FFFF _H F0:0000 _H	30:FFFF _H 30:0000 _H				
E0:FFFF _H E0:0000 _H					
DF:FFFF _H DF:8000 _H				Reserved	
DF:7FFF _H DF:6000 _H	1F:7FFF _H 1F:6000 _H			SA3 - 8K	Flash A
DF:5FFF _H DF:4000 _H	1F:5FFF _H 1F:4000 _H			SA2 - 8K	
DF:3FFF _H DF:2000 _H	1F:3FFF _H 1F:2000 _H			SA1 - 8K	
DF:1FFF _H DF:0000 _H	1F:1FFF _H 1F:0000 _H			SA0 - 8K ^[1]	
DE:FFFF _H DE:0000 _H				Reserved	
0E:FFFF _H 0E:FF00 _H	(0E:FFFF _H) (0E:FF00 _H)			SDA0-256 ^[2]	Data Flash A
0E:FEFF _H 0E:0000 _H				Reserved	
0D:FFFF _H 0D:C000 _H	(0F:FFFF _H) (0F:C000 _H)	SDA4-16K	Data Flash A		
0D:BFFF _H 0D:8000 _H	(0F:BFFF _H) (0F:8000 _H)	SDA3-16K			
0D:7FFF _H 0D:4000 _H	(0F:7FFF _H) (0F:4000 _H)	SDA2-16K			
0D:3FFF _H 0D:0000 _H	(0F:3FFF _H) (0F:0000 _H)	SDA1-16K			
0C:FFFF _H 0C:0000 _H		Reserved			

[1]: Sector SA0 contains the ROM Configuration Block RCBA at CPU address DF:0000_H - DF:007F_H

[2]: Sector SDA0 contains the ROM Configuration Block RCBD A at CPU address DE:FF00_H - DE:FF2F_H

[1]: Sector SA0 contains the ROM Configuration Block RCBA at CPU address DF:0000_H - DF:007F_H

[2]: Sector SDA0 contains the ROM Configuration Block RCBDA at CPU address DE:FF00_H - DE:FF2F_H

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00002B _H	OCU0 - Compare Register			R/W
00002C _H	OCU1 - Compare Register		OCCP1	R/W
00002D _H	OCU1 - Compare Register			R/W
00002E _H	OCU2 - Output Compare Control Status	OCS2		R/W
00002F _H	OCU3 - Output Compare Control Status	OCS3		R/W
000030 _H	OCU2 - Compare Register		OCCP2	R/W
000031 _H	OCU2 - Compare Register			R/W
000032 _H	OCU3 - Compare Register		OCCP3	R/W
000033 _H	OCU3 - Compare Register			R/W
000034 _H	OCU4 - Output Compare Control Status	OCS4		R/W
000035 _H	OCU5 - Output Compare Control Status	OCS5		R/W
000036 _H	OCU4 - Compare Register		OCCP4	R/W
000037 _H	OCU4 - Compare Register			R/W
000038 _H	OCU5 - Compare Register		OCCP5	R/W
000039 _H	OCU5 - Compare Register			R/W
00003A _H	OCU6 - Output Compare Control Status	OCS6		R/W
00003B _H	OCU7 - Output Compare Control Status	OCS7		R/W
00003C _H	OCU6 - Compare Register		OCCP6	R/W
00003D _H	OCU6 - Compare Register			R/W
00003E _H	OCU7 - Compare Register		OCCP7	R/W
00003F _H	OCU7 - Compare Register			R/W
000040 _H	ICU0/ICU1 - Control Status Register	ICS01		R/W
000041 _H	ICU0/ICU1 - Edge register	ICE01		R/W
000042 _H	ICU0 - Capture Register Low	IPCPL0	IPCP0	R
000043 _H	ICU0 - Capture Register High	IPCPH0		R
000044 _H	ICU1 - Capture Register Low	IPCPL1	IPCP1	R
000045 _H	ICU1 - Capture Register High	IPCPH1		R
000046 _H	ICU2/ICU3 - Control Status Register	ICS23		R/W
000047 _H	ICU2/ICU3 - Edge register	ICE23		R/W
000048 _H	ICU2 - Capture Register Low	IPCPL2	IPCP2	R
000049 _H	ICU2 - Capture Register High	IPCPH2		R
00004A _H	ICU3 - Capture Register Low	IPCPL3	IPCP3	R

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00004B _H	ICU3 - Capture Register High	IPCPH3		R
00004C _H	ICU4/ICU5 - Control Status Register	ICS45		R/W
00004D _H	ICU4/ICU5 - Edge register	ICE45		R/W
00004E _H	ICU4 - Capture Register Low	IPCPL4	IPCP4	R
00004F _H	ICU4 - Capture Register High	IPCPH4		R
000050 _H	ICU5 - Capture Register Low	IPCPL5	IPCP5	R
000051 _H	ICU5 - Capture Register High	IPCPH5		R
000052 _H	ICU6/ICU7 - Control Status Register	ICS67		R/W
000053 _H	ICU6/ICU7 - Edge register	ICE67		R/W
000054 _H	ICU6 - Capture Register Low	IPCPL6	IPCP6	R
000055 _H	ICU6 - Capture Register High	IPCPH6		R
000056 _H	ICU7 - Capture Register Low	IPCPL7	IPCP7	R
000057 _H	ICU7 - Capture Register High	IPCPH7		R
000058 _H	EXTINT0 - External Interrupt Enable Register	ENIR0		R/W
000059 _H	EXTINT0 - External Interrupt Interrupt request Register	EIRR0		R/W
00005A _H	EXTINT0 - External Interrupt Level Select Low	ELVRL0	ELVR0	R/W
00005B _H	EXTINT0 - External Interrupt Level Select High	ELVRH0		R/W
00005C _H	EXTINT1 - External Interrupt Enable Register	ENIR1		R/W
00005D _H	EXTINT1 - External Interrupt Interrupt request Register	EIRR1		R/W
00005E _H	EXTINT1 - External Interrupt Level Select Low	ELVRL1	ELVR1	R/W
00005F _H	EXTINT1 - External Interrupt Level Select High	ELVRH1		R/W
000060 _H	RLT0 - Timer Control Status Register Low	TMCSRL0	TMCSR0	R/W
000061 _H	RLT0 - Timer Control Status Register High	TMCSRH0		R/W
000062 _H	RLT0 - Reload Register - for writing		TMRLR0	W
000062 _H	RLT0 - Reload Register - for reading		TMR0	R
000063 _H	RLT0 - Reload Register - for writing			W
000063 _H	RLT0 - Reload Register - for reading			R
000064 _H	RLT1 - Timer Control Status Register Low	TMCSRL1	TMCSR1	R/W
000065 _H	RLT1 - Timer Control Status Register High	TMCSRH1		R/W
000066 _H	RLT1 - Reload Register - for writing		TMRLR1	W
000066 _H	RLT1 - Reload Register - for reading		TMR1	R
000067 _H	RLT1 - Reload Register - for writing			W

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000382 _H	DMA2 - Interrupt select	DISEL2		R/W
000383 _H	DMA3 - Interrupt select	DISEL3		R/W
000384 _H	DMA4 - Interrupt select	DISEL4		R/W
000385 _H	DMA5 - Interrupt select	DISEL5		R/W
000386 _H -00038F _H	Reserved			-
000390 _H	DMA - Status register low byte	DSRL	DSR	R/W
000391 _H	DMA - Status register high byte	DSRH		R/W
000392 _H	DMA - Stop status register low byte	DSSRL	DSSR	R/W
000393 _H	DMA - Stop status register high byte	DSSRH		R/W
000394 _H	DMA - Enable register low byte	DERL	DER	R/W
000395 _H	DMA - Enable register high byte	DERH		R/W
000396 _H -00039F _H	Reserved			-
0003A0 _H	Interrupt level register	ILR	ICR	R/W
0003A1 _H	Interrupt index register	IDX		R/W
0003A2 _H	Interrupt vector table base register Low	TBRL	TBR	R/W
0003A3 _H	Interrupt vector table base register High	TBRH		R/W
0003A4 _H	Delayed Interrupt register	DIRR		R/W
0003A5 _H	Non Maskable Interrupt register	NMI		R/W
0003A6 _H -0003AB _H	Reserved			-
0003AC _H	EDSU communication interrupt selection Low	EDSU2L	EDSU2	R/W
0003AD _H	EDSU communication interrupt selection High	EDSU2H		R/W
0003AE _H	ROM mirror control register	ROMM		R/W
0003AF _H	EDSU configuration register	EDSU		R/W
0003B0 _H	Memory patch control/status register ch 0/1		PFCS0	R/W
0003B1 _H	Memory patch control/status register ch 0/1			R/W
0003B2 _H	Memory patch control/status register ch 2/3		PFCS1	R/W
0003B3 _H	Memory patch control/status register ch 2/3			R/W
0003B4 _H	Memory patch control/status register ch 4/5		PFCS2	R/W
0003B5 _H	Memory patch control/status register ch 4/5			R/W
0003B6 _H	Memory patch control/status register ch 6/7		PFCS3	R/W
0003B7 _H	Memory patch control/status register ch 6/7			R/W
0003B8 _H	Memory Patch function - Patch address 0 low	PFAL0		R/W

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0004E3 _H	RTC - Second Register	WTSR		R/W
0004E4 _H	RTC - Minutes	WTMR		R/W
0004E5 _H	RTC - Hour	WTHR		R/W
0004E6 _H	RTC - Timer Control Extended Register	WTCER		R/W
0004E7 _H	RTC - Clock select register	WTCKSR		R/W
0004E8 _H	RTC - Timer Control Register Low	WTCRL	WTCR	R/W
0004E9 _H	RTC - Timer Control Register High	WTCRH		R/W
0004EA _H	CAL - Calibration unit Control register	CUCR		R/W
0004EB _H	Reserved			-
0004EC _H	CAL - Duration Timer Data Register Low	CUTDL	CUTD	R/W
0004ED _H	CAL - Duration Timer Data Register High	CUTDH		R/W
0004EE _H	CAL - Calibration Timer Register 2 Low	CUTR2L	CUTR2	R
0004EF _H	CAL - Calibration Timer Register 2 High	CUTR2H		R
0004F0 _H	CAL - Calibration Timer Register 1 Low	CUTR1L	CUTR1	R
0004F1 _H	CAL - Calibration Timer Register 1 High	CUTR1H		R
0004F2 _H -0004F9 _H	Reserved			-
0004FA _H	RLT - Timer input select (for Cascading)	TMISR		R/W
0004FB _H -00053D _H	Reserved			-
00053E _H	USART7 - Serial Mode Register	SMR7		R/W
00053F _H	USART7 - Serial Control Register	SCR7		R/W
000540 _H	USART7 - Serial TX Register	TDR7		W
000540 _H	USART7 - Serial RX Register	RDR7		R
000541 _H	USART7 - Serial Status Register	SSR7		R/W
000542 _H	USART7 - Ext. Control/Com. Register	ECCR7		R/W
000543 _H	USART7 - Ext. Status Com. Register	ESCR7		R/W
000544 _H	USART7 - Baud Rate Generator Register Low	BGRL7	BGR7	R/W
000545 _H	USART7 - Baud Rate Generator Register High	BGRH7		R/W
000546 _H	USART7 - Extended Serial Interrupt Register	ESIR7		R/W
000547 _H	Reserved			-
000548 _H	USART8 - Serial Mode Register	SMR8		R/W
000549 _H	USART8 - Serial Control Register	SCR8		R/W
00054A _H	USART8 - Serial TX Register	TDR8		W

Table 5: Interrupt vector table MB96(F)34x

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
60	30C _H	ICU4	Yes	60	Input Capture Unit 4
61	308 _H	ICU5	Yes	61	Input Capture Unit 5
62	304 _H	ICU6	Yes	62	Input Capture Unit 6
63	300 _H	ICU7	Yes	63	Input Capture Unit 7
64	2FC _H	OCU0	Yes	64	Output Compare Unit 0
65	2F8 _H	OCU1	Yes	65	Output Compare Unit 1
66	2F4 _H	OCU2	Yes	66	Output Compare Unit 2
67	2F0 _H	OCU3	Yes	67	Output Compare Unit 3
68	2EC _H	OCU4	Yes	68	Output Compare Unit 4
69	2E8 _H	OCU5	Yes	69	Output Compare Unit 5
70	2E4 _H	OCU6	Yes	70	Output Compare Unit 6
71	2E0 _H	OCU7	Yes	71	Output Compare Unit 7
72	2DC _H	FRT0	Yes	72	Free Running Timer 0
73	2D8 _H	FRT1	Yes	73	Free Running Timer 1
74	2D4 _H	IIC0	Yes	74	I2C interface
75	2D0 _H	IIC1	Yes	75	I2C interface
76	2CC _H	ADC0	Yes	76	A/D Converter
77	2C8 _H	ALARM0	No	77	Alarm Comparator 0 (except MB96F345Dyy or MB96F345Fyy)
78	2C4 _H	ALARM1	No	78	Alarm Comparator 1 (except MB96F345Dyy or MB96F345Fyy)
79	2C0 _H	LINR0	Yes	79	LIN USART 0 RX
80	2BC _H	LINT0	Yes	80	LIN USART 0 TX
81	2B8 _H	LINR1	Yes	81	LIN USART 1 RX
82	2B4 _H	LINT1	Yes	82	LIN USART 1 TX
83	2B0 _H	LINR2	Yes	83	LIN USART 2 RX
84	2AC _H	LINT2	Yes	84	LIN USART 2 TX
85	2A8 _H	LINR3	Yes	85	LIN USART 3 RX
86	2A4 _H	LINT3	Yes	86	LIN USART 3 TX
87	2A0 _H	FLASH_A	No	87	Flash memory A (only Flash devices)
88	29C _H	FLASH_B	No	88	Flash memory B (only MB96F348T/H/C)
89	298 _H	LINR7	Yes	89	LIN USART 7 RX

13. Handling Devices

Special care is required for the following when handling the device:

- Latch-up prevention
- Unused pins handling
- External clock usage
- Unused sub clock signal
- Notes on PLL clock mode operation
- Power supply pins (V_{CC}/V_{SS})
- Crystal oscillator circuit
- Turn on sequence of power supply to A/D converter and analog inputs
- Pin handling when not using the A/D converter
- Notes on energization
- Stabilization of power supply voltage
- Serial communication
- Handling of Data Flash

13.1 Latch-up prevention

CMOS IC chips may suffer latch-up under the following conditions:

- A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V_{CC} pins and V_{SS} pins.
- The AV_{CC} power supply is applied before the V_{CC} voltage.

Latch-up may increase the power supply current dramatically, causing thermal damages to the device.

For the same reason, extra care is required to not let the analog power-supply voltage (AV_{CC} , $AVRH$) exceed the digital power-supply voltage.

13.2 Unused pins handling

Unused input pins can be left open when the input is disabled (corresponding bit of Port Input Enable register $PIER = 0$).

Leaving unused input pins open when the input is enabled may result in misbehavior and possible permanent damage of the device. They must therefore be pulled up or pulled down through resistors. To prevent latch-up, those resistors should be more than 2 k Ω .

Unused bidirectional pins can be set either to the output state and be then left open, or to the input state with either input disabled or external pull-up/pull-down resistor as described above.

13.3 External clock usage

The permitted frequency range of an external clock depends on the oscillator type and configuration. See [AC Characteristics](#) for detailed modes and frequency limits. Single and opposite phase external clocks must be connected as follows:

13.7 Crystal oscillator and ceramic resonator circuit

Noise at X0, X1 pins or X0A, X1A pins might cause abnormal operation. It is required to provide bypass capacitors with shortest possible distance to X0, X1 pins and X0A, X1A pins, crystal oscillator (or ceramic resonator) and ground lines, and, to the utmost effort, that the lines of oscillation circuit do not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board artwork surrounding X0, X1 pins and X0A, X1A pins with a ground area for stabilizing the operation.

It is highly recommended to evaluate the quartz/MCU or resonator/MCU system at the quartz or resonator manufacturer, especially when using low-Q resonators at higher frequencies.

13.8 Turn on sequence of power supply to A/D converter and analog inputs

It is required to turn the A/D converter power supply (AV_{CC} , $AVRH$, $AVRL$) and analog inputs (ANn) on after turning the digital power supply (V_{CC}) on.

It is also required to turn the digital power off after turning the A/D converter supply and analog inputs off. In this case, the voltage must not exceed $AVRH$ or AV_{CC} (turning the analog and digital power supplies simultaneously on or off is acceptable).

13.9 Pin handling when not using the A/D converter

It is required to connect the unused pins of the A/D converter as $AV_{CC} = V_{CC}$, $AV_{SS} = AVRH = AVRL = V_{SS}$.

13.10 Notes on Power-on

To prevent malfunction of the internal voltage regulator, supply voltage profile while turning the power supply on should be slower than $50\mu s$ from 0.2 V to 2.7 V.

13.11 Stabilization of power supply voltage

If the power supply voltage varies acutely even within the operation safety range of the V_{CC} power supply voltage, a malfunction may occur. The V_{CC} power supply voltage must therefore be stabilized. As stabilization guidelines, the power supply voltage must be stabilized in such a way that V_{CC} ripple fluctuations (peak to peak value) in the commercial frequencies (50 to 60 Hz) fall within 10% of the standard V_{CC} power supply voltage and the transient fluctuation rate becomes $0.1V/\mu s$ or less in instantaneous fluctuation for power supply switching.

13.12 Serial communication

There is a possibility to receive wrong data due to noise or other causes on the serial communication. Therefore, design a printed circuit board so as to avoid noise. Consider receiving of wrong data when designing the system. For example apply a checksum and retransmit the data if an error occurs.

13.13 Handling of Data Flash

The Data Flash requires different and additional control signals for parallel programming. Please check with your programming equipment maker for support of this interface.

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Permitted Power dissipation (Mask ROM devices) ^[4]	P_D	-	350	mW	$T_A=105^{\circ}\text{C}$
		-	360	mW	$T_A=125^{\circ}\text{C}$ [6]
Operating ambient temperature	T_A	0	+70	$^{\circ}\text{C}$	MB96V300B
		-40	+105		
		-40	+125		[6]
Storage temperature	T_{STG}	-55	+150	$^{\circ}\text{C}$	

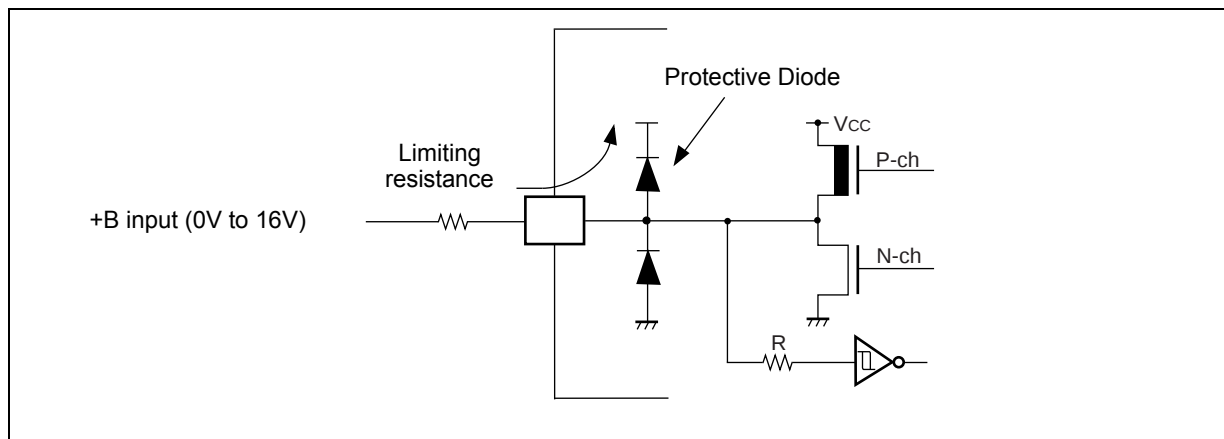
[1]: AV_{CC} and V_{CC} must be set to the same voltage. It is required that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} neither when the power is switched on.

[2]: V_I and V_O should not exceed $V_{CC} + 0.3\text{ V}$. V_I should also not exceed the specified ratings. However if the maximum current to/from a input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating. Input/output voltages of standard ports depend on V_{CC} .

[3]:

- Applicable to all general purpose I/O pins (Pnn_m)
- Use within recommended operating conditions.
- Use at DC voltage (current)
- The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the Power reset (except devices with persistent low voltage reset in internal vector mode).

Sample recommended circuits:

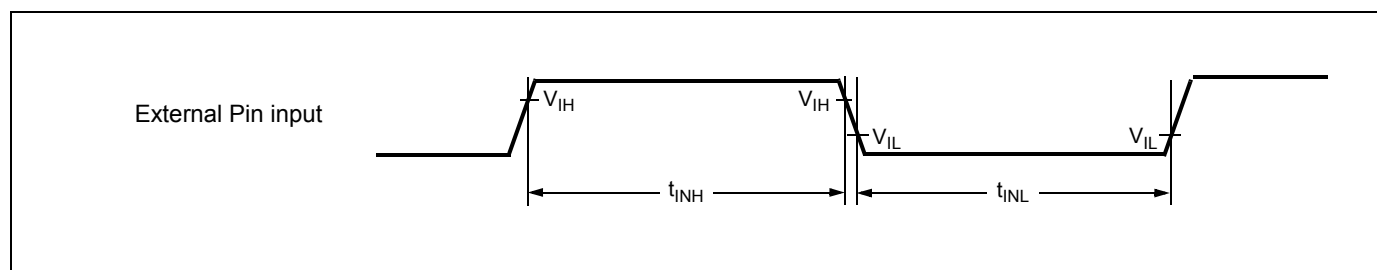


14.4.5 External Input timing

($T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = 0\text{V}$)

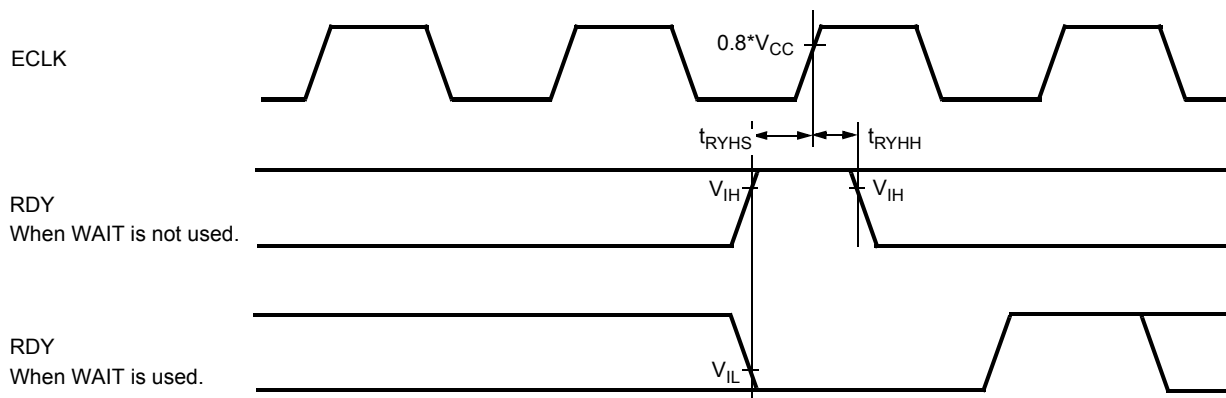
Parameter	Symbol	Pin	Condition	Value		Unit	Used Pin input function
				Min	Max		
Input pulse width	t_{INH} t_{INL}	INTn(_R)	-	200	-	ns	External Interrupt
		NMI(_R)					NMI
		Pnn_m		$2 \cdot t_{CLKP1} + 200$ ($t_{CLKP1} = 1/f_{CLKP1}$)	-	ns	General Purpose IO
		TINn(_R)					Reload Timer
		TTGn(_R)					PPG Trigger input
		ADTG(_R)					AD Converter Trigger
		FRCKn(_R)					Free Running Timer external clock
		INn(_R)					Input Capture

Note : Relocated Resource Inputs have same characteristics



14.4.6 External Bus timing

Note: The values given below are for an I/O driving strength $IO_{drive} = 5\text{mA}$. If IO_{drive} is 2mA , all the maximum output timing described in the different tables must then be increased by 10ns .



Refer to the Hardware Manual for detailed Timing Charts

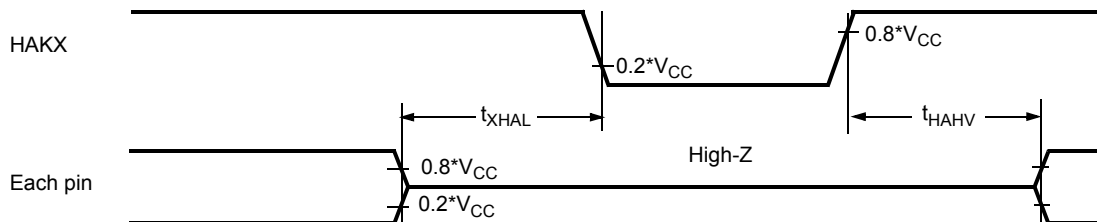
14.4.11 Hold Timing

(T_A = -40°C to +125°C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, I_{Odrive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min	Max		
Pin floating ⇒ HAKX ↓ time	t _{XHAL}	HAKX	-	t _{CYC} - 20	t _{CYC} + 20	ns	
HAKX ↑ time ⇒ Pin valid time	t _{HAHV}	HAKX		t _{CYC} - 20	t _{CYC} + 20	ns	

(T_A = -40°C to +125°C, V_{CC} = 3.0 to 4.5V, V_{SS} = 0.0 V, I_{Odrive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min	Max		
Pin floating ⇒ HAKX ↓ time	t _{XHAL}	HAKX	-	t _{CYC} - 25	t _{CYC} + 25	ns	
HAKX ↑ time ⇒ Pin valid time	t _{HAHV}	HAKX		t _{CYC} - 25	t _{CYC} + 25	ns	



Refer to the Hardware Manual for detailed Timing Charts

14.5 Analog Digital Converter

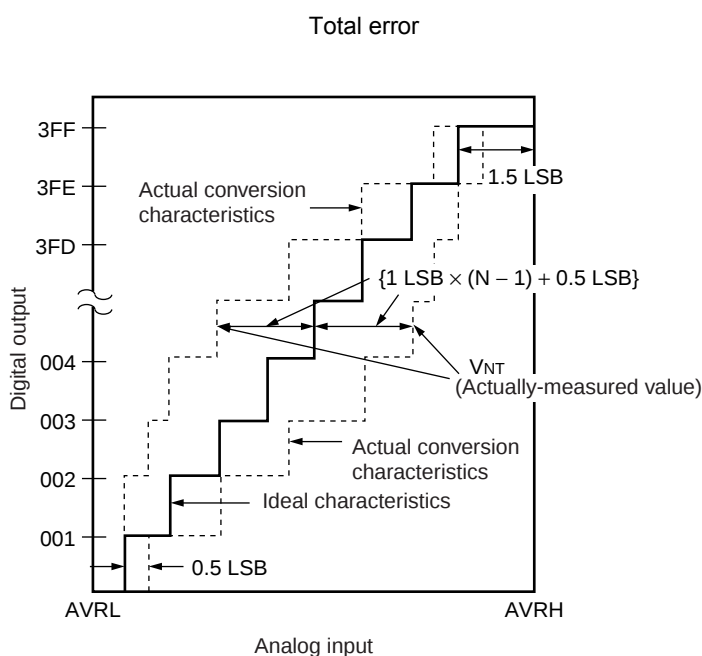
($T_A = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$, $3.0\text{ V} \leq \text{AVRH} - \text{AVRL}$, $V_{CC} = \text{AV}_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = \text{AV}_{SS} = 0\text{V}$)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	10	bit	
Total error	-	-	-3	-	+3	LSB	
Nonlinearity error	-	-	-2.5	-	+2.5	LSB	
Differential nonlinearity error	-	-	-1.9	-	+1.9	LSB	
Zero reading voltage	V_{OT}	ANn	$\text{AVRL} - 1.5\text{ LSB}$	$\text{AVRL} + 0.5\text{ LSB}$	$\text{AVRL} + 2.5\text{ LSB}$	V	
Full scale reading voltage	V_{FST}	ANn	$\text{AVRH} - 3.5\text{ LSB}$	$\text{AVRH} - 1.5\text{ LSB}$	$\text{AVRH} + 0.5\text{ LSB}$	V	
Compare time	-	-	1.0	-	16,500	μs	$4.5\text{V} \leq \text{AV}_{CC} \leq 5.5\text{V}$
			2.0	-	-	μs	$3.0\text{V} \leq \text{AV}_{CC} < 4.5\text{V}$
Sampling time	-	-	0.5	-	-	μs	$4.5\text{V} \leq \text{AV}_{CC} \leq 5.5\text{V}$
			1.2	-	-	μs	$3.0\text{V} \leq \text{AV}_{CC} < 4.5\text{V}$
Analog port input curren	I_{AIN}	ANn	-3	-	+3	μA	AV_{SS} , $\text{AVRL} < V_I < \text{AV}_{CC}$, AVRH
Analog port input curren	I_{AIN}	ANn	-1	-	+1	μA	$T_A = 25\text{ }^{\circ}\text{C}$, AV_{SS} , $\text{AVRL} < V_I < \text{AV}_{CC}$, AVRH
			-3	-	+3	μA	$T_A = 125\text{ }^{\circ}\text{C}$, AV_{SS} , $\text{AVRL} < V_I < \text{AV}_{CC}$, AVRH
Analog input voltage range	V_{AIN}	ANn	AVRL	-	AVRH	V	
Reference voltage range	AVRH	$\text{AVRH}/\text{AVRH} \cdot 2$	0.75 AV_{CC}	-	AV_{CC}	V	
	AVRL	AVRL	AV_{SS}	-	0.25 AV_{CC}	V	
Power supply current	I_A	AV_{CC}	-	2.5	5	mA	A/D Converter active
	I_{AH}	AV_{CC}	-	-	5	μA	A/D Converter not operated
Reference voltage current	I_R	AVRH/AVRL	-	0.7	1	mA	A/D Converter active
	I_{RH}	AVRH/AVRL	-	-	5	μA	A/D Converter not operated
Offset between input channels	-	ANn	-	-	4	LSB	

Note: The accuracy gets worse as $|\text{AVRH} - \text{AVRL}|$ becomes smaller.

14.5.1 Definition of A/D Converter Terms

- **Resolution:** Analog variation that is recognized by an A/D converter.
- **Total error:** Difference between the actual value and the ideal value. The total error includes zero transition error, full-scale transition error and nonlinearity error.
- **Nonlinearity error:** Deviation between a line across zero-transition line ("00 0000 0000" <--> "00 0000 0001") and full-scale transition line ("11 1111 1110" <--> "11 1111 1111") and actual conversion characteristics.
- **Differential nonlinearity error:** Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.
- **Zero reading voltage:** Input voltage which results in the minimum conversion value.
- **Full scale reading voltage:** Input voltage which results in the maximum conversion value.



$$\text{Total error of digital output "N"} = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + 0.5 \text{ LSB}\}}{1 \text{ LSB}} \quad [\text{LSB}]$$

$$1 \text{ LSB} = (\text{Ideal value}) \times \frac{AVRH - AVRL}{1024} \quad [\text{V}]$$

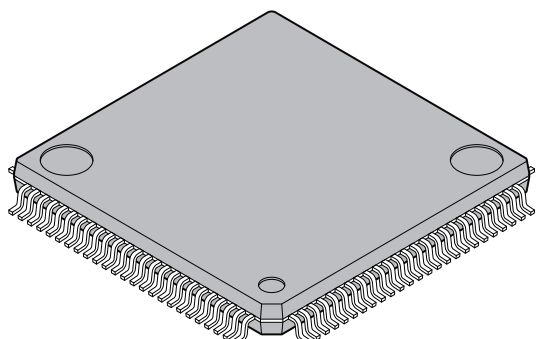
N: A/D converter digital output value

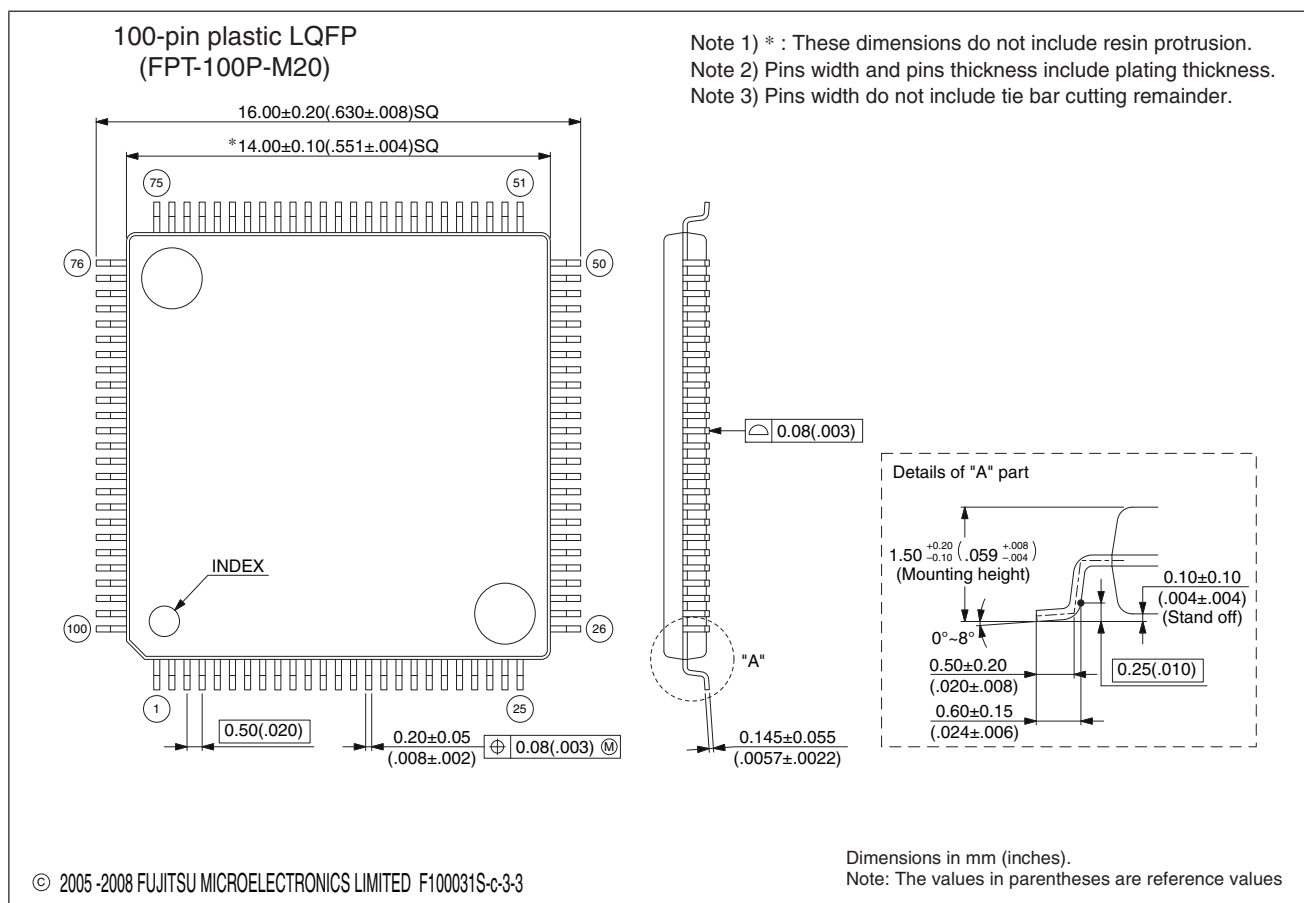
$$V_{OT} (\text{Ideal value}) = AVRL + 0.5 \text{ LSB} \quad [\text{V}]$$

$$V_{FST} (\text{Ideal value}) = AVRH - 1.5 \text{ LSB} \quad [\text{V}]$$

V_{NT}: A voltage at which digital output transitions from (N - 1) to N.

16. Package Dimension MB96(F)34x LQFP 100P

100-pin plastic LQFP  (FPT-100P-M20)	Lead pitch	0.50 mm
	Package width × package length	14.0 mm × 14.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm Max
	Weight	0.65 g
	Code (Reference)	P-LFQFP100-14×14-0.50



18.2 MCU without CAN Controller

Part number	Flash/ROM	Subclock	Package
MB96F346ASB PQC-GSE2	Flash A (288KB)	No	100 pin Plastic QFP (FPT-100P-M22)
MB96F346AWB PQC-GSE2		Yes	
MB96F346ASB PMC-GSE2		No	100 pin Plastic LQFP (FPT-100P-M20)
MB96F346AWB PMC-GSE2		Yes	
MB96F347ASB PQC-GSE2	Flash A (416KB)	No	100 pin Plastic QFP (FPT-100P-M22)
MB96F347AWB PQC-GSE2		Yes	
MB96F347ASB PMC-GSE2		No	100 pin Plastic LQFP (FPT-100P-M20)
MB96F347AWB PMC-GSE2		Yes	
MB96F348ASB PQC-GSE2	Flash A (544KB)	No	100 pin Plastic QFP (FPT-100P-M22)
MB96F348AWB PQC-GSE2		Yes	
MB96F348ASB PMC-GSE2		No	100 pin Plastic LQFP (FPT-100P-M20)
MB96F348AWB PMC-GSE2		Yes	
MB96F348CSC PQC-GSE2	Flash A (544KB) Flash B (32KB)	No	100 pin Plastic QFP (FPT-100P-M22)
MB96F348CWC PQC-GSE2		Yes	
MB96F348CSC PMC-GSE2		No	100 pin Plastic LQFP (FPT-100P-M20)
MB96F348CWC PMC-GSE2		Yes	

[1]: These devices are under development and specification is preliminary. These products under development may change its specification without notice.

This datasheet is also valid for the following outdated devices:

MB96F346YSA, MB96F346RSA, MB96F346YWA, MB96F346RWA,
 MB96F347YSA, MB96F347RSA, MB96F347YWA, MB96F347RWA,
 MB96F348YSA, MB96F348RSA, MB96F348YWA, MB96F348RWA,
 MB96F348TSB, MB96F348HSB, MB96F348TWB, MB96F348HWB,
 MB96F346ASA, MB96F346AWA,
 MB96F347ASA, MB96F347AWA,
 MB96F348ASA, MB96F348AWA,
 MB96F348CSB, MB96F348CWB

20. Main Changes in this Edition

Page	Section	Change Results
89	Electrical Characteristics 14.5. Analog Digital Converter	Corrected "Value" and "Unit" of Zero reading voltage. (AVRL - 1.5 → AVRL - 1.5 LSB AVRL + 0.5 → AVRL + 0.5 LSB AVRL + 2.5 → AVRL + 2.5 LSB LSB → V) Corrected "Value" and "Unit" of Full scale reading voltage. (AVRH - 3.5 → AVRH - 3.5 LSB AVRH - 1.5 → AVRH - 1.5 LSB AVRH + 0.5 → AVRH + 0.5 LSB LSB → V)

NOTE: Please see "Document History" for later revised information.

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	—	AKIH	06/17/2009	Migrated to Cypress and assigned document number 002-04579. No change to document contents or format.
*A	5198948	AKIH	04/04/2016	Updated to Cypress template