Infineon Technologies - MB96F346RWAPMC-GSE2 Datasheet

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Applications of "Embedded - Microcontrollers"

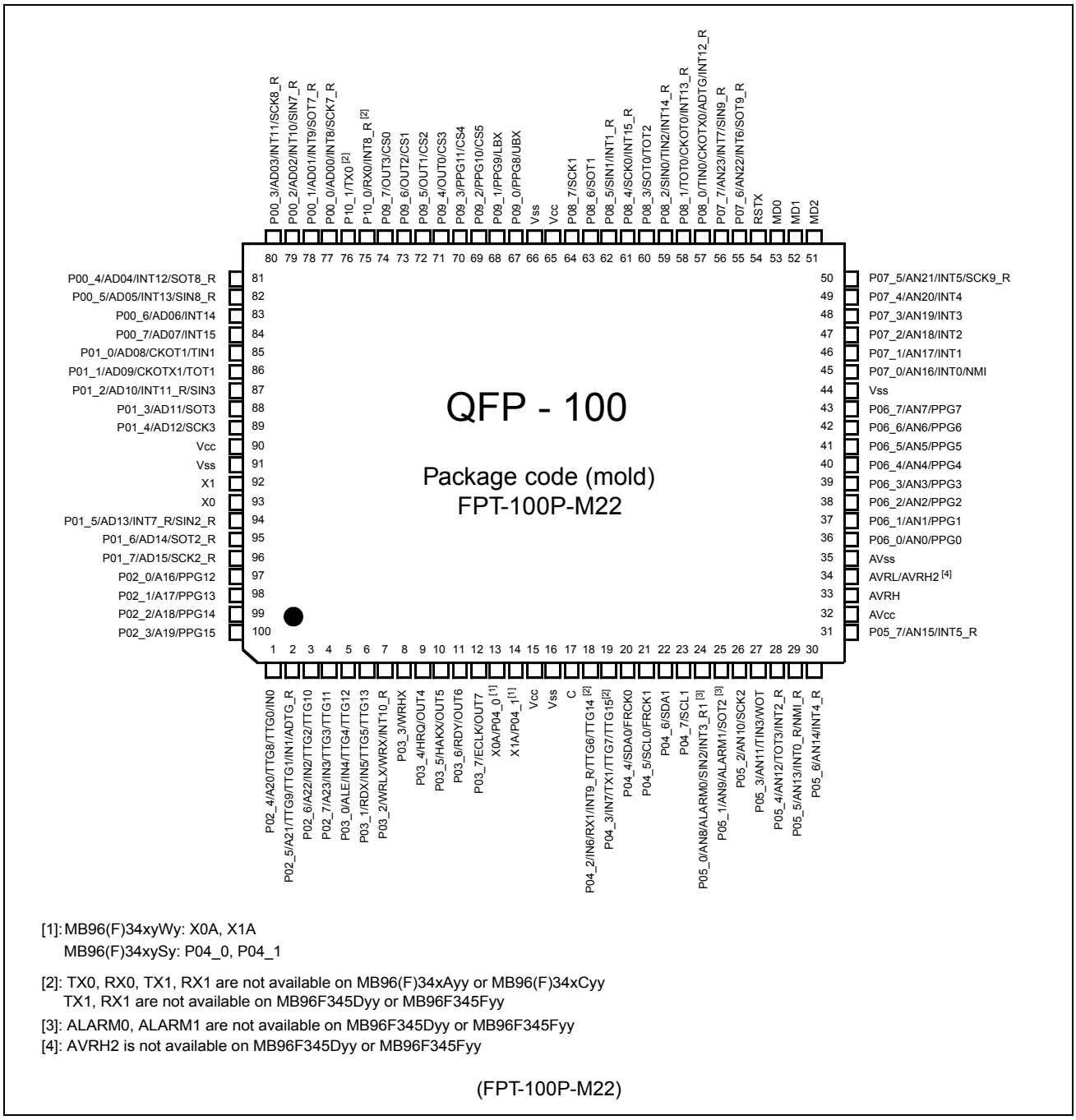
Details	
Product Status	Active
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	56MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, LVR, POR, PWM, WDT
Number of I/O	80
Program Memory Size	288KB (288K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f346rwapmc-gse2

1. Product Lineup

Features		MB96V300B	MB96(F)34x
Product type		Evaluation sample	Flash product: MB96F34x Mask ROM product: MB9634x
Product options			
YS		NA	Low voltage reset persistently on / Single clock
RS			Low voltage reset can be disabled / Single clock
YW			Low voltage reset persistently on / Dual clock
RW			Low voltage reset can be disabled / Dual clock
TS			indep. 32KB Flash / Low voltage reset persistently on / Single clock
HS			indep. 32KB Flash / Low voltage reset can be disabled / Single clock
TW			indep. 32KB Flash / Low voltage reset persistently on / Dual clock
HW			indep. 32KB Flash / Low voltage reset can be disabled / Dual clock
FS			64KB Data Flash / Low voltage reset persistently on / Single clock
DS			64KB Data Flash / Low voltage reset can be disabled / Single clock
FW			64KB Data Flash / Low voltage reset persistently on / Dual clock
DW			64KB Data Flash / Low voltage reset can be disabled / Dual clock
AS			No CAN / Low voltage reset can be disabled / Single clock devices
CS			No CAN / indep. 32KB Flash / Low voltage reset can be disabled / Single clock
AW			No CAN / Low voltage reset can be disabled / Dual clock
CW			No CAN / indep. 32KB Flash / Low voltage reset can be disabled / Dual clock
Flash/ROM	RAM		
160KB	8KB	ROM/Flash memory emulation by external RAM, 92KB internal RAM	MB96345Y [1], MB96345R [1]
224KB [Flash A: 160KB, Data Flash A: 64KB]	8KB		MB96F345F [1], MB96F345D [1]
288KB	16KB		MB96F346Y, MB96346Y [1], MB96F346R, MB96346R [1], MB96F346A
416KB	16KB		MB96F347Y, MB96F347R, MB96F347A
544KB	24KB		MB96F348Y, MB96F348R, MB96F348A
576KB [Flash A: 544KB, Flash B: 32KB]	24KB		MB96F348T, MB96F348H, MB96F348C
Package		BGA416	FPT-100P-M20 FPT-100P-M22
DMA		16 channels	6 channels
USART		10 channels	7 channels

3. Pin Assignments

Figure 2. Pin assignment of MB96(F)34x (FPT-100P-M22)



[1]: MB96(F)34xyWy: X0A, X1A
MB96(F)34xySy: P04_0, P04_1

[2]: TX0, RX0, TX1, RX1 are not available on MB96(F)34xAyy or MB96(F)34xCyy
TX1, RX1 are not available on MB96F345Dyy or MB96F345Fyy

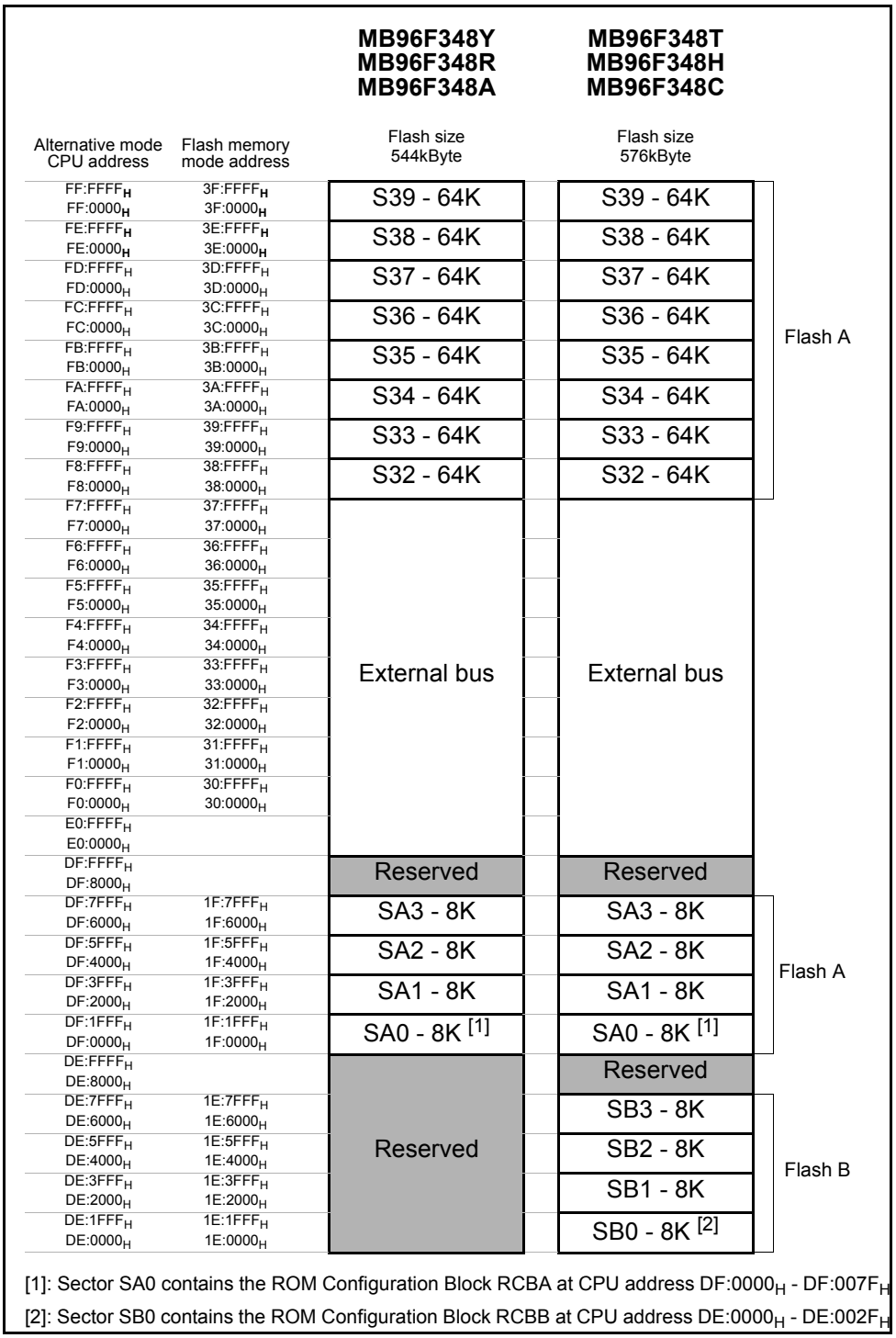
[3]: ALARM0, ALARM1 are not available on MB96F345Dyy or MB96F345Fyy

[4]: AVRH2 is not available on MB96F345Dyy or MB96F345Fyy

(FPT-100P-M22)

Remark:

MB96(F)34x products are pin-compatible to F^{2}MC-16LX family MB90340 series.



[1]: Sector SA0 contains the ROM Configuration Block RCBA at CPU address DF:0000$_H$ - DF:007F$_H$

[2]: Sector SB0 contains the ROM Configuration Block RCBB at CPU address DE:0000$_H$ - DE:002F$_H$

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$00004B_H$	ICU3 - Capture Register High	IPCPH3		R
$00004C_H$	ICU4/ICU5 - Control Status Register	ICS45		R/W
$00004D_H$	ICU4/ICU5 - Edge register	ICE45		R/W
$00004E_H$	ICU4 - Capture Register Low	IPCPL4	IPCP4	R
$00004F_H$	ICU4 - Capture Register High	IPCPH4		R
000050_H	ICU5 - Capture Register Low	IPCPL5	IPCP5	R
000051_H	ICU5 - Capture Register High	IPCPH5		R
000052_H	ICU6/ICU7 - Control Status Register	ICS67		R/W
000053_H	ICU6/ICU7 - Edge register	ICE67		R/W
000054_H	ICU6 - Capture Register Low	IPCPL6	IPCP6	R
000055_H	ICU6 - Capture Register High	IPCPH6		R
000056_H	ICU7 - Capture Register Low	IPCPL7	IPCP7	R
000057_H	ICU7 - Capture Register High	IPCPH7		R
000058_H	EXTINT0 - External Interrupt Enable Register	ENIR0		R/W
000059_H	EXTINT0 - External Interrupt Interrupt request Register	EIRR0		R/W
$00005A_H$	EXTINT0 - External Interrupt Level Select Low	ELVRL0	ELVR0	R/W
$00005B_H$	EXTINT0 - External Interrupt Level Select High	ELVRH0		R/W
$00005C_H$	EXTINT1 - External Interrupt Enable Register	ENIR1		R/W
$00005D_H$	EXTINT1 - External Interrupt Interrupt request Register	EIRR1		R/W
$00005E_H$	EXTINT1 - External Interrupt Level Select Low	ELVRL1	ELVR1	R/W
$00005F_H$	EXTINT1 - External Interrupt Level Select High	ELVRH1		R/W
000060_H	RLT0 - Timer Control Status Register Low	TMCSRL0	TMCSR0	R/W
000061_H	RLT0 - Timer Control Status Register High	TMCSRH0		R/W
000062_H	RLT0 - Reload Register - for writing		TMRLR0	W
000062_H	RLT0 - Reload Register - for reading		TMR0	R
000063_H	RLT0 - Reload Register - for writing			W
000063_H	RLT0 - Reload Register - for reading			R
000064_H	RLT1 - Timer Control Status Register Low	TMCSRL1	TMCSR1	R/W
000065_H	RLT1 - Timer Control Status Register High	TMCSRH1		R/W
000066_H	RLT1 - Reload Register - for writing		TMRLR1	W
000066_H	RLT1 - Reload Register - for reading		TMR1	R
000067_H	RLT1 - Reload Register - for writing			W

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$0000DE_H$	USART3 - Serial Mode Register	SMR3		R/W
$0000DF_H$	USART3 - Serial Control Register	SCR3		R/W
$0000E0_H$	USART3 - TX Register	TDR3		W
$0000E0_H$	USART3 - RX Register	RDR3		R
$0000E1_H$	USART3 - Serial Status	SSR3		R/W
$0000E2_H$	USART3 - Control/Com. Register	ECCR3		R/W
$0000E3_H$	USART3 - Ext. Status Register	ESCR3		R/W
$0000E4_H$	USART3 - Baud Rate Generator Register Low	BGRL3	BGR3	R/W
$0000E5_H$	USART3 - Baud Rate Generator Register High	BGRH3		R/W
$0000E6_H$	USART3 - Extended Serial Interrupt Register	ESIR3		R/W
$0000E7_H$-$0000EF_H$	Reserved			-
$0000F0_H$-$0000FF_H$	External Bus area	EXTBUS0		R/W
000100_H	DMA0 - Buffer address pointer low byte	BAPL0		R/W
000101_H	DMA0 - Buffer address pointer middle byte	BAPM0		R/W
000102_H	DMA0 - Buffer address pointer high byte	BAPH0		R/W
000103_H	DMA0 - DMA control register	DMACS0		R/W
000104_H	DMA0 - I/O register address pointer low byte	IOAL0	IOA0	R/W
000105_H	DMA0 - I/O register address pointer high byte	IOAH0		R/W
000106_H	DMA0 - Data counter low byte	DCTL0	DCT0	R/W
000107_H	DMA0 - Data counter high byte	DCTH0		R/W
000108_H	DMA1 - Buffer address pointer low byte	BAPL1		R/W
000109_H	DMA1 - Buffer address pointer middle byte	BAPM1		R/W
$00010A_H$	DMA1 - Buffer address pointer high byte	BAPH1		R/W
$00010B_H$	DMA1 - DMA control register	DMACS1		R/W
$00010C_H$	DMA1 - I/O register address pointer low byte	IOAL1	IOA1	R/W
$00010D_H$	DMA1 - I/O register address pointer high byte	IOAH1		R/W
$00010E_H$	DMA1 - Data counter low byte	DCTL1	DCT1	R/W
$00010F_H$	DMA1 - Data counter high byte	DCTH1		R/W
000110_H	DMA2 - Buffer address pointer low byte	BAPL2		R/W
000111_H	DMA2 - Buffer address pointer middle byte	BAPM2		R/W
000112_H	DMA2 - Buffer address pointer high byte	BAPH2		R/W
000113_H	DMA2 - DMA control register	DMACS2		R/W

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000473_H	I/O Port P07 - Extended Port Input Level Register	EPILR07		R/W
000474_H	I/O Port P08 - Extended Port Input Level Register	EPILR08		R/W
000475_H	I/O Port P09 - Extended Port Input Level Register	EPILR09		R/W
000476_H	I/O Port P10 - Extended Port Input Level Register	EPILR10		R/W
000477_H-$00047F_H$	Reserved			-
000480_H	I/O Port P00 - Port Output Drive Register	PODR00		R/W
000481_H	I/O Port P01 - Port Output Drive Register	PODR01		R/W
000482_H	I/O Port P02 - Port Output Drive Register	PODR02		R/W
000483_H	I/O Port P03 - Port Output Drive Register	PODR03		R/W
000484_H	I/O Port P04 - Port Output Drive Register	PODR04		R/W
000485_H	I/O Port P05 - Port Output Drive Register	PODR05		R/W
000486_H	I/O Port P06 - Port Output Drive Register	PODR06		R/W
000487_H	I/O Port P07 - Port Output Drive Register	PODR07		R/W
000488_H	I/O Port P08 - Port Output Drive Register	PODR08		R/W
000489_H	I/O Port P09 - Port Output Drive Register	PODR09		R/W
$00048A_H$	I/O Port P10 - Port Output Drive Register	PODR10		R/W
$00048B_H$-$00049B_H$	Reserved			-
$00049C_H$	I/O Port P08 - Port High Drive Register	PHDR08		R/W
$00049D_H$	I/O Port P09 - Port High Drive Register	PHDR09		R/W
$00049E_H$	I/O Port P10 - Port High Drive Register	PHDR10		R/W
$00049F_H$-$0004A7_H$	Reserved			-
$0004A8_H$	I/O Port P00 - Pull-Up resistor Control Register	PUCR00		R/W
$0004A9_H$	I/O Port P01 - Pull-Up resistor Control Register	PUCR01		R/W
$0004AA_H$	I/O Port P02 - Pull-Up resistor Control Register	PUCR02		R/W
$0004AB_H$	I/O Port P03 - Pull-Up resistor Control Register	PUCR03		R/W
$0004AC_H$	I/O Port P04 - Pull-Up resistor Control Register	PUCR04		R/W
$0004AD_H$	I/O Port P05 - Pull-Up resistor Control Register	PUCR05		R/W
$0004AE_H$	I/O Port P06 - Pull-Up resistor Control Register	PUCR06		R/W
$0004AF_H$	I/O Port P07 - Pull-Up resistor Control Register	PUCR07		R/W
$0004B0_H$	I/O Port P08 - Pull-Up resistor Control Register	PUCR08		R/W
$0004B1_H$	I/O Port P09 - Pull-Up resistor Control Register	PUCR09		R/W
$0004B2_H$	I/O Port P10 - Pull-Up resistor Control Register	PUCR10		R/W

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$00054A_H$	USART8 - Serial RX Register	RDR8		R
$00054B_H$	USART8 - Serial Status Register	SSR8		R/W
$00054C_H$	USART8 - Ext. Control/Com. Register	ECCR8		R/W
$00054D_H$	USART8 - Ext. Status Com. Register	ESCR8		R/W
$00054E_H$	USART8 - Baud Rate Generator Register Low	BGRL8	BGR8	R/W
$00054F_H$	USART8 - Baud Rate Generator Register High	BGRH8		R/W
000550_H	USART8 - Extended Serial Interrupt Register	ESIR8		R/W
000551_H	Reserved			-
000552_H	USART9 - Serial Mode Register	SMR9		R/W
000553_H	USART9 - Serial Control Register	SCR9		R/W
000554_H	USART9 - Serial TX Register	TDR9		W
000554_H	USART9 - Serial RX Register	RDR9		R
000555_H	USART9 - Serial Status Register	SSR9		R/W
000556_H	USART9 - Ext. Control/Com. Register	ECCR9		R/W
000557_H	USART9 - Ext. Status Com. Register	ESCR9		R/W
000558_H	USART9 - Baud Rate Generator Register Low	BGRL9	BGR9	R/W
000559_H	USART9 - Baud Rate Generator Register High	BGRH9		R/W
$00055A_H$	USART9 - Extended Serial Interrupt Register	ESIR9		R/W
$00055B_H$-$00055F_H$	Reserved			-
000560_H	ALARM0 - Control Status Register	ACSR0		R/W
000561_H	ALARM0 - Extended Control Status Register	AECSR0		R/W
000562_H	ALARM1 - Control Status Register	ACSR1		R/W
000563_H	ALARM1 - Extended Control Status Register	AECSR1		R/W
000564_H	PPG6 - Timer register		PTMR6	R
000565_H	PPG6 - Timer register			R
000566_H	PPG6 - Period setting register		PCSR6	W
000567_H	PPG6 - Period setting register			W
000568_H	PPG6 - Duty cycle register		PDUT6	W
000569_H	PPG6 - Duty cycle register			W
$00056A_H$	PPG6 - Control status register Low	PCNL6	PCN6	R/W
$00056B_H$	PPG6 - Control status register High	PCNH6		R/W
$00056C_H$	PPG7 - Timer register		PTMR7	R

Table 4: I/O map MB96(F)34x

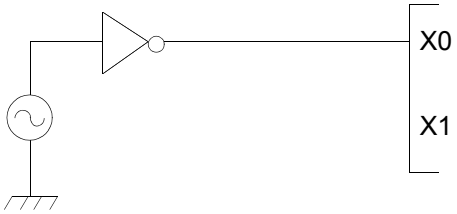
Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000715_H	CAN0 - IF1 Mask 1 Register High	IF1MSK1H0		R/W
000716_H	CAN0 - IF1 Mask 2 Register Low	IF1MSK2L0	IF1MSK20	R/W
000717_H	CAN0 - IF1 Mask 2 Register High	IF1MSK2H0		R/W
000718_H	CAN0 - IF1 Arbitration 1 Register Low	IF1ARB1L0	IF1ARB10	R/W
000719_H	CAN0 - IF1 Arbitration 1 Register High	IF1ARB1H0		R/W
$00071A_H$	CAN0 - IF1 Arbitration 2 Register Low	IF1ARB2L0	IF1ARB20	R/W
$00071B_H$	CAN0 - IF1 Arbitration 2 Register High	IF1ARB2H0		R/W
$00071C_H$	CAN0 - IF1 Message Control Register Low	IF1MCTRL0	IF1MCTR0	R/W
$00071D_H$	CAN0 - IF1 Message Control Register High	IF1MCTRH0		R/W
$00071E_H$	CAN0 - IF1 Data A1 Low	IF1DTA1L0	IF1DTA10	R/W
$00071F_H$	CAN0 - IF1 Data A1 High	IF1DTA1H0		R/W
000720_H	CAN0 - IF1 Data A2 Low	IF1DTA2L0	IF1DTA20	R/W
000721_H	CAN0 - IF1 Data A2 High	IF1DTA2H0		R/W
000722_H	CAN0 - IF1 Data B1 Low	IF1DTB1L0	IF1DTB10	R/W
000723_H	CAN0 - IF1 Data B1 High	IF1DTB1H0		R/W
000724_H	CAN0 - IF1 Data B2 Low	IF1DTB2L0	IF1DTB20	R/W
000725_H	CAN0 - IF1 Data B2 High	IF1DTB2H0		R/W
000726_H-$00073F_H$	Reserved			-
000740_H	CAN0 - IF2 Command request register Low	IF2CREQL0	IF2CREQ0	R/W
000741_H	CAN0 - IF2 Command request register High	IF2CREQH0		R/W
000742_H	CAN0 - IF2 Command Mask register Low	IF2CMSKL0	IF2CMSK0	R/W
000743_H	CAN0 - IF2 Command Mask register High (reserved)	IF2CMSKH0		R
000744_H	CAN0 - IF2 Mask 1 Register Low	IF2MSK1L0	IF2MSK10	R/W
000745_H	CAN0 - IF2 Mask 1 Register High	IF2MSK1H0		R/W
000746_H	CAN0 - IF2 Mask 2 Register Low	IF2MSK2L0	IF2MSK20	R/W
000747_H	CAN0 - IF2 Mask 2 Register High	IF2MSK2H0		R/W
000748_H	CAN0 - IF2 Arbitration 1 Register Low	IF2ARB1L0	IF2ARB10	R/W
000749_H	CAN0 - IF2 Arbitration 1 Register High	IF2ARB1H0		R/W
$00074A_H$	CAN0 - IF2 Arbitration 2 Register Low	IF2ARB2L0	IF2ARB20	R/W
$00074B_H$	CAN0 - IF2 Arbitration 2 Register High	IF2ARB2H0		R/W
$00074C_H$	CAN0 - IF2 Message Control Register Low	IF2MCTRL0	IF2MCTR0	R/W
$00074D_H$	CAN0 - IF2 Message Control Register High	IF2MCTRH0		R/W

Table 5: Interrupt vector table MB96(F)34x

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
60	$30C_H$	ICU4	Yes	60	Input Capture Unit 4
61	308_H	ICU5	Yes	61	Input Capture Unit 5
62	304_H	ICU6	Yes	62	Input Capture Unit 6
63	300_H	ICU7	Yes	63	Input Capture Unit 7
64	$2FC_H$	OCU0	Yes	64	Output Compare Unit 0
65	$2F8_H$	OCU1	Yes	65	Output Compare Unit 1
66	$2F4_H$	OCU2	Yes	66	Output Compare Unit 2
67	$2F0_H$	OCU3	Yes	67	Output Compare Unit 3
68	$2EC_H$	OCU4	Yes	68	Output Compare Unit 4
69	$2E8_H$	OCU5	Yes	69	Output Compare Unit 5
70	$2E4_H$	OCU6	Yes	70	Output Compare Unit 6
71	$2E0_H$	OCU7	Yes	71	Output Compare Unit 7
72	$2DC_H$	FRT0	Yes	72	Free Running Timer 0
73	$2D8_H$	FRT1	Yes	73	Free Running Timer 1
74	$2D4_H$	IIC0	Yes	74	I2C interface
75	$2D0_H$	IIC1	Yes	75	I2C interface
76	$2CC_H$	ADC0	Yes	76	A/D Converter
77	$2C8_H$	ALARM0	No	77	Alarm Comparator 0 (except MB96F345Dyy or MB96F345Fyy)
78	$2C4_H$	ALARM1	No	78	Alarm Comparator 1 (except MB96F345Dyy or MB96F345Fyy)
79	$2C0_H$	LINR0	Yes	79	LIN USART 0 RX
80	$2BC_H$	LINT0	Yes	80	LIN USART 0 TX
81	$2B8_H$	LINR1	Yes	81	LIN USART 1 RX
82	$2B4_H$	LINT1	Yes	82	LIN USART 1 TX
83	$2B0_H$	LINR2	Yes	83	LIN USART 2 RX
84	$2AC_H$	LINT2	Yes	84	LIN USART 2 TX
85	$2A8_H$	LINR3	Yes	85	LIN USART 3 RX
86	$2A4_H$	LINT3	Yes	86	LIN USART 3 TX
87	$2A0_H$	FLASH_A	No	87	Flash memory A (only Flash devices)
88	$29C_H$	FLASH_B	No	88	Flash memory B (only MB96F348T/H/C)
89	298_H	LINR7	Yes	89	LIN USART 7 RX

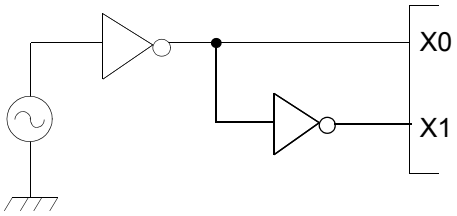
13.3.1 Single phase external clock

■ When using a single phase external clock, X0 pin must be driven and X1 pin left open.



13.3.2 Opposite phase external clock

■ When using an opposite phase external clock, X1 (X1A) must be supplied with a clock signal which has the opposite phase to the X0 (X0A) pins.



13.4 Unused sub clock signal

If the pins X0A and X1A are not connected to an oscillator, a pull-down resistor must be connected on the X0A pin and the X1A pin must be left open.

13.5 Notes on PLL clock mode operation

If the PLL clock mode is selected and no external oscillator is operating or no external clock is supplied, the microcontroller attempts to work with the free oscillating PLL. Performance of this operation, however, cannot be guaranteed.

13.6 Power supply pins (V_{CC}/v_{SS})

It is required that all V_{CC}-level as well as all V_{SS}-level power supply pins are at the same potential. If there is more than one V_{CC} or V_{SS} level, the device may operate incorrectly or be damaged even within the guaranteed operating range.

V_{CC} and V_{SS} must be connected to the device from the power supply with lowest possible impedance.

As a measure against power supply noise, it is required to connect a bypass capacitor of about 0.1 μF between V_{CC} and V_{SS} as close as possible to V_{CC} and V_{SS} pins.

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Permitted Power dissipation (Mask ROM devices) [4]	P_D	-	350	mW	T_A=105°C
		-	360	mW	T_A=125°C [6]
Operating ambient temperature	T_A	0	+70	°C	MB96V300B
		-40	+105		
		-40	+125		[6]
Storage temperature	T_{STG}	-55	+150	°C	

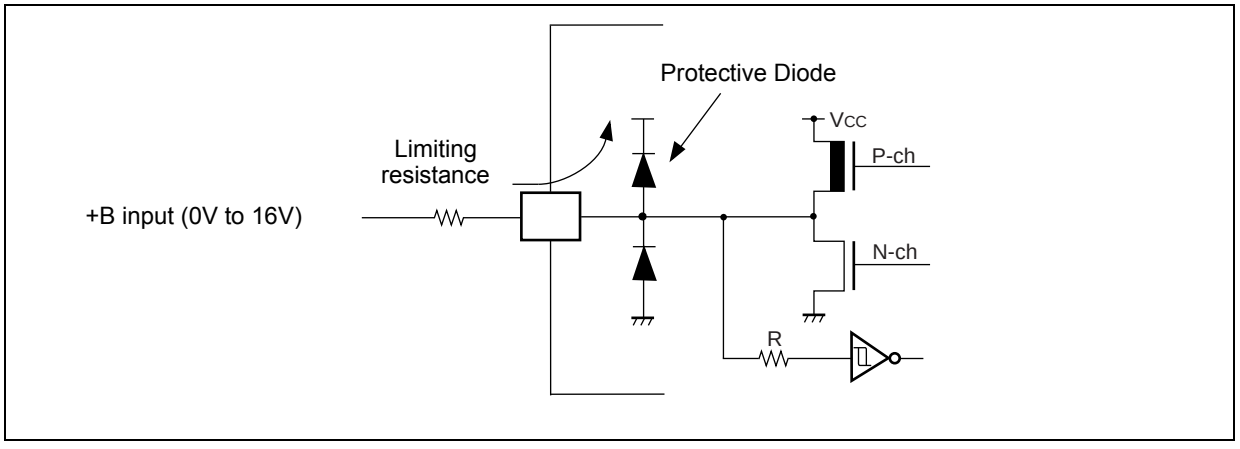
[1]: AV_{CC} and V_{CC} must be set to the same voltage. It is required that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} neither when the power is switched on.

[2]: V_I and V_O should not exceed V_{CC} + 0.3 V. V_I should also not exceed the specified ratings. However if the maximum current to/from a input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating. Input/output voltages of standard ports depend on V_{CC}.

[3]:

- Applicable to all general purpose I/O pins (Pnn_m)
- Use within recommended operating conditions.
- Use at DC voltage (current)
- The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the Power reset (except devices with persistent low voltage reset in internal vector mode).

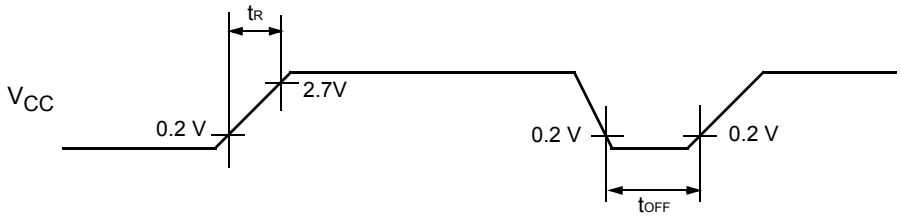
Sample recommended circuits:



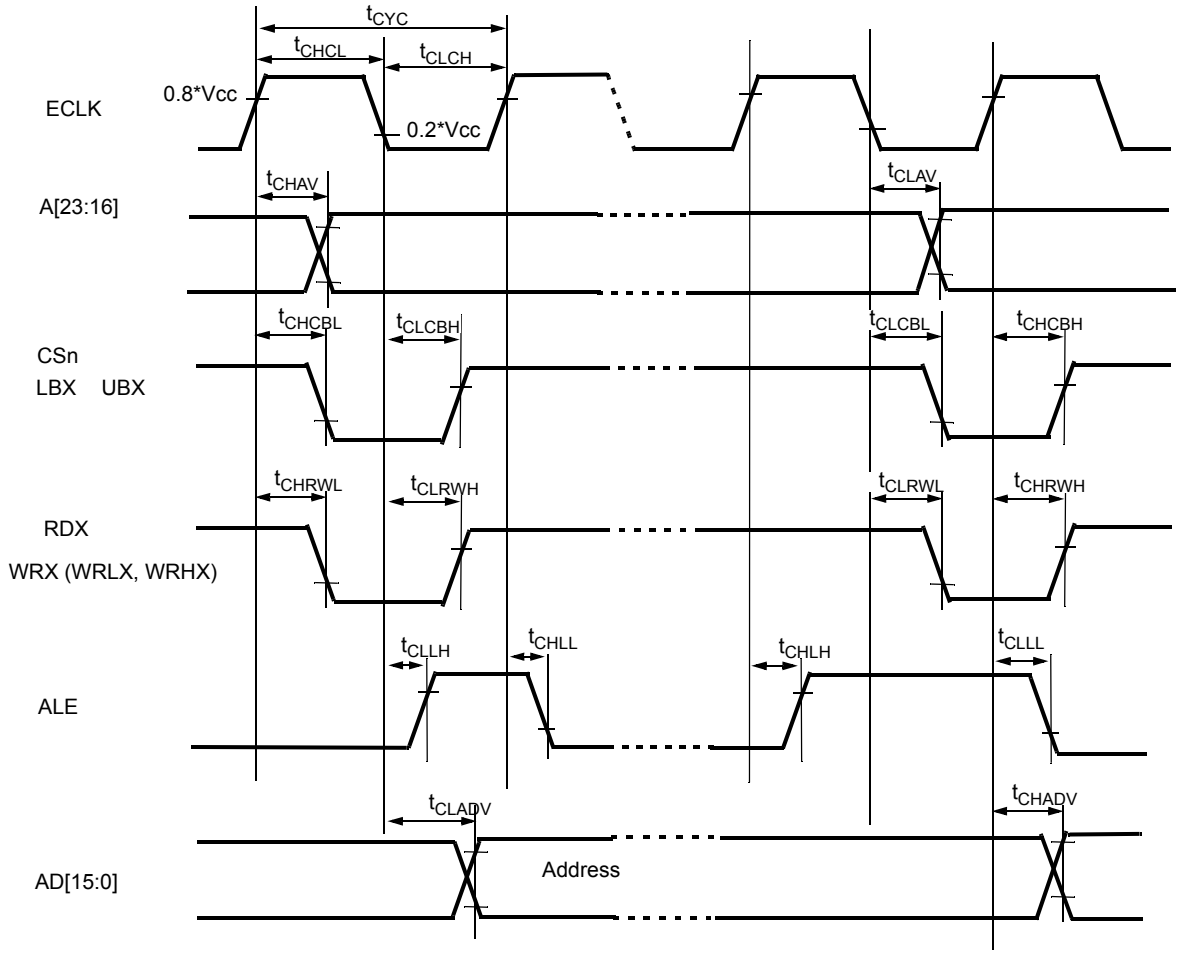
14.4.4 Power On Reset timing

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

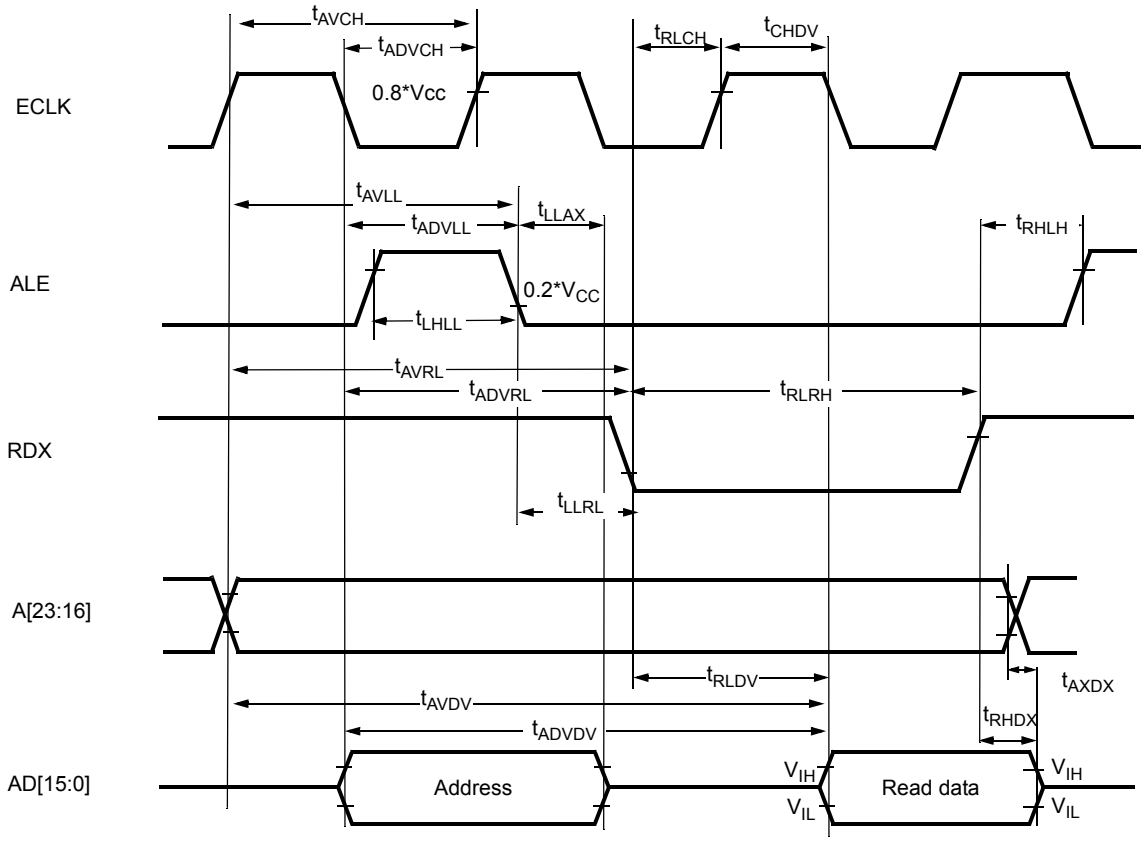
Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Power on rise time	t_R	Vcc	0.05	-	30	ms	
Power off time	t_{OFF}	Vcc	1	-	-	ms	



If the power supply is changed too rapidly, a power-on reset may occur.
We recommend a smooth startup by restraining voltages when changing the power supply voltage during operation, as shown in the figure below.



Refer to the Hardware Manual for detailed Timing Charts



Refer to the Hardware Manual for detailed Timing Charts

14.4.9 Bus Timing (Write)

(T_A = –40°C to +125°C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Valid address ⇒ WRX ↓ time	t_{AVWL}	WRX, WRLX, WRHX, A[23:16]	EACL:ACE=0	$3t_{CYC}/2 - 15$	-	ns	
			EACL:ACE=1	$5t_{CYC}/2 - 15$	-		
	t_{ADVWL}	WRX, WRLX, WRHX, AD[15:0]	EACL:ACE=0	$t_{CYC} - 15$	-	ns	
			EACL:ACE=1	$2t_{CYC} - 15$	-		
WRX pulse width	t_{WLWH}	WRX, WRXL, WRHX	-	$t_{CYC} - 5$	-	ns	w/o cycle extension
Valid data output ⇒ WRX ↑ time	t_{DVWH}	WRX, WRLX, WRHX, AD[15:0]	-	$t_{CYC} - 20$	-	ns	w/o cycle extension
WRX ↑ ⇒ Data hold time	t_{WHDX}	WRX, WRLX, WRHX, AD[15:0]	-	$t_{CYC}/2 - 15$	-	ns	
WRX ↑ ⇒ Address valid time	t_{WHAX}	WRX, WRLX, WRHX, A[23:16]	-	$t_{CYC}/2 - 15$	-	ns	
WRX ↑ ⇒ ALE ↑ time	t_{WHLH}	WRX, WRLX, WRHX, ALE	EBM:ACE=1 and EACL:STS=1	$2t_{CYC} - 10$	-	ns	
			other EBM:ACE and EACL:STS setting	$t_{CYC} - 10$	-		
WRX ↓ ⇒ ECLK ↑ time	t_{WLCH}	WRX, WRLX, WRHX, ECLK	-	$t_{CYC}/2 - 10$	-	ns	
CSn ⇒ WRX time	t_{CSLWL}	WRX, WRLX, WRHX, CSn	EACL:ACE=0	-	$3t_{CYC}/2 - 15$	ns	
			EACL:ACE=1	-	$5t_{CYC}/2 - 15$		
WRX ⇒ CSn time	t_{WHCSH}	WRX, WRLX, WRHX, CSn	-	$t_{CYC}/2 - 15$	-	ns	

(T_A = –40°C to +125°C, V_{CC} = 3.0 to 4.5V, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Valid address ⇒ WRX ↓ time	t_{AVWL}	WRX, WRLX, WRHX, A[23:16]	EACL:ACE=0	$3t_{CYC}/2 - 20$	-	ns	
			EACL:ACE=1	$5t_{CYC}/2 - 20$	-		
	t_{ADVWL}	WRX, WRLX, WRHX, AD[15:0]	EACL:ACE=0	$t_{CYC} - 20$	-	ns	
			EACL:ACE=1	$2t_{CYC} - 20$	-		

14.4.12 USART timing

WARNING: The values given below are for an I/O driving strength IO_{drive} = 5mA. If IO_{drive} is 2mA, all the maximum output timing described in the different tables must then be increased by 10ns.

(T_A = -40°C to 125°C, V_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Condition	V_{CC} = AV_{CC}= 4.5V to 5.5V		V_{CC} = AV_{CC}= 3.0V to 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYCI}	SCKn	Internal Shift Clock Mode	4 t_{CLKP1}	-	4 t_{CLKP1}	-	ns
SCK ↓→ SOT delay time	t_{SLOVI}	SCKn, SOTn		-20	+20	-30	+30	ns
SOT → SCK ↑ delay time	t_{OVSHI}	SCKn, SOTn		N*t_{CLKP1} - 20 [1]	-	N*t_{CLKP1} - 30 [1]	-	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCKn, SINn		t_{CLKP1} + 45	-	t_{CLKP1} + 55	-	ns
SCK ↑→ Valid SIN hold time	t_{SHIXI}	SCKn, SINn		0	-	0	-	ns
Serial clock “L” pulse width	t_{SLSHE}	SCKn	External Shift Clock Mode	t_{CLKP1} + 10	-	t_{CLKP1} + 10	-	ns
Serial clock “H” pulse width	t_{SHSLE}	SCKn		t_{CLKP1} + 10	-	t_{CLKP1} + 10	-	ns
SCK ↓→ SOT delay time	t_{SLOVE}	SCKn, SOTn		-	2 t_{CLKP1} + 45	-	2 t_{CLKP1} + 55	ns
Valid SIN → SCK ↑	t_{IVSHE}	SCKn, SINn		t_{CLKP1}/2 + 10	-	t_{CLKP1}/2 + 10	-	ns
SCK ↑→ Valid SIN hold time	t_{SHIXE}	SCKn, SINn		t_{CLKP1} + 10	-	t_{CLKP1} + 10	-	ns
SCK fall time	t_{FE}	SCKn		-	20	-	20	ns
SCK rise time	t_{RE}	SCKn		-	20	-	20	ns

Notes:

- AC characteristic in CLK synchronized mode.
- C_L is the load capacity value of pins when testing.
- Depending on the used machine clock frequency, the maximum possible baud rate can be limited by some parameters. These parameters are shown in “MB96300 Super series HARDWARE MANUAL”.
- t_{CLKP1} is the cycle time of the peripheral clock 1 (CLKP1), Unit : ns

[1]: Parameter N depends on t_{SCYCI} and can be calculated as follows:

- if t_{SCYCI} = 2*k*t_{CLKP1}, then N = k, where k is an integer > 2
- if t_{SCYCI} = (2*k+1)*t_{CLKP1}, then N = k+1, where k is an integer > 1

Examples:

t_{SCYCI}	N
4*t_{CLKP1}	2
5*t_{CLKP1},	3
7*t_{CLKP1},	4
...	...

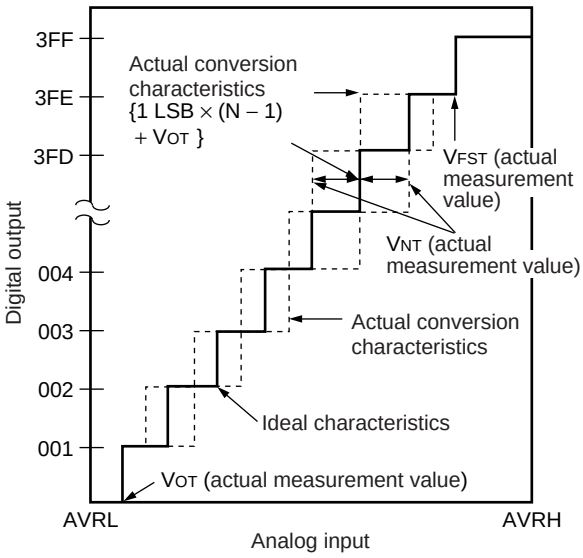
14.5 Analog Digital Converter

(T_A = -40 °C to +125 °C, 3.0 V ≤ AVRH - AVRL, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

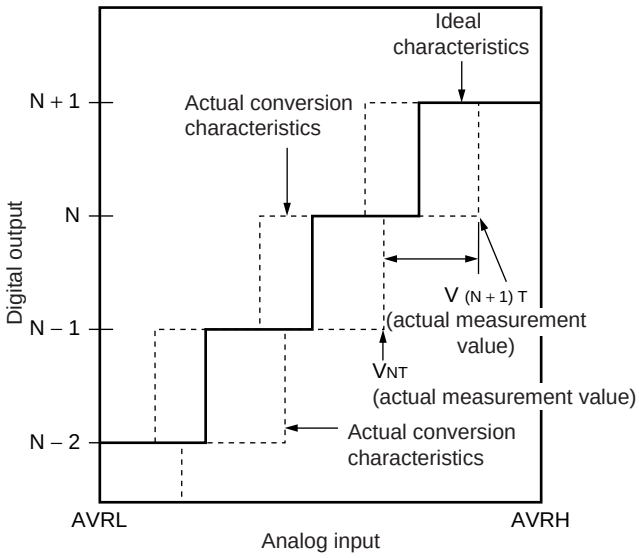
Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	10	bit	
Total error	-	-	-3	-	+3	LSB	
Nonlinearity error	-	-	-2.5	-	+2.5	LSB	
Differential nonlinearity error	-	-	-1.9	-	+1.9	LSB	
Zero reading voltage	V_{OT}	ANn	AVRL - 1.5 LSB	AVRL+ 0.5 LSB	AVRL + 2.5 LSB	V	
Full scale reading voltage	V_{FST}	ANn	AVRH - 3.5 LSB	AVRH - 1.5 LSB	AVRH + 0.5 LSB	V	
Compare time	-	-	1.0	-	16,500	µs	4.5V ≤ AV_{CC} ≤ 5.5V
			2.0	-	-	µs	3.0V ≤ AV_{CC} < 4.5V
Sampling time	-	-	0.5	-	-	µs	4.5V ≤ AV_{CC} ≤ 5.5V
			1.2	-	-	µs	3.0V ≤ AV_{CC} < 4.5V
Analog port input curren	I_{AIN}	ANn	-3	-	+3	µA	AV_{SS}, AVRL < V_I < AV_{CC}, AVRH
Analog port input curren	I_{AIN}	ANn	-1	-	+1	µA	T_A = 25 °C, AV_{SS}, AVRL < V_I < AV_{CC}, AVRH
			-3	-	+3	µA	T_A = 125 °C,AV_{SS}, AVRL < V_I < AV_{CC}, AVRH
Analog input voltage range	V_{AIN}	ANn	AVRL	-	AVRH	V	
Reference voltage range	AVRH	AVRH/ AVRH 2	0.75 AVcc	-	AVcc	V	
	AVRL	AVRL	AV_{SS}	-	0.25 AV_{CC}	V	
Power supply current	I_A	AVcc	-	2.5	5	mA	A/D Converter active
	I_{AH}	AVcc	-	-	5	µA	A/D Converter not operated
Reference voltage current	I_R	AVRH/ AVRL	-	0.7	1	mA	A/D Converter active
	I_{RH}	AVRH/ AVRL	-	-	5	µA	A/D Converter not operated
Offset between input channels	-	ANn	-	-	4	LSB	

Note: The accuracy gets worse as |AVRH - AVRL| becomes smaller.

Nonlinearity error



Differential nonlinearity error



$$\text{Nonlinearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

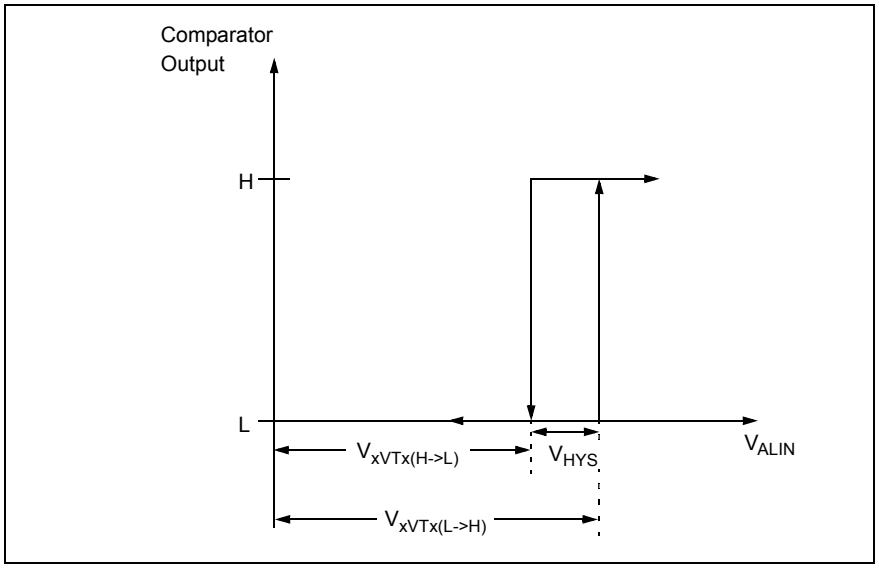
$$\text{Differential nonlinearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\text{LSB}\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

N: A/D converter digital output value

V_{OT}: Voltage at which digital output transits from "000_H" to "001_H."

V_{FST}: Voltage at which digital output transits from "$3FE_H$" to "$\#FF_H$."


Comparator
Output
H
L
$V_{xVTx(H->L)}$
V_{HYS}
V_{ALIN}
$V_{xVTx(L->H)}$

18.1 MCU with CAN Controller

Part number	Flash/ROM	Subclock	Persistent Low Voltage Reset	Package
MB96F347YSB PQC-GSE2	Flash A (416KB)	No	Yes	100 pin Plastic QFP (FPT-100P-M22)
MB96F347RSB PQC-GSE2			No	
MB96F347YWB PQC-GSE2		Yes	Yes	
MB96F347RWB PQC-GSE2			No	
MB96F347YSB PMC-GSE2		No	Yes	100 pin Plastic LQFP (FPT-100P-M20)
MB96F347RSB PMC-GSE2			No	
MB96F347YWB PMC-GSE2		Yes	Yes	
MB96F347RWB PMC-GSE2			No	
MB96F348YSB PQC-GSE2	Flash A (544KB)	No	Yes	100 pin Plastic QFP (FPT-100P-M22)
MB96F348RSB PQC-GSE2			No	
MB96F348YWB PQC-GSE2		Yes	Yes	
MB96F348RWB PQC-GSE2			No	
MB96F348YSB PMC-GSE2		No	Yes	100 pin Plastic LQFP (FPT-100P-M20)
MB96F348RSB PMC-GSE2			No	
MB96F348YWB PMC-GSE2		Yes	Yes	
MB96F348RWB PMC-GSE2			No	
MB96F348TSC PQC-GSE2	Flash A (544KB) Flash B (32KB)	No	Yes	100 pin Plastic QFP (FPT-100P-M22)
MB96F348HSC PQC-GSE2			No	
MB96F348TWC PQC-GSE2		Yes	Yes	
MB96F348HWC PQC-GSE2			No	
MB96F348TSC PMC-GSE2		No	Yes	100 pin Plastic LQFP (FPT-100P-M20)
MB96F348HSC PMC-GSE2			No	
MB96F348TWC PMC-GSE2		Yes	Yes	
MB96F348HWC PMC-GSE2			No	
MB96V300BRB-ES(for evaluation)	Emulated by ext. RAM	Yes	No	416 pin Plastic BGA (BGA-416P-M02)