Infineon Technologies - MB96F346RWBPMC-GSE2 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	56MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, LVR, POR, PWM, WDT
Number of I/O	80
Program Memory Size	288KB (288K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f346rwbpmc-gse2

Features

Feature	Description
Technology	■ 0.18μm CMOS
CPU	■ F^{2}MC-16FX CPU ■ Up to 56 MHz internal, 17.8 ns instruction cycle time ■ Optimized instruction set for controller applications (bit, byte, word and long-word data types; 23 different addressing modes; barrel shift; variety of pointers) ■ 8-byte instruction execution queue ■ Signed multiply (16-bit × 16-bit) and divide (32-bit/16-bit) instructions available
System clock	■ On-chip PLL clock multiplier (x1 - x25, x1 when PLL stop) ■ 3 MHz - 16 MHz external crystal oscillator clock (maximum frequency when using ceramic resonator depends on Q-factor). ■ Up to 56 MHz external clock for devices with fast clock input feature ■ 32-100 kHz subsystem quartz clock ■ 100kHz/2MHz internal RC clock for quick and safe startup, oscillator stop detection, watchdog ■ Clock source selectable from main- and subclock oscillator (part number suffix “W”) and on-chip RC oscillator, independently for CPU and 2 clock domains of peripherals. ■ Low Power Consumption - 13 operating modes : (different Run, Sleep, Timer modes, Stop mode) ■ Clock modulator
On-chip voltage regulator	■ Internal voltage regulator supports reduced internal MCU voltage, offering low EMI and low power consumption figures
Low voltage reset	■ Reset is generated when supply voltage is below minimum.
Code Security	■ Protects ROM content from unintended read-out
Memory Patch Function	■ Replaces ROM content ■ Can also be used to implement embedded debug support
DMA	■ Automatic transfer function independent of CPU, can be assigned freely to resources
Interrupts	■ Fast Interrupt processing ■ 8 programmable priority levels ■ Non-Maskable Interrupt (NMI)
Timers	■ Three independent clock timers (23-bit RC clock timer, 23-bit Main clock timer, 17-bit Sub clock timer) ■ Watchdog Timer
CAN	■ Supports CAN protocol version 2.0 part A and B ■ ISO16845 certified ■ Bit rates up to 1 Mbit/s ■ 32 message objects ■ Each message object has its own identifier mask ■ Programmable FIFO mode (concatenation of message objects) ■ Maskable interrupt ■ Disabled Automatic Retransmission mode for Time Triggered CAN applications ■ Programmable loop-back mode for self-test operation
USART	■ Full duplex USARTs (SCI/LIN) ■ Wide range of baud rate settings using a dedicated reload timer ■ Special synchronous options for adapting to different synchronous serial protocols ■ LIN functionality working either as master or slave LIN device

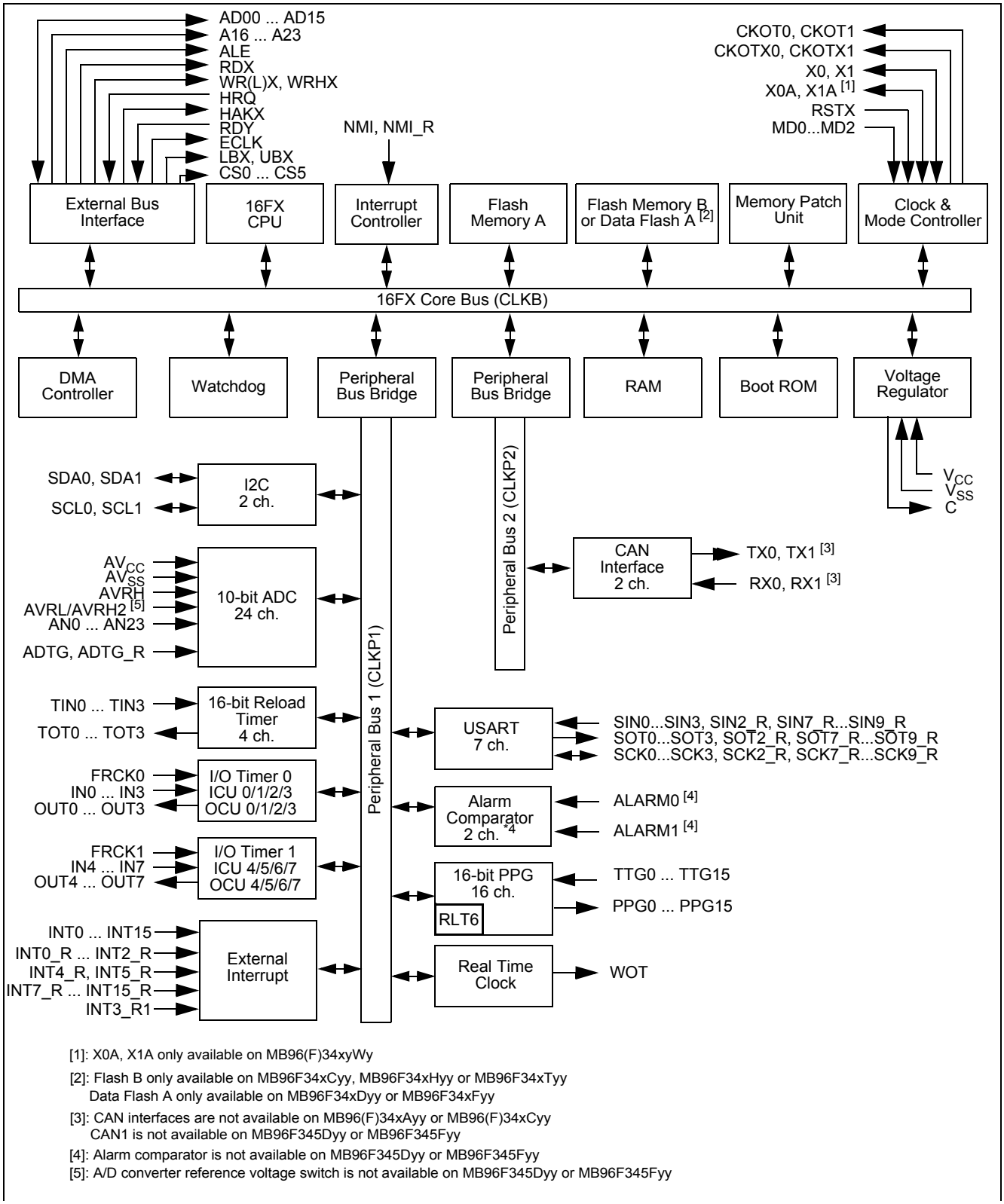
Feature	Description
I^2C	■ Up to 400 kbps ■ Master and Slave functionality, 8-bit and 10-bit addressing
A/D converter	■ SAR-type ■ 10-bit resolution ■ Signals interrupt on conversion end, single conversion mode, continuous conversion mode, stop conversion mode, activation by software, external trigger or reload timer
A/D Converter Reference Voltage switch	■ 2 independent positive A/D converter reference voltages available
Reload Timers	■ 16-bit wide ■ Prescaler with $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$ of peripheral clock frequency ■ Event count function
Free Running Timers	■ Signals an interrupt on overflow, supports timer clear upon match with Output Compare (0, 4), Prescaler with 1, $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$, $1/2^7$,$1/2^8$ of peripheral clock frequency
Input Capture Units	■ 16-bit wide ■ Signals an interrupt upon external event ■ Rising edge, falling edge or rising & falling edge sensitive
Output Compare Units	■ 16-bit wide ■ Signals an interrupt when a match with 16-bit I/O Timer occurs ■ A pair of compare registers can be used to generate an output signal.
Programmable Pulse Generator	■ 16-bit down counter, cycle and duty setting registers ■ Interrupt at trigger, counter borrow and/or duty match ■ PWM operation and one-shot operation ■ Internal prescaler allows 1, 1/4, 1/16, 1/64 of peripheral clock as counter clock and Reload timer overflow as clock input ■ Can be triggered by software or reload timer
Real Time Clock	■ Can be clocked either from sub oscillator (devices with part number suffix “W”), main oscillator or from the RC oscillator ■ Facility to correct oscillation deviation of Sub clock or RC oscillator clock (clock calibration) ■ Read/write accessible second/minute/hour registers ■ Can signal interrupts every half second/second/minute/hour/day ■ Internal clock divider and prescaler provide exact 1s clock
External Interrupts	■ Edge sensitive or level sensitive ■ Interrupt mask and pending bit per channel ■ Each available CAN channel RX has an external interrupt for wake-up ■ Selected USART channels SIN have an external interrupt for wake-up
Non Maskable Interrupt	■ Disabled after reset ■ Once enabled, can not be disabled other than by reset. ■ Level high or level low sensitive ■ Pin shared with external interrupt 0.
External bus interface	■ 8-bit or 16-bit bidirectional data ■ Up to 24-bit addresses ■ 6 chip select signals ■ Multiplexed address/data lines ■ Wait state request ■ External bus master possible ■ Timing programmable

Features	MB96V300B	MB96(F)34x
I^2C	2 channels	2 channels
A/D Converter	40 channels	24 channels
A/D Converter Reference Voltage switch	yes	yes (except MB96F345Dyy or MB96F345Fyy)
16-bit Reload Timer	6 channels + 1 channel (for PPG)	4 channels + 1 channel (for PPG)
16-bit Free-Running Timer	4 channels	2 channels
16-bit Output Compare	12 channels	8 channels
16-bit Input Capture	12 channels	8 channels
16-bit Programmable Pulse Generator	20 channels	16 channels
CAN Interface	5 channels	MB96(F)34xAyy or MB96(F)34xCyy: no MB96F345Dyy or MB96F345Fyy: 1 channel others: 2 channels
External Interrupts	16 channels	
Non-Maskable Interrupt	1 channel	
Real Time Clock	1	
I/O Ports	136	80 for part number with suffix "W", 82 for part number with suffix "S"
Alarm comparator	2 channels	MB96F345Dyy or MB96F345Fyy: no others: 2 channels
External bus interface	Yes	Yes (multiplexed address/data)
Chip select	6 signals	
Clock output function	2 channels	
Low voltage reset	Yes	
On-chip RC-oscillator	Yes	

[1]: These devices are under development and specification is preliminary. These products under development may change its specification without notice.

2. Block Diagram

Figure 1. Block diagram of MB96(F)34x



[1]: X0A, X1A only available on MB96(F)34xyWy

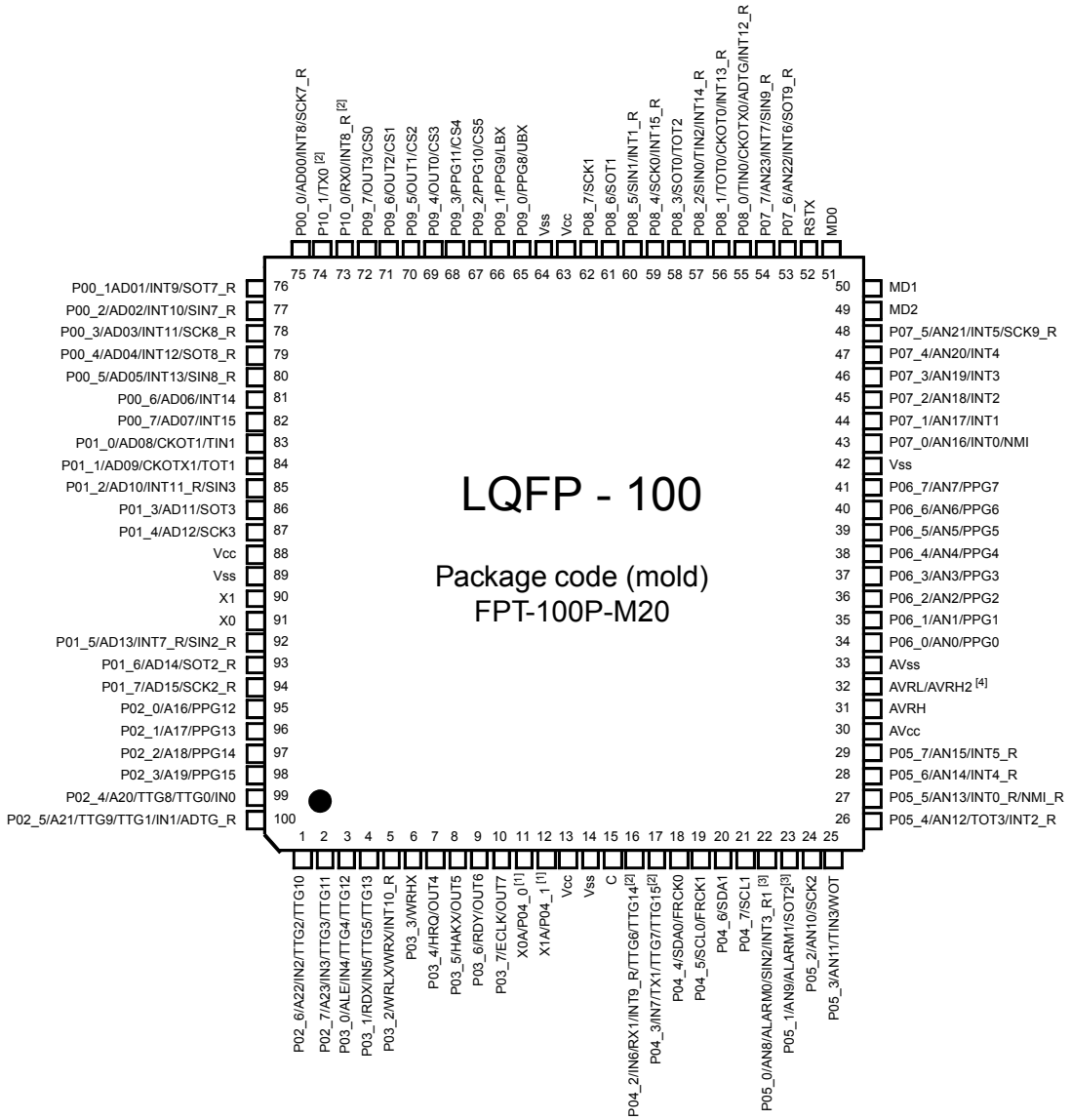
[2]: Flash B only available on MB96F34xCyy, MB96F34xHyy or MB96F34xTyy
Data Flash A only available on MB96F34xDyy or MB96F34xFyy

[3]: CAN interfaces are not available on MB96(F)34xAyy or MB96(F)34xCyy
CAN1 is not available on MB96F345Dyy or MB96F345Fyy

[4]: Alarm comparator is not available on MB96F345Dyy or MB96F345Fyy

[5]: A/D converter reference voltage switch is not available on MB96F345Dyy or MB96F345Fyy

Figure 3. Pin assignment of MB96(F)34x (FPT-100P-M20)



[1]: MB96(F)34xyWy: X0A, X1A
MB96(F)34xySy: P04_0, P04_1

[2]: TX0, RX0, TX1, RX1 are not available on MB96(F)34xAyy or MB96(F)34xCyy
TX1, RX1 are not available on MB96F345Dyy or MB96F345Fyy

[3]: ALARM0, ALARM1 are not available on MB96F345Dyy or MB96F345Fyy

[4]: AVRH2 is not available on MB96F345Dyy or MB96F345Fyy

(FPT-100P-M20)

Remark:

MB96(F)34x products are pin-compatible to F^{2}MC-16LX family MB90340 series.

5. Pin Circuit Type

Table 2: Pin circuit types

FPT-100P-M20		FPT-100P-M22	
Pin no.	Circuit type [1]	Pin no.	Circuit type [1]
1-10	H	1-12	H
11,12	B [2]	13, 14	B [2]
11,12	H [3]	13, 14	H [3]
13,14	Supply	15,16	Supply
15	F	17	F
16,17	H	18,19	H
18-21	N	20-23	N
22-29	I	24-31	I
30	Supply	32	Supply
31-32	G	33-34	G
33	Supply	35	Supply
34 to 41	I	36 to 43	I
42	Supply	44	Supply
43 to 48	I	45 to 50	I
49 to 51	C	51 to 53	C
52	E	54	E
53 to 54	I	55 to 56	I
55 to 62	H	57 to 64	H
63, 64	Supply	65, 66	Supply
65 to 87	H	67 to 89	H
88,89	Supply	90, 91	Supply
90, 91	A	92, 93	A
92-100	H	94 to 100	H

[1]: Please refer to “ I/O Circuit Type” for details on the I/O circuit types
[2]: Devices with suffix ”W”
[3]: Devices without suffix ”W”

8. User ROM Memory Map For Flash Devices

MB96F345D
MB96F345F

Alternative mode CPU address	Flash memory mode address	Flash size 160kByte +64KByte Data Flash	
$FF:FFFF_H$ $FF:0000_H$	$3F:FFFF_H$ $3F:0000_H$	S39 - 64K	Flash A
$FE:FFFF_H$ $FE:0000_H$	$3E:FFFF_H$ $3E:0000_H$	S38 - 64K	
$FD:FFFF_H$ $FD:0000_H$	$3D:FFFF_H$ $3D:0000_H$	External bus	
$FC:FFFF_H$ $FC:0000_H$	$3C:FFFF_H$ $3C:0000_H$		
$FB:FFFF_H$ $FB:0000_H$	$3B:FFFF_H$ $3B:0000_H$		
$FA:FFFF_H$ $FA:0000_H$	$3A:FFFF_H$ $3A:0000_H$		
$F9:FFFF_H$ $F9:0000_H$	$39:FFFF_H$ $39:0000_H$		
$F8:FFFF_H$ $F8:0000_H$	$38:FFFF_H$ $38:0000_H$		
$F7:FFFF_H$ $F7:0000_H$	$37:FFFF_H$ $37:0000_H$		
$F6:FFFF_H$ $F6:0000_H$	$36:FFFF_H$ $36:0000_H$		
$F5:FFFF_H$ $F5:0000_H$	$35:FFFF_H$ $35:0000_H$		
$F4:FFFF_H$ $F4:0000_H$	$34:FFFF_H$ $34:0000_H$		
$F3:FFFF_H$ $F3:0000_H$	$33:FFFF_H$ $33:0000_H$		
$F2:FFFF_H$ $F2:0000_H$	$32:FFFF_H$ $32:0000_H$		
$F1:FFFF_H$ $F1:0000_H$	$31:FFFF_H$ $31:0000_H$		
$F0:FFFF_H$ $F0:0000_H$	$30:FFFF_H$ $30:0000_H$		
$E0:FFFF_H$ $E0:0000_H$			
$DF:FFFF_H$ $DF:8000_H$		Reserved	
$DF:7FFF_H$ $DF:6000_H$	$1F:7FFF_H$ $1F:6000_H$	SA3 - 8K	Flash A
$DF:5FFF_H$ $DF:4000_H$	$1F:5FFF_H$ $1F:4000_H$	SA2 - 8K	
$DF:3FFF_H$ $DF:2000_H$	$1F:3FFF_H$ $1F:2000_H$	SA1 - 8K	
$DF:1FFF_H$ $DF:0000_H$	$1F:1FFF_H$ $1F:0000_H$	SA0 - 8K [1]	
$DE:FFFF_H$ $DE:0000_H$		Reserved	
$0E:FFFF_H$ $0E:FF00_H$	$(0E:FFFF_H)$ $(0E:FF00_H)$	SDA0-256 [2]	Data Flash A
$0E:FEFF_H$ $0E:0000_H$		Reserved	
$0D:FFFF_H$ $0D:C000_H$	$(0F:FFFF_H)$ $(0F:C000_H)$	SDA4-16K	Data Flash A
$0D:BFFF_H$ $0D:8000_H$	$(0F:BFFF_H)$ $(0F:8000_H)$	SDA3-16K	
$0D:7FFF_H$ $0D:4000_H$	$(0F:7FFF_H)$ $(0F:4000_H)$	SDA2-16K	
$0D:3FFF_H$ $0D:0000_H$	$(0F:3FFF_H)$ $(0F:0000_H)$	SDA1-16K	
$0C:FFFF_H$ $0C:0000_H$		Reserved	

[1]: Sector SA0 contains the ROM Configuration Block RCBA at CPU address $DF:0000_H$ - $DF:007F_H$

[2]: Sector SDA0 contains the ROM Configuration Block RCBDA at CPU address $DE:FF00_H$ - $DE:FF2F_H$

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$0004E3_H$	RTC - Second Register	WTSR		R/W
$0004E4_H$	RTC - Minutes	WTMR		R/W
$0004E5_H$	RTC - Hour	WTHR		R/W
$0004E6_H$	RTC - Timer Control Extended Register	WTCER		R/W
$0004E7_H$	RTC - Clock select register	WTCKSR		R/W
$0004E8_H$	RTC - Timer Control Register Low	WTCRL	WTCR	R/W
$0004E9_H$	RTC - Timer Control Register High	WTCRH		R/W
$0004EA_H$	CAL - Calibration unit Control register	CUCR		R/W
$0004EB_H$	Reserved			-
$0004EC_H$	CAL - Duration Timer Data Register Low	CUTDL	CUTD	R/W
$0004ED_H$	CAL - Duration Timer Data Register High	CUTDH		R/W
$0004EE_H$	CAL - Calibration Timer Register 2 Low	CUTR2L	CUTR2	R
$0004EF_H$	CAL - Calibration Timer Register 2 High	CUTR2H		R
$0004F0_H$	CAL - Calibration Timer Register 1 Low	CUTR1L	CUTR1	R
$0004F1_H$	CAL - Calibration Timer Register 1 High	CUTR1H		R
$0004F2_H$-$0004F9_H$	Reserved			-
$0004FA_H$	RLT - Timer input select (for Cascading)	TMISR		R/W
$0004FB_H$-$00053D_H$	Reserved			-
$00053E_H$	USART7 - Serial Mode Register	SMR7		R/W
$00053F_H$	USART7 - Serial Control Register	SCR7		R/W
000540_H	USART7 - Serial TX Register	TDR7		W
000540_H	USART7 - Serial RX Register	RDR7		R
000541_H	USART7 - Serial Status Register	SSR7		R/W
000542_H	USART7 - Ext. Control/Com. Register	ECCR7		R/W
000543_H	USART7 - Ext. Status Com. Register	ESCR7		R/W
000544_H	USART7 - Baud Rate Generator Register Low	BGRL7	BGR7	R/W
000545_H	USART7 - Baud Rate Generator Register High	BGRH7		R/W
000546_H	USART7 - Extended Serial Interrupt Register	ESIR7		R/W
000547_H	Reserved			-
000548_H	USART8 - Serial Mode Register	SMR8		R/W
000549_H	USART8 - Serial Control Register	SCR8		R/W
$00054A_H$	USART8 - Serial TX Register	TDR8		W

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000801_H	CAN1 - Control register High (reserved)	CTRLRH1		R
000802_H	CAN1 - Status register Low	STATRL1	STATR1	R/W
000803_H	CAN1 - Status register High (reserved)	STATRH1		R
000804_H	CAN1 - Error Counter Low (Transmit)	ERRCNTL1	ERRCNT1	R
000805_H	CAN1 - Error Counter High (Receive)	ERRCNTH1		R
000806_H	CAN1 - Bit Timing Register Low	BTRL1	BTR1	R/W
000807_H	CAN1 - Bit Timing Register High	BTRH1		R/W
000808_H	CAN1 - Interrupt Register Low	INTRL1	INTR1	R
000809_H	CAN1 - Interrupt Register High	INTRH1		R
$00080A_H$	CAN1 - Test Register Low	TESTRL1	TESTR1	R/W
$00080B_H$	CAN1 - Test Register High (reserved)	TESTRH1		R
$00080C_H$	CAN1 - BRP Extension register Low	BRPERL1	BRPER1	R/W
$00080D_H$	CAN1 - BRP Extension register High (reserved)	BRPERH1		R
$00080E_H$-$00080F_H$	Reserved			-
000810_H	CAN1 - IF1 Command request register Low	IF1CREQL1	IF1CREQ1	R/W
000811_H	CAN1 - IF1 Command request register High	IF1CREQH1		R/W
000812_H	CAN1 - IF1 Command Mask register Low	IF1CMSKL1	IF1CMSK1	R/W
000813_H	CAN1 - IF1 Command Mask register High (reserved)	IF1CMSKH1		R
000814_H	CAN1 - IF1 Mask 1 Register Low	IF1MSK1L1	IF1MSK11	R/W
000815_H	CAN1 - IF1 Mask 1 Register High	IF1MSK1H1		R/W
000816_H	CAN1 - IF1 Mask 2 Register Low	IF1MSK2L1	IF1MSK21	R/W
000817_H	CAN1 - IF1 Mask 2 Register High	IF1MSK2H1		R/W
000818_H	CAN1 - IF1 Arbitration 1 Register Low	IF1ARB1L1	IF1ARB11	R/W
000819_H	CAN1 - IF1 Arbitration 1 Register High	IF1ARB1H1		R/W
$00081A_H$	CAN1 - IF1 Arbitration 2 Register Low	IF1ARB2L1	IF1ARB21	R/W
$00081B_H$	CAN1 - IF1 Arbitration 2 Register High	IF1ARB2H1		R/W
$00081C_H$	CAN1 - IF1 Message Control Register Low	IF1MCTRL1	IF1MCTR1	R/W
$00081D_H$	CAN1 - IF1 Message Control Register High	IF1MCTRH1		R/W
$00081E_H$	CAN1 - IF1 Data A1 Low	IF1DTA1L1	IF1DTA11	R/W
$00081F_H$	CAN1 - IF1 Data A1 High	IF1DTA1H1		R/W
000820_H	CAN1 - IF1 Data A2 Low	IF1DTA2L1	IF1DTA21	R/W
000821_H	CAN1 - IF1 Data A2 High	IF1DTA2H1		R/W

Table 5: Interrupt vector table MB96(F)34x

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
60	$30C_H$	ICU4	Yes	60	Input Capture Unit 4
61	308_H	ICU5	Yes	61	Input Capture Unit 5
62	304_H	ICU6	Yes	62	Input Capture Unit 6
63	300_H	ICU7	Yes	63	Input Capture Unit 7
64	$2FC_H$	OCU0	Yes	64	Output Compare Unit 0
65	$2F8_H$	OCU1	Yes	65	Output Compare Unit 1
66	$2F4_H$	OCU2	Yes	66	Output Compare Unit 2
67	$2F0_H$	OCU3	Yes	67	Output Compare Unit 3
68	$2EC_H$	OCU4	Yes	68	Output Compare Unit 4
69	$2E8_H$	OCU5	Yes	69	Output Compare Unit 5
70	$2E4_H$	OCU6	Yes	70	Output Compare Unit 6
71	$2E0_H$	OCU7	Yes	71	Output Compare Unit 7
72	$2DC_H$	FRT0	Yes	72	Free Running Timer 0
73	$2D8_H$	FRT1	Yes	73	Free Running Timer 1
74	$2D4_H$	IIC0	Yes	74	I2C interface
75	$2D0_H$	IIC1	Yes	75	I2C interface
76	$2CC_H$	ADC0	Yes	76	A/D Converter
77	$2C8_H$	ALARM0	No	77	Alarm Comparator 0 (except MB96F345Dyy or MB96F345Fyy)
78	$2C4_H$	ALARM1	No	78	Alarm Comparator 1 (except MB96F345Dyy or MB96F345Fyy)
79	$2C0_H$	LINR0	Yes	79	LIN USART 0 RX
80	$2BC_H$	LINT0	Yes	80	LIN USART 0 TX
81	$2B8_H$	LINR1	Yes	81	LIN USART 1 RX
82	$2B4_H$	LINT1	Yes	82	LIN USART 1 TX
83	$2B0_H$	LINR2	Yes	83	LIN USART 2 RX
84	$2AC_H$	LINT2	Yes	84	LIN USART 2 TX
85	$2A8_H$	LINR3	Yes	85	LIN USART 3 RX
86	$2A4_H$	LINT3	Yes	86	LIN USART 3 TX
87	$2A0_H$	FLASH_A	No	87	Flash memory A (only Flash devices)
88	$29C_H$	FLASH_B	No	88	Flash memory B (only MB96F348T/H/C)
89	298_H	LINR7	Yes	89	LIN USART 7 RX

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Sleep modes[1]	I_{CCSPLL}	PLL Sleep mode with CLKS1/2 = 48MHz, CLKP1/2 = 24MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	9	10.5	mA	Flash devices
			+125°C	9.7	13		
			+25°C	8	9.5	mA	MB96345/346
			+125°C	8.7	11.5		
		PLL Sleep mode with CLKS1/2 = CLKP1= 56MHz, CLKP2 = 28MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	14	15.5	mA	MB96F346/F347/F348
			+125°C	14.8	18		
			+25°C	13.5	15	mA	MB96345/346
			+125°C	14.3	17		
		PLL Sleep mode with CLKS1/2 = 72MHz, CLKP1 = 36MHz, CLKP2 = 18MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	10.5	12	mA	MB96F346/F347/F348Y/R/Ayy
			+125°C	11.3	14.5		
		PLL Sleep mode with CLKS1/2 = 80MHz, CLKP1 = 40MHz, CLKP2 = 20MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	TBD	TBD	mA	MB96F345
			+125°C	TBD	TBD		
		PLL Sleep mode with CLKS1/2 = 96MHz, CLKP1= 48MHz, CLKP2 = 24MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	15	16.5	mA	MB96F348T/H/CyB/C
			+125°C	15.8	19		
			+25°C	14	15.5	mA	MB96345/346
			+125°C	14.8	17.5		
	$I_{CCSMAIN}$	Main Sleep mode with CLKS1/2 = CLKP1/2 = 4MHz (CLKPLL, CLKSC and CLKRC stopped)	+25°C	1.5	1.8	mA	Flash devices
			+125°C	2	4.5		
			+25°C	1.5	1.8	mA	MB96345/346
			+125°C	2	3.8		

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

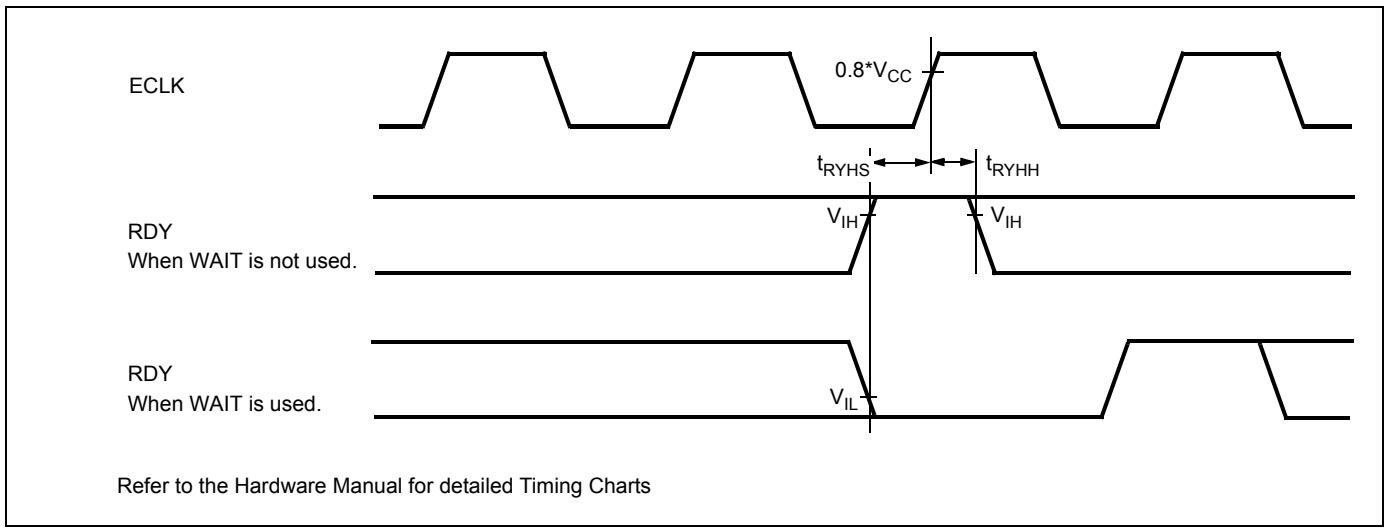
Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Timer modes[1]	I_{CCTRCL}	RC Timer mode with CLKRC = 100kHz, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)	+25°C	0.3	0.45	mA	MB96F346/F347/F348
			+125°C	0.8	3.2		
			+25°C	0.08	0.15	mA	MB96F345
			+125°C	0.58	2.95		
			+25°C	0.3	0.45	mA	MB96345/346
			+125°C	0.8	2.2		
		RC Timer mode with CLKRC = 100kHz, SMCR:LPMSS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode)	+25°C	0.05	0.1	mA	Flash devices
			+125°C	0.55	2.85		
			+25°C	0.05	0.1	mA	MB96345/346
			+125°C	0.55	1.85		
	I_{CCTSUB}	Sub Timer mode with CLKSC = 32kHz (CLKMC, CLKPLL and CLKRC stopped)	+25°C	0.03	0.1	mA	Flash devices
			+125°C	0.53	2.85		
			+25°C	0.03	0.1	mA	MB96345/346
			+125°C	0.53	1.85		
Power supply current in Stop Mode	I_{CCH}	VRCR:LPMB[2:0] = 110_B (Core voltage at 1.8V)	+25°C	0.02	0.08	mA	Flash devices
			+125°C	0.52	2.8		
			+25°C	0.02	0.08	mA	MB96345/346
			+125°C	0.52	1.8		
		VRCR:LPMB[2:0] = 000_B (Core voltage at 1.2V)	+25°C	0.015	0.06	mA	Flash devices
			+125°C	0.4	2.3		
			+25°C	0.015	0.06	mA	MB96345/346
			+125°C	0.4	1.4		
Power supply current for active Low Voltage detector	I_{CCLVD}	Low voltage detector enabled (RCR:LVDE = 1)	-	5	10	µA	MB96F345 Must be added to all current above
			+25°C	90	140	µA	Other devices Must be added to all current above
			+125°C	100	150		

(T_A = –40°C to +125°C, V_{CC} = 3.0 to 4.5V, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
ECLK	t_{CYC}	ECLK	-	30	-	ns	
	t_{CHCL}			t_{CYC}/2-8	t_{CYC}/2+8		
	t_{CLCH}			t_{CYC}/2-8	t_{CYC}/2+8		
ECLK → UBX/ LBX / CSn time	t_{CHCBH}	CSn, UBX, LBX, ECLK	-	-25	25	ns	
	t_{CHCBL}			-25	25		
	t_{CLCBH}			-25	25		
	t_{CLCBL}			-25	25		
ECLK → ALE time	t_{CHLH}	ALE, ECLK	-	-15	15	ns	
	t_{CHLL}			-15	15		
	t_{CLLH}			-15	15		
	t_{CLLL}			-15	15		
ECLK → address valid time	t_{CHAV}	A[23:16], ECLK	-	-20	20	ns	
	t_{CLAV}			-20	20		
	t_{CLADV}	AD[15:0], ECLK	-	-20	20	ns	
	t_{CHADV}			-20	20		
ECLK → RDX /WRX time	t_{CHRWH}	RDX, WRX, WRLX, WRHX, ECLK	-	-15	15	ns	
	t_{CHRWL}			-15	15		
	t_{CLRWH}			-15	15		
	t_{CLRWL}			-15	15		

(T_A = −40°C to +125°C, V_{CC} = 3.0 to 4.5V, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
WRX pulse width	t_{WLWH}	WRX, WRXL, WRHX	-	t_{CYC} − 8	-	ns	w/o cycle extension
Valid data output ⇒ WRX ↑ time	t_{DVWH}	WRX, WRLX, WRHX, AD[15:0]	-	t_{CYC} − 25	-	ns	w/o cycle extension
WRX ↑ ⇒ Data hold time	t_{WHDX}	WRX, WRLX, WRHX, AD[15:0]	-	$t_{CYC}/2$ − 20	-	ns	
WRX ↑ ⇒ Address valid time	t_{WHAX}	WRX, WRLX, WRHX, A[23:16]	-	$t_{CYC}/2$ − 20	-	ns	
WRX ↑ ⇒ ALE ↑ time	t_{WHLH}	WRX, WRLX, WRHX, ALE	EBM:ACE=1 and EACL:STS=1	$2t_{CYC}$ − 15	-	ns	
			other EBM:ACE and EACL:STS setting	t_{CYC} − 15	-		
WRX ↓ ⇒ ECLK ↑ time	t_{WLCH}	WRX, WRLX, WRHX, ECLK	-	$t_{CYC}/2$ − 15	-	ns	
CSn ⇒ WRX time	t_{CSLWL}	WRX, WRLX, WRHX, CSn	EACL:ACE=0	-	$3t_{CYC}/2$ − 20	ns	
			EACL:ACE=1	-	$5t_{CYC}/2$ − 20		
WRX ⇒ CSn time	t_{WHCSH}	WRX, WRLX, WRHX, CSn	-	$t_{CYC}/2$ − 20	-	ns	



Refer to the Hardware Manual for detailed Timing Charts

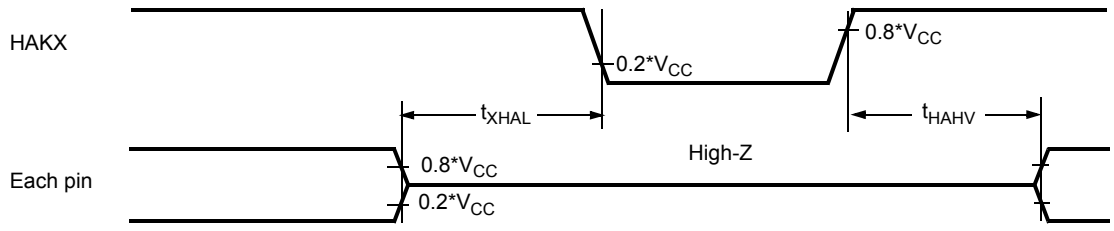
14.4.11 Hold Timing

(T_A = –40°C to +125°C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min	Max		
Pin floating ⇒ HAKX ↓ time	t_{XHAL}	HAKX	-	t_{CYC} – 20	t_{CYC} + 20	ns	
HAKX ↑ time ⇒ Pin valid time	t_{HAHV}	HAKX		t_{CYC} – 20	t_{CYC} + 20	ns	

(T_A = –40°C to +125°C, V_{CC} = 3.0 to 4.5V, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min	Max		
Pin floating ⇒ HAKX ↓ time	t_{XHAL}	HAKX	-	t_{CYC} – 25	t_{CYC} + 25	ns	
HAKX ↑ time ⇒ Pin valid time	t_{HAHV}	HAKX		t_{CYC} – 25	t_{CYC} + 25	ns	



Refer to the Hardware Manual for detailed Timing Charts

14.5 Analog Digital Converter

(T_A = -40 °C to +125 °C, 3.0 V ≤ AVRH - AVRL, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	10	bit	
Total error	-	-	-3	-	+3	LSB	
Nonlinearity error	-	-	-2.5	-	+2.5	LSB	
Differential nonlinearity error	-	-	-1.9	-	+1.9	LSB	
Zero reading voltage	V_{OT}	ANn	AVRL - 1.5 LSB	AVRL+ 0.5 LSB	AVRL + 2.5 LSB	V	
Full scale reading voltage	V_{FST}	ANn	AVRH - 3.5 LSB	AVRH - 1.5 LSB	AVRH + 0.5 LSB	V	
Compare time	-	-	1.0	-	16,500	µs	4.5V ≤ AV_{CC} ≤ 5.5V
			2.0	-	-	µs	3.0V ≤ AV_{CC} < 4.5V
Sampling time	-	-	0.5	-	-	µs	4.5V ≤ AV_{CC} ≤ 5.5V
			1.2	-	-	µs	3.0V ≤ AV_{CC} < 4.5V
Analog port input curren	I_{AIN}	ANn	-3	-	+3	µA	AV_{SS}, AVRL < V_I < AV_{CC}, AVRH
Analog port input curren	I_{AIN}	ANn	-1	-	+1	µA	T_A = 25 °C, AV_{SS}, AVRL < V_I < AV_{CC}, AVRH
			-3	-	+3	µA	T_A = 125 °C,AV_{SS}, AVRL < V_I < AV_{CC}, AVRH
Analog input voltage range	V_{AIN}	ANn	AVRL	-	AVRH	V	
Reference voltage range	AVRH	AVRH/ AVRH 2	0.75 AVcc	-	AVcc	V	
	AVRL	AVRL	AV_{SS}	-	0.25 AV_{CC}	V	
Power supply current	I_A	AVcc	-	2.5	5	mA	A/D Converter active
	I_{AH}	AVcc	-	-	5	µA	A/D Converter not operated
Reference voltage current	I_R	AVRH/ AVRL	-	0.7	1	mA	A/D Converter active
	I_{RH}	AVRH/ AVRL	-	-	5	µA	A/D Converter not operated
Offset between input channels	-	ANn	-	-	4	LSB	

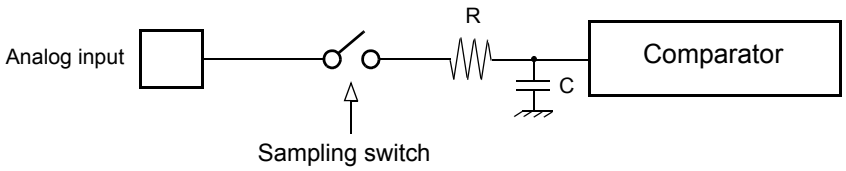
Note: The accuracy gets worse as |AVRH - AVRL| becomes smaller.

14.5.2 Notes on A/D Converter Section

■ About the external impedance of the analog input and the sampling time of the A/D converter (with sample and hold circuit):

If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision.

Analog input circuit model:



Reference value:
C = 8.5 pF (Max)

To satisfy the A/D conversion precision standard, the relationship between the external impedance and minimum sampling time must be considered and then either the resistor value and operating frequency must be adjusted or the external impedance must be decreased so that the sampling time (T_{samp}) is longer than the minimum value. Usually, this value is set to 7τ, where τ = RC. If the external input resistance (R_{ext}) connected to the analog input is included, the sampling time is expressed as follows:

T_{samp} [min] = 7 × (R_{ext} + 2.6kΩ) × C for 4.5 ≤ AV_{cc} ≤ 5.5

T_{samp} [min] = 7 × (R_{ext} + 12.1kΩ) × C for 3.0 ≤ AV_{cc} ≤ 4.5

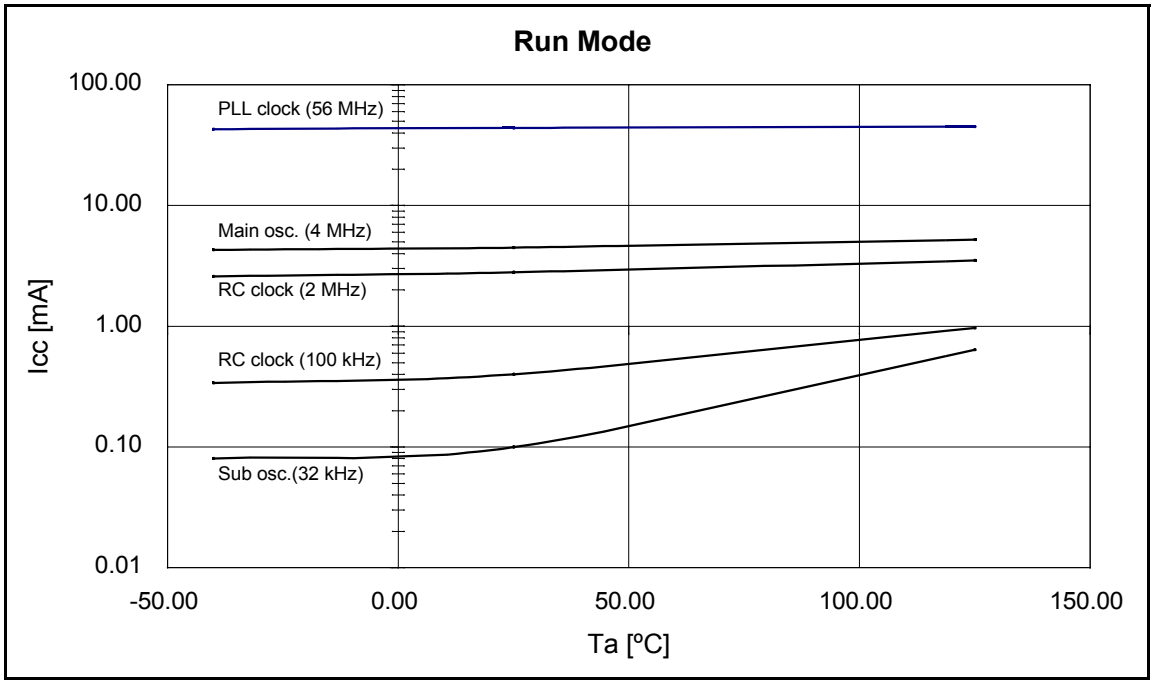
If the sampling time cannot be sufficient, connect a capacitor of about 0.1 μF to the analog input pin.

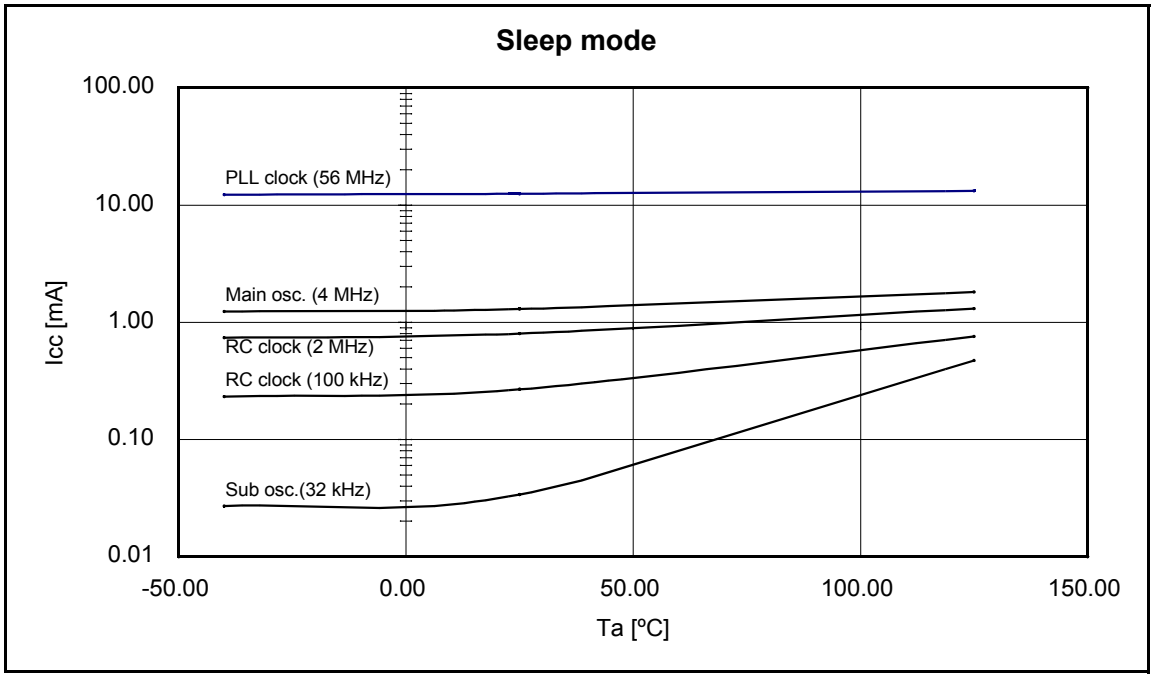
■ About the error

The accuracy gets worse as |AVRH - AVRL| becomes smaller.

15. Example Characteristics

The diagrams below show the characteristics of one measured sample with typical process parameters.





19. Revision History

Revision	Date	Modification
Prelim 1	2007-05-07	Creation
Prelim 2	2007-05-10	External bus hold timing update
Prelim 3	2007-05-23	Electrical characteristics updates
Prelim 4	2007-08-02	Electrical characteristics updates, Product lineup, changes and ordering information
Prelim 5	2007-09-12	Addition of the electrical characteristic examples and the LVD characteristics specifications, updates of the DC characteristics. Pin circuit type drawing modifications.
Prelim 6	2007-11-21	LVD typo correction. Update of the DC characteristics. Typos corrections.
Prelim 7	2007-12-04	Absolute maximum rating asterisks numbering corrected. Typos page 59: Hardware -> Hardware. IO map table regenerated. Typos corrections. IO circuit drawings modified. Renaming of the Main/Satellite Flash into Flash memory A/B. Memory map reworked.
Prelim 8	2008-02-04	■ Satellite Flash -> 32kB Data Flash ■ MB96345 added (under development) ■ MB96F348 TSA/HSA/TWA/HWA removed (outdated devices) ■ Block diagram and pin assignment corrected (existing resource pins) ■ Pin function table corrected ■ I/O circuit type diagrams corrected ■ Memory map cleaned up ■ "Flash sector configuration" replaced by corrected "User ROM Memory map for Flash devices", “ROM configuration” replaced by “User ROM Memory map for Mask ROM devices” ■ Parallel Flash programming pinning removed ■ IO map table regenerated: ❒ Port register: Naming style corrected ❒ Memory control registers renamed (Main/Sat -> A/B) ❒ addresses after 000BFFh removed ■ Absolute maximum ratings: Pd and Ta specified more precisely ■ oscillator input levels in oscillation mode with external clock added ■ Run and Sleep mode currents: 96/48MHz and 72/36MHz settings added ■ Run mode current spec in 48/24MHz mode corrected ■ Maximum CLKS1/2 frequency for all devices correctly specified ■ Maximum CLKP2 for MB96F34xY/R/Axx corrected ■ External bus timings: missing conditions added and readability improved ■ Alarm comparator spec updated (transition voltages defined) ■ MB96V300A removed ■ Ordering information updated ■ Typos and formatting corrected

20. Main Changes in this Edition

Page	Section	Change Results
89	Electrical Characteristics 14.5. Analog Digital Converter	Corrected "Value" and "Unit" of Zero reading voltage. (AVRL - 1.5 → AVRL - 1.5 LSB AVRL + 0.5 → AVRL + 0.5 LSB AVRL + 2.5 → AVRL + 2.5 LSB LSB → V) Corrected "Value" and "Unit" of Full scale reading voltage. (AVRH - 3.5 → AVRH - 3.5 LSB AVRH - 1.5 → AVRH - 1.5 LSB AVRH + 0.5 → AVRH + 0.5 LSB LSB → V)

NOTE: Please see "Document History" for later revised information.

Document History

Spansion Publication Number: **DS07-13802-3E**

Document Title: MB96345/346, MB96F345, MB96F346/F347/F348, F^{2}MC-16FX, MB96340 Series, 16-bit Proprietary Microcontroller Datasheet **Document Number: 002-04579**				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	_	AKIH	06/17/2009	Migrated to Cypress and assigned document number 002-04579. No change to document contents or format.
*A	5198948	AKIH	04/04/2016	Updated to Cypress template