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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Discontinued at Digi-Key
Core Processor	F ² MC-16FX
Core Size	16-Bit
Speed	56MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, LVR, POR, PWM, WDT
Number of I/O	80
Program Memory Size	288KB (288K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-PQFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f346rwpqc-gse2

2. Block Diagram

Figure 1. Block diagram of MB96(F)34x

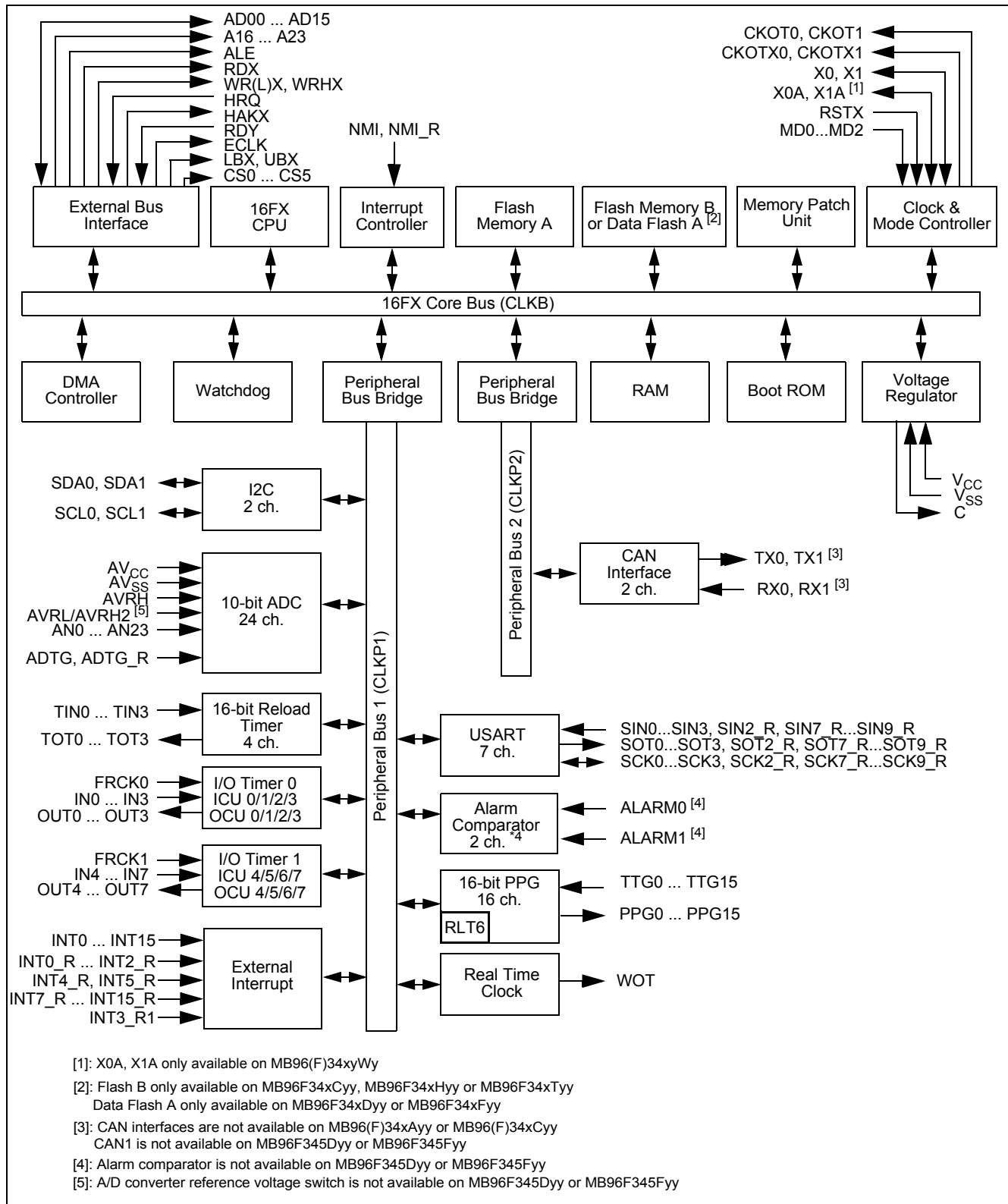
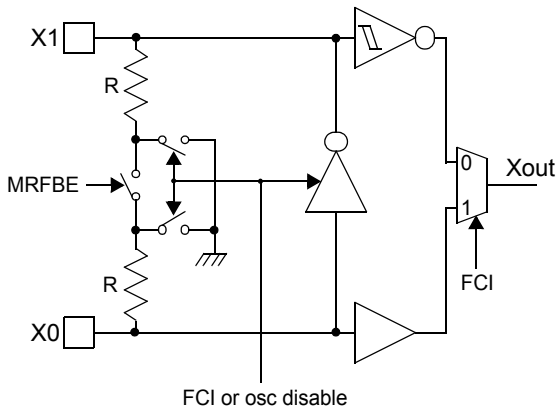
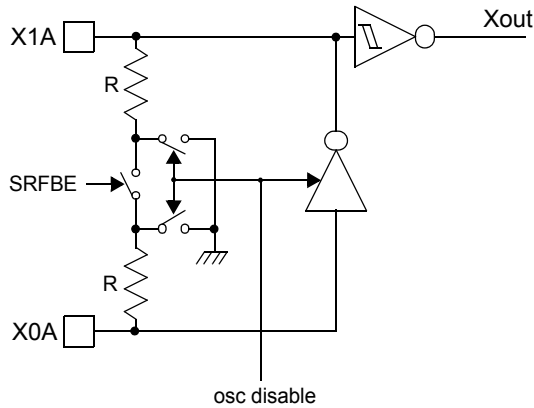
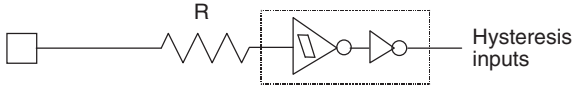
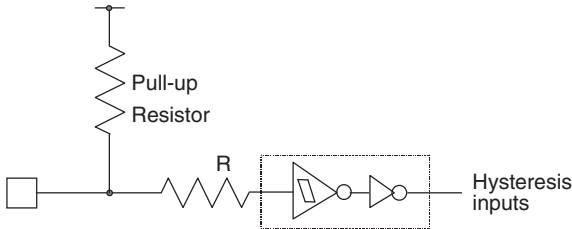
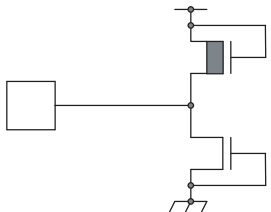
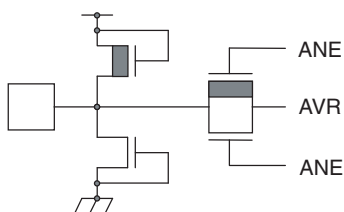
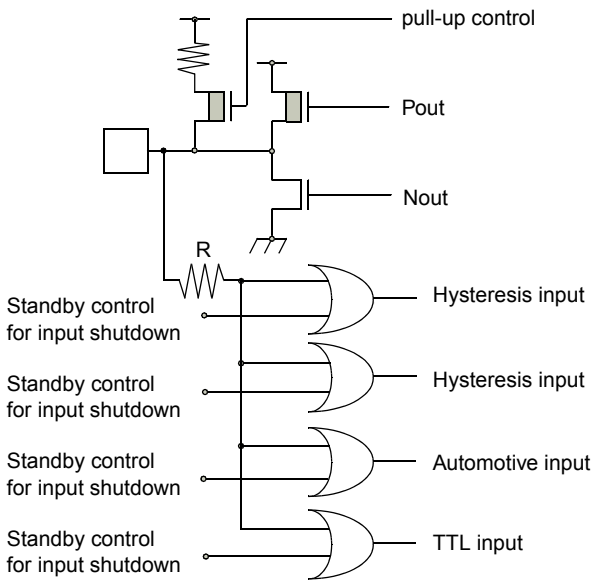


Table 1: Pin Function description

Pin name	Feature	Description
RDY	External bus	External bus interface external wait state request input
RSTX	Core	Reset input
RXn	CAN	CAN interface n RX input
SCKn	USART	USART n serial clock input/output
SCKn_R	USART	Relocated USART n serial clock input/output
SCLn	I ² C	I ² C interface n clock I/O input/output
SDAn	I ² C	I ² C interface n serial data I/O input/output
SINn	USART	USART n serial data input
SINn_R	USART	Relocated USART n serial data input
SOTn	USART	USART n serial data output
SOTn_R	USART	Relocated USART n serial data output
TINn	Reload Timer	Reload Timer n event input
TOTn	Reload Timer	Reload Timer n output
TTGn	PPG	Programmable Pulse Generator n trigger input
TXn	CAN	CAN interface n TX output
UBX	External bus	External Bus Interface Upper Byte select strobe output
V _{CC}	Supply	Power supply
V _{SS}	Supply	Power supply
WOT	RTC	Real Timer clock output
WRHX	External bus	External bus High byte write strobe output
WRLX/WRX	External bus	External bus Low byte / Word write strobe output
X0	Clock	Oscillator input
X0A	Clock	Subclock Oscillator input (only for devices with suffix "W")
X1	Clock	Oscillator output
X1A	Clock	Subclock Oscillator output (only for devices with suffix "W")

6. I/O Circuit Type

Type	Circuit	Remarks
A		High-speed oscillation circuit: ■ Programmable between oscillation mode (external crystal or resonator connected to X0/X1 pins) and Fast external Clock Input (FCI) mode (external clock connected to X0 pin) ■ Programmable feedback resistor = approx. $2 * 0.5 \text{ M}\Omega$. Feedback resistor is grounded in the center when the oscillator is disabled or in FCI mode
B		Low-speed oscillation circuit: ■ Programmable feedback resistor = approx. $2 * 5 \text{ M}\Omega$. Feedback resistor is grounded in the center when the oscillator is disabled
C		■ Mask ROM and EVA device: CMOS Hysteresis input pin ■ Flash device: CMOS input pin
E		■ CMOS Hysteresis input pin ■ Pull-up resistor value: approx. $50 \text{ k}\Omega$

Type	Circuit	Remarks
F		■ Power supply input protection circuit
G		■ A/D converter ref+ (AVRH/AVRH2) power supply input pin with protection circuit ■ Flash devices do not have a protection circuit against VCC for pins AVRH/AVRH2 ■ Devices without AVRH reference switch do not have an analog switch for the AVRL pin
H		■ CMOS level output (programmable $I_{OL} = 5\text{mA}$, $I_{OH} = -5\text{mA}$ and $I_{OL} = 2\text{mA}$, $I_{OH} = -2\text{mA}$) ■ 2 different CMOS hysteresis inputs with input shutdown function * ■ Automotive input with input shutdown function ■ TTL input with input shutdown function * ■ Programmable pull-up resistor: 50kΩ approx. *MB96F345Dyy or MB96F345Fyy: Only Automotive input and CMOS hysteresis input (0.7/0.3) are supported

8. User ROM Memory Map For Flash Devices

MB96F345D MB96F345F					
Alternative mode CPU address	Flash memory mode address	Flash size 160kByte +64KByte Data Flash			
FF:FFFF _H FF:0000 _H	3F:FFFF _H 3F:0000 _H	S39 - 64K	Flash A		
FE:FFFF _H FE:0000 _H	3E:FFFF _H 3E:0000 _H	S38 - 64K			
FD:FFFF _H FD:0000 _H	3D:FFFF _H 3D:0000 _H	External bus			
FC:FFFF _H FC:0000 _H	3C:FFFF _H 3C:0000 _H				
FB:FFFF _H FB:0000 _H	3B:FFFF _H 3B:0000 _H				
FA:FFFF _H FA:0000 _H	3A:FFFF _H 3A:0000 _H				
F9:FFFF _H F9:0000 _H	39:FFFF _H 39:0000 _H				
F8:FFFF _H F8:0000 _H	38:FFFF _H 38:0000 _H				
F7:FFFF _H F7:0000 _H	37:FFFF _H 37:0000 _H				
F6:FFFF _H F6:0000 _H	36:FFFF _H 36:0000 _H				
F5:FFFF _H F5:0000 _H	35:FFFF _H 35:0000 _H				
F4:FFFF _H F4:0000 _H	34:FFFF _H 34:0000 _H				
F3:FFFF _H F3:0000 _H	33:FFFF _H 33:0000 _H				
F2:FFFF _H F2:0000 _H	32:FFFF _H 32:0000 _H				
F1:FFFF _H F1:0000 _H	31:FFFF _H 31:0000 _H				
F0:FFFF _H F0:0000 _H	30:FFFF _H 30:0000 _H				
E0:FFFF _H E0:0000 _H					
DF:FFFF _H DF:8000 _H				Reserved	
DF:7FFF _H DF:6000 _H	1F:7FFF _H 1F:6000 _H			SA3 - 8K	Flash A
DF:5FFF _H DF:4000 _H	1F:5FFF _H 1F:4000 _H			SA2 - 8K	
DF:3FFF _H DF:2000 _H	1F:3FFF _H 1F:2000 _H			SA1 - 8K	
DF:1FFF _H DF:0000 _H	1F:1FFF _H 1F:0000 _H			SA0 - 8K ^[1]	
DE:FFFF _H DE:0000 _H				Reserved	
0E:FFFF _H 0E:FF00 _H	(0E:FFFF _H) (0E:FF00 _H)			SDA0-256 ^[2]	Data Flash A
0E:FEFF _H 0E:0000 _H				Reserved	
0D:FFFF _H 0D:C000 _H	(0F:FFFF _H) (0F:C000 _H)			SDA4-16K	Data Flash A
0D:BFFF _H 0D:8000 _H	(0F:BFFF _H) (0F:8000 _H)			SDA3-16K	
0D:7FFF _H 0D:4000 _H	(0F:7FFF _H) (0F:4000 _H)			SDA2-16K	
0D:3FFF _H 0D:0000 _H	(0F:3FFF _H) (0F:0000 _H)			SDA1-16K	
0C:FFFF _H 0C:0000 _H				Reserved	

[1]: Sector SA0 contains the ROM Configuration Block RCBA at CPU address DF:0000_H - DF:007F_H

[2]: Sector SDA0 contains the ROM Configuration Block RCBD A at CPU address DE:FF00_H - DE:FF2F_H

[1]: Sector SA0 contains the ROM Configuration Block RCBA at CPU address DF:0000_H - DF:007F_H

[2]: Sector SDA0 contains the ROM Configuration Block RCBDA at CPU address DE:FF00_H - DE:FF2F_H

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00004B _H	ICU3 - Capture Register High	IPCPH3		R
00004C _H	ICU4/ICU5 - Control Status Register	ICS45		R/W
00004D _H	ICU4/ICU5 - Edge register	ICE45		R/W
00004E _H	ICU4 - Capture Register Low	IPCPL4	IPCP4	R
00004F _H	ICU4 - Capture Register High	IPCPH4		R
000050 _H	ICU5 - Capture Register Low	IPCPL5	IPCP5	R
000051 _H	ICU5 - Capture Register High	IPCPH5		R
000052 _H	ICU6/ICU7 - Control Status Register	ICS67		R/W
000053 _H	ICU6/ICU7 - Edge register	ICE67		R/W
000054 _H	ICU6 - Capture Register Low	IPCPL6	IPCP6	R
000055 _H	ICU6 - Capture Register High	IPCPH6		R
000056 _H	ICU7 - Capture Register Low	IPCPL7	IPCP7	R
000057 _H	ICU7 - Capture Register High	IPCPH7		R
000058 _H	EXTINT0 - External Interrupt Enable Register	ENIR0		R/W
000059 _H	EXTINT0 - External Interrupt Interrupt request Register	EIRR0		R/W
00005A _H	EXTINT0 - External Interrupt Level Select Low	ELVRL0	ELVR0	R/W
00005B _H	EXTINT0 - External Interrupt Level Select High	ELVRH0		R/W
00005C _H	EXTINT1 - External Interrupt Enable Register	ENIR1		R/W
00005D _H	EXTINT1 - External Interrupt Interrupt request Register	EIRR1		R/W
00005E _H	EXTINT1 - External Interrupt Level Select Low	ELVRL1	ELVR1	R/W
00005F _H	EXTINT1 - External Interrupt Level Select High	ELVRH1		R/W
000060 _H	RLT0 - Timer Control Status Register Low	TMCSRL0	TMCSR0	R/W
000061 _H	RLT0 - Timer Control Status Register High	TMCSRH0		R/W
000062 _H	RLT0 - Reload Register - for writing		TMRLR0	W
000062 _H	RLT0 - Reload Register - for reading		TMR0	R
000063 _H	RLT0 - Reload Register - for writing			W
000063 _H	RLT0 - Reload Register - for reading			R
000064 _H	RLT1 - Timer Control Status Register Low	TMCSRL1	TMCSR1	R/W
000065 _H	RLT1 - Timer Control Status Register High	TMCSRH1		R/W
000066 _H	RLT1 - Reload Register - for writing		TMRLR1	W
000066 _H	RLT1 - Reload Register - for reading		TMR1	R
000067 _H	RLT1 - Reload Register - for writing			W

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000081 _H	PPG1 - Timer register			R
000082 _H	PPG1 - Period setting register		PCSR1	W
000083 _H	PPG1 - Period setting register			W
000084 _H	PPG1 - Duty cycle register		PDUT1	W
000085 _H	PPG1 - Duty cycle register			W
000086 _H	PPG1 - Control status register Low	PCNL1	PCN1	R/W
000087 _H	PPG1 - Control status register High	PCNH1		R/W
000088 _H	PPG2 - Timer register		PTMR2	R
000089 _H	PPG2 - Timer register			R
00008A _H	PPG2 - Period setting register		PCSR2	W
00008B _H	PPG2 - Period setting register			W
00008C _H	PPG2 - Duty cycle register		PDUT2	W
00008D _H	PPG2 - Duty cycle register			W
00008E _H	PPG2 - Control status register Low	PCNL2	PCN2	R/W
00008F _H	PPG2 - Control status register High	PCNH2		R/W
000090 _H	PPG3 - Timer register		PTMR3	R
000091 _H	PPG3 - Timer register			R
000092 _H	PPG3 - Period setting register		PCSR3	W
000093 _H	PPG3 - Period setting register			W
000094 _H	PPG3 - Duty cycle register		PDUT3	W
000095 _H	PPG3 - Duty cycle register			W
000096 _H	PPG3 - Control status register Low	PCNL3	PCN3	R/W
000097 _H	PPG3 - Control status register High	PCNH3		R/W
000098 _H	PPG7-PPG4 - General Control register 1 Low	GCN1L1	GCN11	R/W
000099 _H	PPG7-PPG4 - General Control register 1 High	GCN1H1		R/W
00009A _H	PPG7-PPG4 - General Control register 2 Low	GCN2L1	GCN21	R/W
00009B _H	PPG7-PPG4 - General Control register 2 High	GCN2H1		R/W
00009C _H	PPG4 - Timer register		PTMR4	R
00009D _H	PPG4 - Timer register			R
00009E _H	PPG4 - Period setting register		PCSR4	W
00009F _H	PPG4 - Period setting register			W
0000A0 _H	PPG4 - Duty cycle register		PDUT4	W

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000382 _H	DMA2 - Interrupt select	DISSEL2		R/W
000383 _H	DMA3 - Interrupt select	DISSEL3		R/W
000384 _H	DMA4 - Interrupt select	DISSEL4		R/W
000385 _H	DMA5 - Interrupt select	DISSEL5		R/W
000386 _H -00038F _H	Reserved			-
000390 _H	DMA - Status register low byte	DSRL	DSR	R/W
000391 _H	DMA - Status register high byte	DSRH		R/W
000392 _H	DMA - Stop status register low byte	DSSRL	DSSR	R/W
000393 _H	DMA - Stop status register high byte	DSSRH		R/W
000394 _H	DMA - Enable register low byte	DERL	DER	R/W
000395 _H	DMA - Enable register high byte	DERH		R/W
000396 _H -00039F _H	Reserved			-
0003A0 _H	Interrupt level register	ILR	ICR	R/W
0003A1 _H	Interrupt index register	IDX		R/W
0003A2 _H	Interrupt vector table base register Low	TBRL	TBR	R/W
0003A3 _H	Interrupt vector table base register High	TBRH		R/W
0003A4 _H	Delayed Interrupt register	DIRR		R/W
0003A5 _H	Non Maskable Interrupt register	NMI		R/W
0003A6 _H -0003AB _H	Reserved			-
0003AC _H	EDSU communication interrupt selection Low	EDSU2L	EDSU2	R/W
0003AD _H	EDSU communication interrupt selection High	EDSU2H		R/W
0003AE _H	ROM mirror control register	ROMM		R/W
0003AF _H	EDSU configuration register	EDSU		R/W
0003B0 _H	Memory patch control/status register ch 0/1		PFCS0	R/W
0003B1 _H	Memory patch control/status register ch 0/1			R/W
0003B2 _H	Memory patch control/status register ch 2/3		PFCS1	R/W
0003B3 _H	Memory patch control/status register ch 2/3			R/W
0003B4 _H	Memory patch control/status register ch 4/5		PFCS2	R/W
0003B5 _H	Memory patch control/status register ch 4/5			R/W
0003B6 _H	Memory patch control/status register ch 6/7		PFCS3	R/W
0003B7 _H	Memory patch control/status register ch 6/7			R/W
0003B8 _H	Memory Patch function - Patch address 0 low	PFAL0		R/W

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0004B3 _H -0004BB _H	Reserved			-
0004BC _H	I/O Port P00 - External Pin State Register	EPSR00		R
0004BD _H	I/O Port P01 - External Pin State Register	EPSR01		R
0004BE _H	I/O Port P02 - External Pin State Register	EPSR02		R
0004BF _H	I/O Port P03 - External Pin State Register	EPSR03		R
0004C0 _H	I/O Port P04 - External Pin State Register	EPSR04		R
0004C1 _H	I/O Port P05 - External Pin State Register	EPSR05		R
0004C2 _H	I/O Port P06 - External Pin State Register	EPSR06		R
0004C3 _H	I/O Port P07 - External Pin State Register	EPSR07		R
0004C4 _H	I/O Port P08 - External Pin State Register	EPSR08		R
0004C5 _H	I/O Port P09 - External Pin State Register	EPSR09		R
0004C6 _H	I/O Port P10 - External Pin State Register	EPSR10		R
0004C7 _H -0004CF _H	Reserved			-
0004D0 _H	ADC analog input enable register 0	ADER0		R/W
0004D1 _H	ADC analog input enable register 1	ADER1		R/W
0004D2 _H	ADC analog input enable register 2	ADER2		R/W
0004D3 _H	ADC analog input enable register 3	ADER3		R/W
0004D4 _H	ADC analog input enable register 4	ADER4		R/W
0004D5 _H	Reserved			-
0004D6 _H	Peripheral Resource Relocation Register 0	PRRR0		R/W
0004D7 _H	Peripheral Resource Relocation Register 1	PRRR1		R/W
0004D8 _H	Peripheral Resource Relocation Register 2	PRRR2		R/W
0004D9 _H	Peripheral Resource Relocation Register 3	PRRR3		R/W
0004DA _H	Peripheral Resource Relocation Register 4	PRRR4		R/W
0004DB _H	Peripheral Resource Relocation Register 5	PRRR5		R/W
0004DC _H	Peripheral Resource Relocation Register 6	PRRR6		R/W
0004DD _H	Peripheral Resource Relocation Register 7	PRRR7		R/W
0004DE _H	Peripheral Resource Relocation Register 8	PRRR8		R/W
0004DF _H	Peripheral Resource Relocation Register 9	PRRR9		R/W
0004E0 _H	RTC - Sub Second Register L	WTBRL0	WTBR0	R/W
0004E1 _H	RTC - Sub Second Register M	WTBRH0		R/W
0004E2 _H	RTC - Sub-Second Register H	WTBR1		R/W

[4]: The maximum permitted power dissipation depends on the ambient temperature, the air flow velocity and the thermal conductance of the package on the PCB. The actual power dissipation depends on the customer application and can be calculated as follows:

$$P_D = P_{IO} + P_{INT}$$

$$P_{IO} = \sum (V_{OL} * I_{OL} + V_{OH} * I_{OH}) \text{ (IO load power dissipation, sum is performed on all IO ports)}$$

$$P_{INT} = V_{CC} * (I_{CC} + I_A) \text{ (internal power dissipation)}$$

I_{CC} is the total core current consumption into V_{CC} as described in the "DC characteristics" and depends on the selected operation mode and clock frequency and the usage of functions like Flash programming or the clock modulator. I_A is the analog current consumption into AV_{CC} .

[5]: Worst case value for a package mounted on single layer PCB at specified T_A without air flow.

[6]: Please contact Cypress for reliability limitations when using under these conditions.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed any of these ratings.

14.2 Recommended Operating Conditions

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}	3.0	-	5.5	V	
Smoothing capacitor at C pin	C_S	3.5	4.7 - 10	15	μF	Use a low inductance capacitor (for example X7R ceramic capacitor)

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

($T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = 0\text{V}$)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Run modes ^[1]	I_{CCRCH}	RC Run mode with $CLKS1/2 = CLKB = CLKP1/2 = 2\text{MHz}$ (CLKMC, CLKPLL and CLKSC stopped)	+25°C	2.9	4	mA	Flash devices at 1 Flash wait state
			+125°C	3.5	6.5		
			+25°C	1.7	2.7	mA	MB96345/346 at 1 ROM wait state
			+125°C	2.3	4.7		
	I_{CCRCL}	RC Run mode with $CLKS1/2 = CLKB = CLKP1/2 = 100\text{kHz}$, SMCR:LPMS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)	+25°C	0.4	0.6	mA	MB96F346/F347/F348 at 1 Flash wait state
			+125°C	0.9	3.5		
			+25°C	0.18	0.3	mA	MB96F345 at 1 Flash wait state
			+125°C	0.68	3.3		
		RC Run mode with $CLKS1/2 = CLKB = CLKP1/2 = 100\text{kHz}$, SMCR:LPMS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode, no Flash programming/erasing allowed)	+25°C	0.4	0.6	mA	MB96345/346 at 1 ROM wait state
			+125°C	0.9	2.4		
			+25°C	0.15	0.25	mA	Flash devices at 1 Flash wait state
			+125°C	0.65	3.2		
			+25°C	0.15	0.25	mA	MB96345/346 at 1 ROM wait state
			+125°C	0.65	2.1		
	I_{CCSUB}	Sub Run mode with $CLKS1/2 = CLKB = CLKP1/2 = 32\text{kHz}$ (CLKMC, CLKPLL and CLKRC stopped, no Flash programming/erasing allowed)	+25°C	0.1	0.2	mA	Flash devices at 1 Flash wait state
			+125°C	0.6	3		
			+25°C	0.1	0.2	mA	MB96345/346 at 1 ROM wait state
			+125°C	0.6	2		

($T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = 0\text{V}$)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Sleep modes ^[1]	I_{CCSPLL}	PLL Sleep mode with $CLKS1/2 = 48\text{MHz}$, $CLKP1/2 = 24\text{MHz}$ (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	9	10.5	mA	Flash devices
			+125°C	9.7	13		
			+25°C	8	9.5	mA	MB96345/346
			+125°C	8.7	11.5		
		PLL Sleep mode with $CLKS1/2 =$ $CLKP1 = 56\text{MHz}$, $CLKP2 = 28\text{MHz}$ (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	14	15.5	mA	MB96F346/F347/F348
			+125°C	14.8	18		
			+25°C	13.5	15	mA	MB96345/346
			+125°C	14.3	17		
		PLL Sleep mode with $CLKS1/2 = 72\text{MHz}$, $CLKP1 = 36\text{MHz}$, $CLKP2 = 18\text{MHz}$ (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	10.5	12	mA	MB96F346/F347/F348Y/R/Ayy
			+125°C	11.3	14.5		
		PLL Sleep mode with $CLKS1/2 = 80\text{MHz}$, $CLKP1 = 40\text{MHz}$, $CLKP2 = 20\text{MHz}$ (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	TBD	TBD	mA	MB96F345
			+125°C	TBD	TBD		
		PLL Sleep mode with $CLKS1/2 = 96\text{MHz}$, $CLKP1 = 48\text{MHz}$, $CLKP2 = 24\text{MHz}$ (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	15	16.5	mA	MB96F348T/H/CyB/C
			+125°C	15.8	19		
			+25°C	14	15.5	mA	MB96345/346
			+125°C	14.8	17.5		
	$I_{CCSMAIN}$	Main Sleep mode with $CLKS1/2 =$ $CLKP1/2 = 4\text{MHz}$ (CLKPLL, CLKSC and CLKRC stopped)	+25°C	1.5	1.8	mA	Flash devices
			+125°C	2	4.5		
			+25°C	1.5	1.8	mA	MB96345/346
			+125°C	2	3.8		

14.4.7 Basic Timing

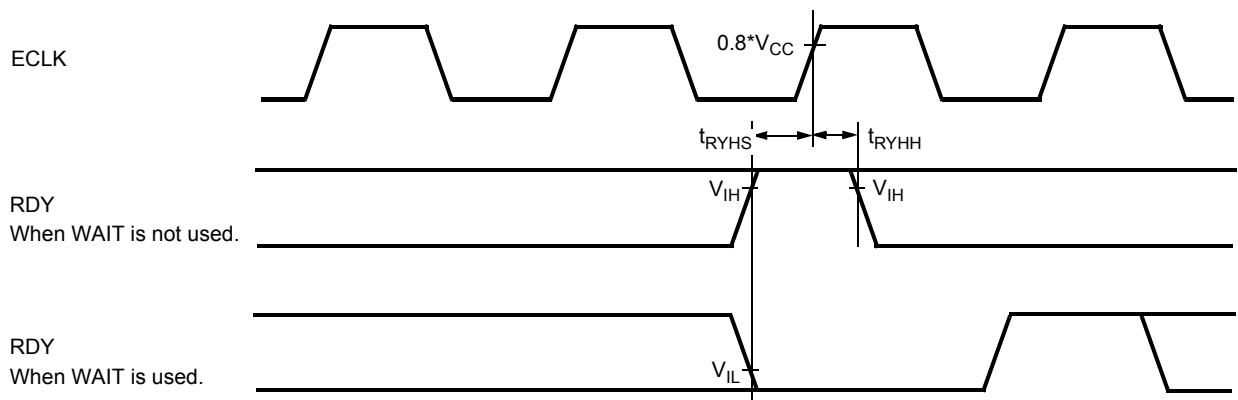
($T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $I_{O_{drive}} = 5\text{mA}$, $C_L = 50\text{pF}$)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
ECLK	t_{CYC}	ECLK	-	25	-	ns	
	t_{CHCL}			$t_{CYC}/2-5$	$t_{CYC}/2+5$		
	t_{CLCH}			$t_{CYC}/2-5$	$t_{CYC}/2+5$		
ECLK → UBX/ LBX / CSn time	t_{CHCBH}	CSn, UBX, LBX, ECLK	-	-20	20	ns	
	t_{CHCBL}			-20	20		
	t_{CLCBH}			-20	20		
	t_{CLCBL}			-20	20		
ECLK → ALE time	t_{CHLH}	ALE, ECLK	-	-10	10	ns	
	t_{CHLL}			-10	10		
	t_{CLLH}			-10	10		
	t_{CLLL}			-10	10		
ECLK → address valid time	t_{CHAV}	A[23:16], ECLK	-	-15	15	ns	
	t_{CLAV}			-15	15		
	t_{CLADV}	AD[15:0], ECLK	-	-15	15	ns	
	t_{CHADV}			-15	15		
ECLK → RDX /WRX time	t_{CHRWL}	RDX, WRX, WRLX, WRHX, ECLK	-	-10	10	ns	
	t_{CHRWL}			-10	10		
	t_{CLRWH}			-10	10		
	t_{CLRWL}			-10	10		

14.4.8 Bus Timing (Read)

($T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $I_{Odrive} = 5\text{mA}$, $C_L = 50\text{pF}$)

Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
ALE pulse width	t _{LHLL}	ALE	EACL:STS=0 and EACL:ACE=0	t _{CYC} /2 – 5	-	ns	
			EACL:STS=1	t _{CYC} – 5	-		
			EACL:STS=0 and EACL:ACE=1	3t _{CYC} /2 – 5	-		
Valid address ⇒ ALE ↓ time	t _{AVLL}	ALE, A[23:16],	EACL:STS=0 and EACL:ACE=0	t _{CYC} – 15	-	ns	
			EACL:STS=1 and EACL:ACE=0	3t _{CYC} /2 – 15	-		
			EACL:STS=0 and EACL:ACE=1	2t _{CYC} – 15	-		
			EACL:STS=1 and EACL:ACE=1	5t _{CYC} /2 – 15	-		
	t _{ADVLL}	ALE,AD[15:0]	EACL:STS=0 and EACL:ACE=0	t _{CYC} /2 – 15	-	ns	
			EACL:STS=1 and EACL:ACE=0	t _{CYC} – 15	-		
			EACL:STS=0 and EACL:ACE=1	3t _{CYC} /2 – 15	-		
			EACL:STS=1 and EACL:ACE=1	2t _{CYC} – 15	-		
ALE ↓ ⇒ Address valid time	t _{LLAX}	ALE, AD[15:0]	EACL:STS=0	t _{CYC} /2 – 15	-	ns	
			EACL:STS=1	-15	-		
Valid address ⇒ RDX ↓ time	t _{AVRL}	RDX, A[23:16]	EACL:ACE=0	3t _{CYC} /2 – 15	-	ns	
			EACL:ACE=1	5t _{CYC} /2 – 15	-		
	t _{ADVRL}	RDX, AD[15:0]	EACL:ACE=0	t _{CYC} – 15	-	ns	
			EACL:ACE=1	2t _{CYC} – 15	-		
Valid address ⇒ Valid data input	t _{AVDV}	A[23:16], AD[15:0]	EACL:ACE=0	-	3t _{CYC} – 55	ns	w/o cycle extension
			EACL:ACE=1	-	4t _{CYC} – 55		
	t _{ADV DV}	AD[15:0]	EACL:ACE=0	-	5t _{CYC} /2 – 55	ns	w/o cycle extension
			EACL:ACE=1	-	7t _{CYC} /2 – 55		
RDX pulse width	t _{RLRH}	RDX	-	3 t _{CYC} /2 – 5	-	ns	w/o cycle extension
RDX ↓ ⇒ Valid data input	t _{RLDV}	RDX, AD[15:0]	-	-	3 t _{CYC} /2 – 50	ns	w/o cycle extension
RDX ↑ ⇒ Data hold time	t _{RHDX}	RDX, AD[15:0]	-	0	-	ns	
Address valid ⇒ Data hold time	t _{AXDX}	A[23:16], AD[15:0]	-	0	-	ns	



Refer to the Hardware Manual for detailed Timing Charts

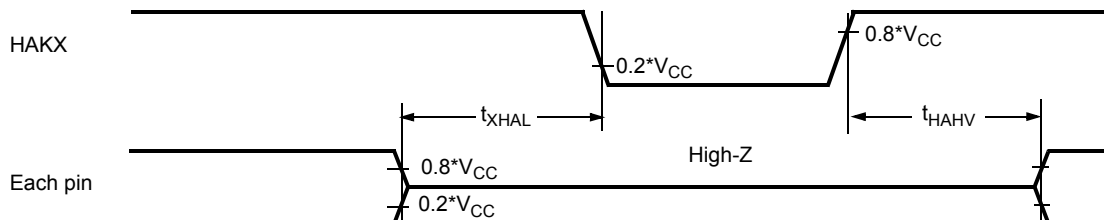
14.4.11 Hold Timing

($T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $I_{O\text{drive}} = 5\text{mA}$, $C_L = 50\text{pF}$)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min	Max		
Pin floating $\Rightarrow$ HAKX $\downarrow$ time	$t_{X\text{HAL}}$	HAKX	-	$t_{CYC} - 20$	$t_{CYC} + 20$	ns	
HAKX $\uparrow$ time $\Rightarrow$ Pin valid time	t_{HAHV}	HAKX		$t_{CYC} - 20$	$t_{CYC} + 20$	ns	

($T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = 3.0$ to 4.5V , $V_{SS} = 0.0\text{ V}$, $I_{O\text{drive}} = 5\text{mA}$, $C_L = 50\text{pF}$)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min	Max		
Pin floating $\Rightarrow$ HAKX $\downarrow$ time	$t_{X\text{HAL}}$	HAKX	-	$t_{CYC} - 25$	$t_{CYC} + 25$	ns	
HAKX $\uparrow$ time $\Rightarrow$ Pin valid time	t_{HAHV}	HAKX		$t_{CYC} - 25$	$t_{CYC} + 25$	ns	



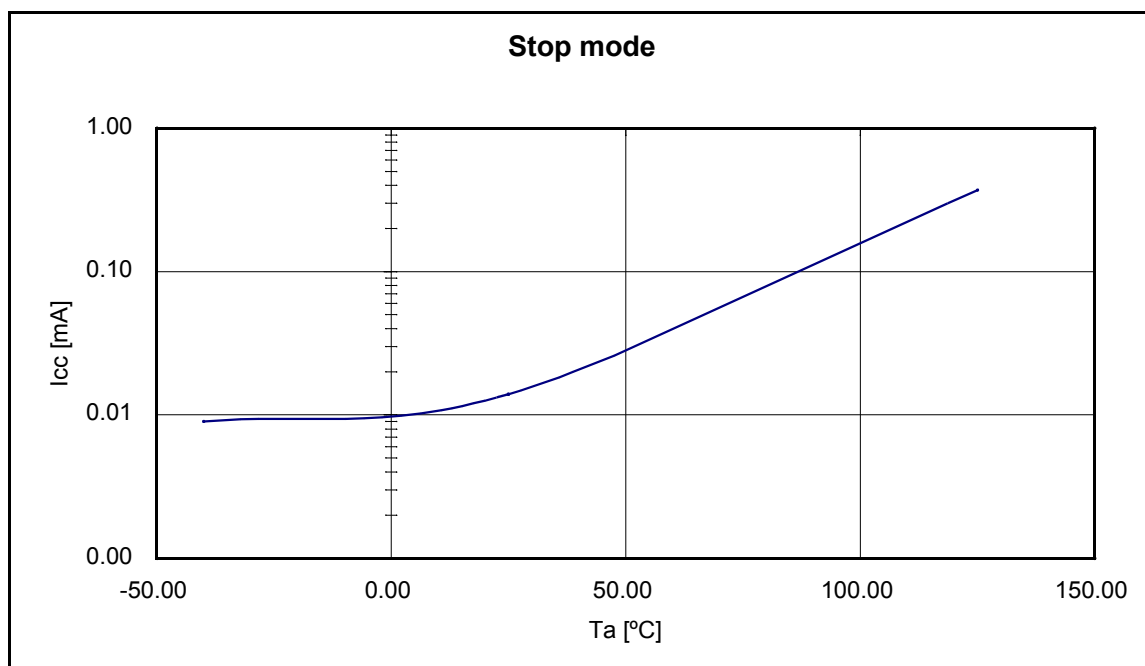
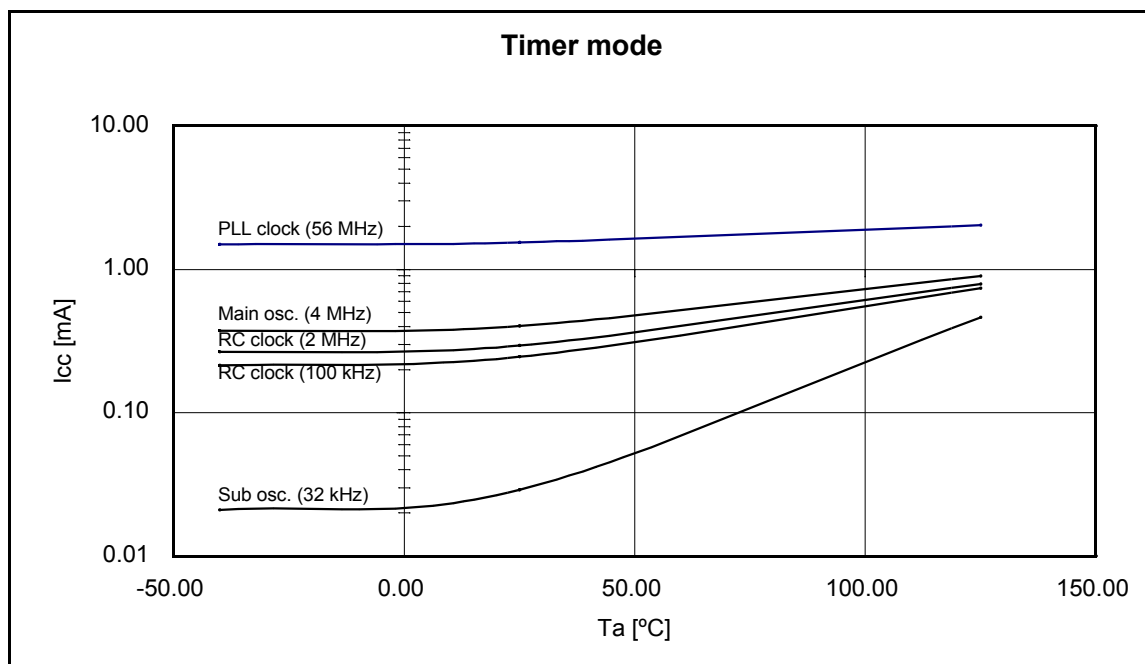
Refer to the Hardware Manual for detailed Timing Charts

14.5 Analog Digital Converter

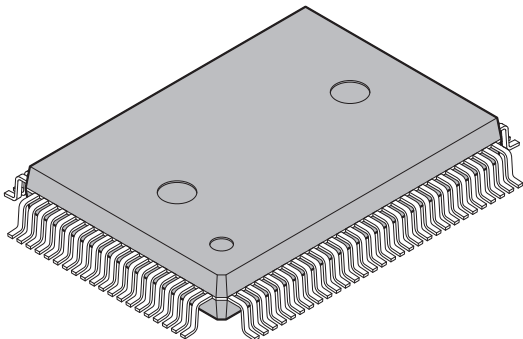
($T_A = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$, $3.0\text{ V} \leq \text{AVRH} - \text{AVRL}$, $V_{CC} = \text{AV}_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = \text{AV}_{SS} = 0\text{V}$)

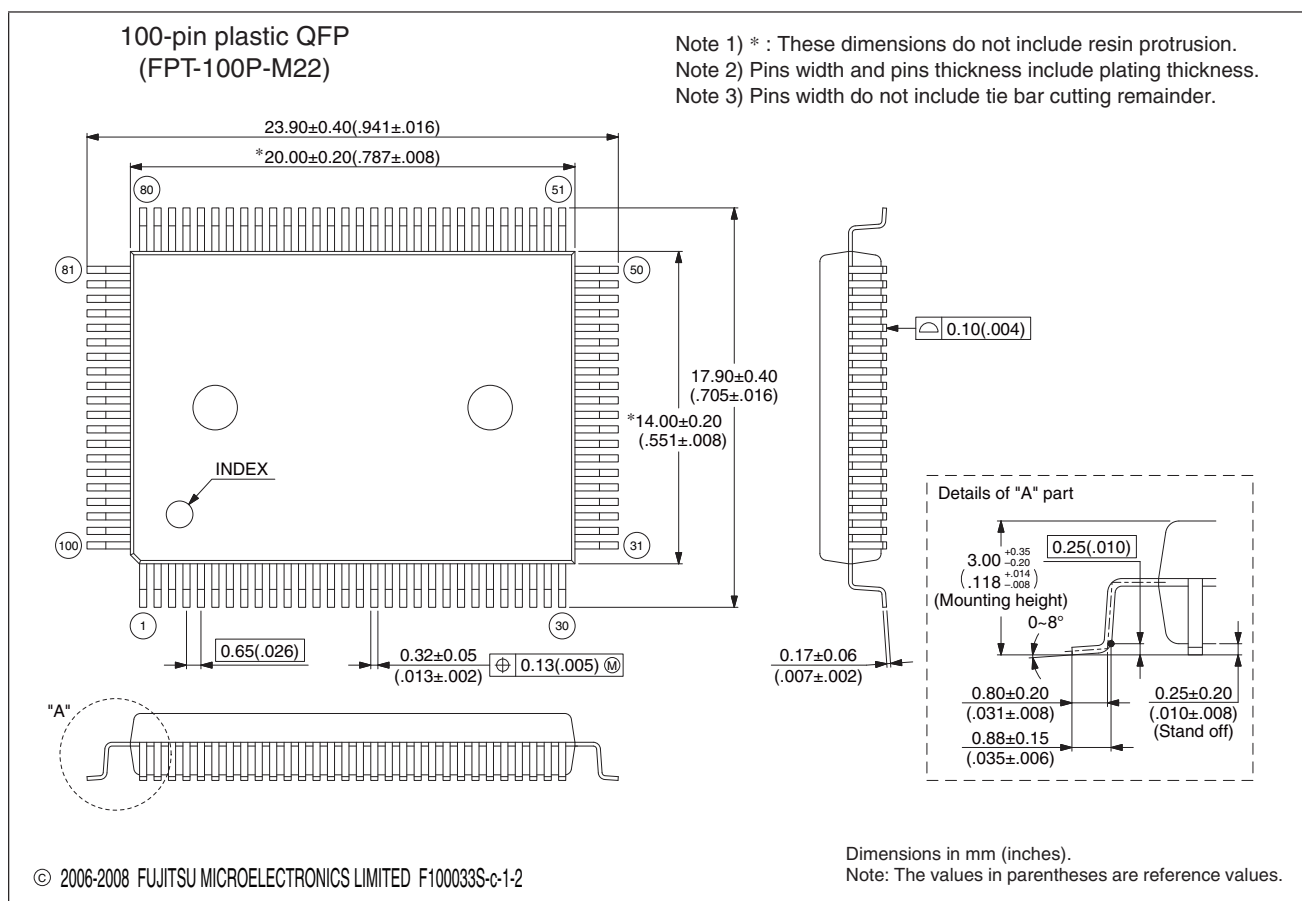
Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	10	bit	
Total error	-	-	-3	-	+3	LSB	
Nonlinearity error	-	-	-2.5	-	+2.5	LSB	
Differential nonlinearity error	-	-	-1.9	-	+1.9	LSB	
Zero reading voltage	V_{OT}	ANn	$\text{AVRL} - 1.5\text{ LSB}$	$\text{AVRL} + 0.5\text{ LSB}$	$\text{AVRL} + 2.5\text{ LSB}$	V	
Full scale reading voltage	V_{FST}	ANn	$\text{AVRH} - 3.5\text{ LSB}$	$\text{AVRH} - 1.5\text{ LSB}$	$\text{AVRH} + 0.5\text{ LSB}$	V	
Compare time	-	-	1.0	-	16,500	μs	$4.5\text{V} \leq \text{AV}_{CC} \leq 5.5\text{V}$
			2.0	-	-	μs	$3.0\text{V} \leq \text{AV}_{CC} < 4.5\text{V}$
Sampling time	-	-	0.5	-	-	μs	$4.5\text{V} \leq \text{AV}_{CC} \leq 5.5\text{V}$
			1.2	-	-	μs	$3.0\text{V} \leq \text{AV}_{CC} < 4.5\text{V}$
Analog port input curren	I_{AIN}	ANn	-3	-	+3	μA	AV_{SS} , $\text{AVRL} < V_I < \text{AV}_{CC}$, AVRH
Analog port input curren	I_{AIN}	ANn	-1	-	+1	μA	$T_A = 25\text{ }^{\circ}\text{C}$, AV_{SS} , $\text{AVRL} < V_I < \text{AV}_{CC}$, AVRH
			-3	-	+3	μA	$T_A = 125\text{ }^{\circ}\text{C}$, AV_{SS} , $\text{AVRL} < V_I < \text{AV}_{CC}$, AVRH
Analog input voltage range	V_{AIN}	ANn	AVRL	-	AVRH	V	
Reference voltage range	AVRH	AVRH/ AVRL 2	0.75 AV_{CC}	-	AV_{CC}	V	
	AVRL	AVRL	AV_{SS}	-	0.25 AV_{CC}	V	
Power supply current	I_A	AV_{CC}	-	2.5	5	mA	A/D Converter active
	I_{AH}	AV_{CC}	-	-	5	μA	A/D Converter not operated
Reference voltage current	I_R	AVRH/ AVRL	-	0.7	1	mA	A/D Converter active
	I_{RH}	AVRH/ AVRL	-	-	5	μA	A/D Converter not operated
Offset between input channels	-	ANn	-	-	4	LSB	

Note: The accuracy gets worse as $|\text{AVRH} - \text{AVRL}|$ becomes smaller.



17. Package Dimension MB96(F)34x QFP 100P

100-pin plastic QFP  (FPT-100P-M22)	Lead pitch	0.65 mm
	Package width × package length	14.00 mm × 20.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	3.35 mm MAX
	Code (Reference)	P-QFP100-14×20-0.65



18. Ordering Information

18.1 MCU with CAN Controller

Part number	Flash/ROM	Subclock	Persistent Low Voltage Reset	Package
MB96345YSA PQC-GSE2 ^[1]	ROM (160KB)	No	Yes	100 pin Plastic QFP (FPT-100P-M22)
MB96345RSA PQC-GSE2 ^[1]			No	
MB96345YWA PQC-GSE2 ^[1]		Yes	Yes	
MB96345RWA PQC-GSE2 ^[1]			No	
MB96345YSA PMC-GSE2 ^[1]		No	Yes	100 pin Plastic LQFP (FPT-100P-M20)
MB96345RSA PMC-GSE2 ^[1]			No	
MB96345YWA PMC-GSE2 ^[1]		Yes	Yes	
MB96345RWA PMC-GSE2 ^[1]			No	
MB96346YSA PQC-GSE2 ^[1]	ROM (288KB)	No	Yes	100 pin Plastic QFP (FPT-100P-M22)
MB96346RSA PQC-GSE2 ^[1]			No	
MB96346YWA PQC-GSE2 ^[1]		Yes	Yes	
MB96346RWA PQC-GSE2 ^[1]			No	
MB96346YSA PMC-GSE2 ^[1]		No	Yes	100 pin Plastic LQFP (FPT-100P-M20)
MB96346RSA PMC-GSE2 ^[1]			No	
MB96346YWA PMC-GSE2 ^[1]		Yes	Yes	
MB96346RWA PMC-GSE2 ^[1]			No	
MB96F345FSA PQC-GSE2 ^[1]	Flash A (160KB) Data Flash A (64KB)	No	Yes	100 pin Plastic QFP (FPT-100P-M22)
MB96F345DSA PQC-GSE2 ^[1]			No	
MB96F345FWA PQC-GSE2 ^[1]		Yes	Yes	
MB96F345DWA PQC-GSE2 ^[1]			No	
MB96F345FSA PMC-GSE2 ^[1]		No	Yes	100 pin Plastic LQFP (FPT-100P-M20)
MB96F345DSA PMC-GSE2 ^[1]			No	
MB96F345FWA PMC-GSE2 ^[1]		Yes	Yes	
MB96F345DWA PMC-GSE2 ^[1]			No	
MB96F346YSB PQC-GSE2	Flash A (288KB)	No	Yes	100 pin Plastic QFP (FPT-100P-M22)
MB96F346RSB PQC-GSE2			No	
MB96F346YWB PQC-GSE2		Yes	Yes	
MB96F346RWB PQC-GSE2			No	
MB96F346YSB PMC-GSE2		No	Yes	100 pin Plastic LQFP (FPT-100P-M20)
MB96F346RSB PMC-GSE2			No	
MB96F346YWB PMC-GSE2		Yes	Yes	
MB96F346RWB PMC-GSE2			No	

19. Revision History

Revision	Date	Modification
Prelim 1	2007-05-07	Creation
Prelim 2	2007-05-10	External bus hold timing update
Prelim 3	2007-05-23	Electrical characteristics updates
Prelim 4	2007-08-02	Electrical characteristics updates, Product lineup, changes and ordering information
Prelim 5	2007-09-12	Addition of the electrical characteristic examples and the LVD characteristics specifications, updates of the DC characteristics. Pin circuit type drawing modifications.
Prelim 6	2007-11-21	LVD typo correction. Update of the DC characteristics. Typos corrections.
Prelim 7	2007-12-04	Absolute maximum rating asterisks numbering corrected. Typos page 59: Hardware -> Hardware. IO map table regenerated. Typos corrections. IO circuit drawings modified. Renaming of the Main/Satellite Flash into Flash memory A/B. Memory map reworked.
Prelim 8	2008-02-04	■ Satellite Flash -> 32kB Data Flash ■ MB96345 added (under development) ■ MB96F348 TSA/HSA/TWA/HWA removed (outdated devices) ■ Block diagram and pin assignment corrected (existing resource pins) ■ Pin function table corrected ■ I/O circuit type diagrams corrected ■ Memory map cleaned up ■ "Flash sector configuration" replaced by corrected "User ROM Memory map for Flash devices", "ROM configuration" replaced by "User ROM Memory map for Mask ROM devices" ■ Parallel Flash programming pinning removed ■ IO map table regenerated: □ Port register: Naming style corrected □ Memory control registers renamed (Main/Sat -> A/B) □ addresses after 000BFFh removed ■ Absolute maximum ratings: Pd and Ta specified more precisely ■ oscillator input levels in oscillation mode with external clock added ■ Run and Sleep mode currents: 96/48MHz and 72/36MHz settings added ■ Run mode current spec in 48/24MHz mode corrected ■ Maximum CLKS1/2 frequency for all devices correctly specified ■ Maximum CLKP2 for MB96F34xY/R/Axx corrected ■ External bus timings: missing conditions added and readability improved ■ Alarm comparator spec updated (transition voltages defined) ■ MB96V300A removed ■ Ordering information updated ■ Typos and formatting corrected