Infineon Technologies - MB96F347ASBPMC-GS-N2E2 Datasheet

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What is "Embedded - Microcontrollers"?

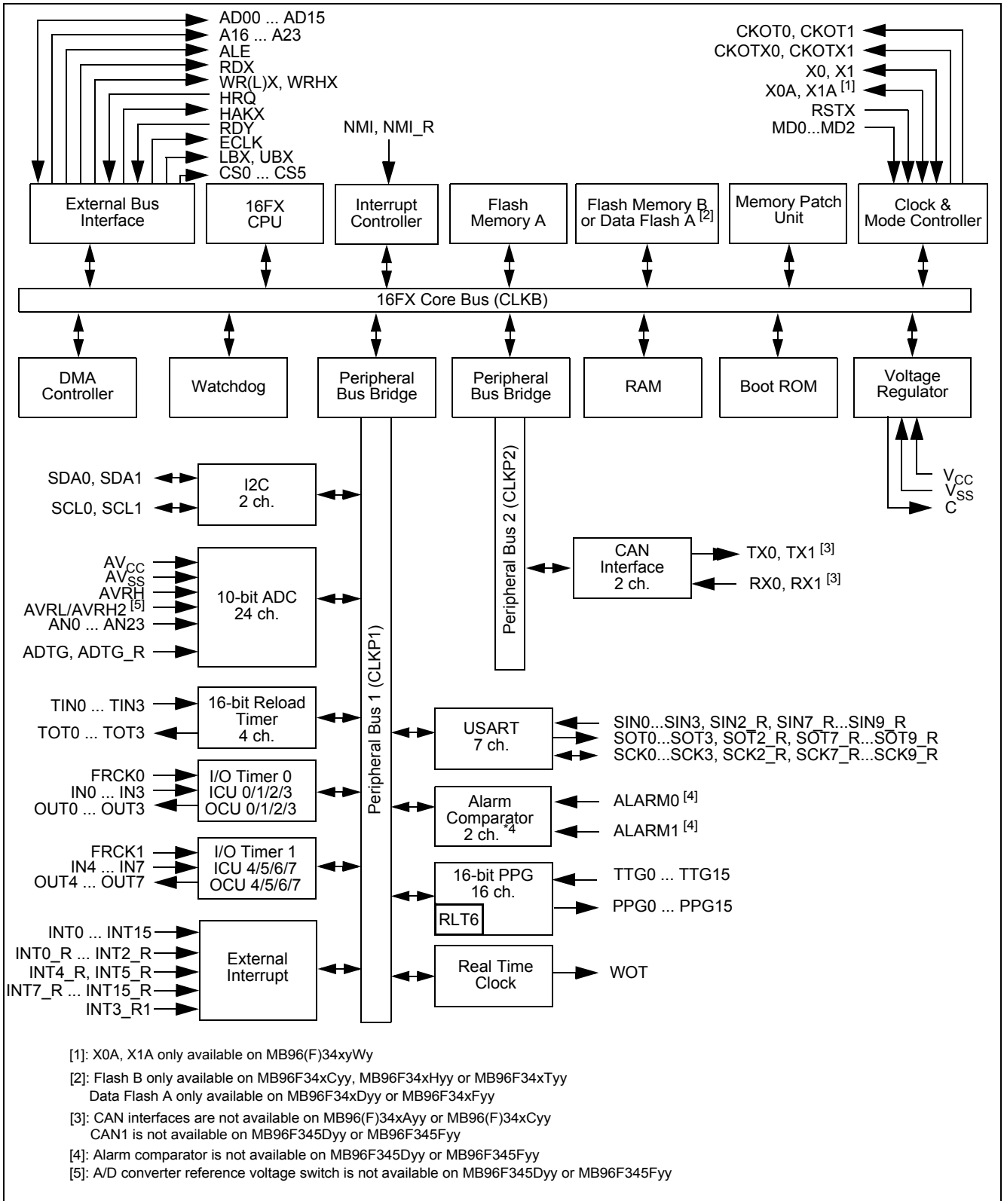
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	56MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, LVR, POR, PWM, WDT
Number of I/O	82
Program Memory Size	416KB (416K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f347asbpmc-gs-n2e2

2. Block Diagram

Figure 1. Block diagram of MB96(F)34x



[1]: X0A, X1A only available on MB96(F)34xyWy

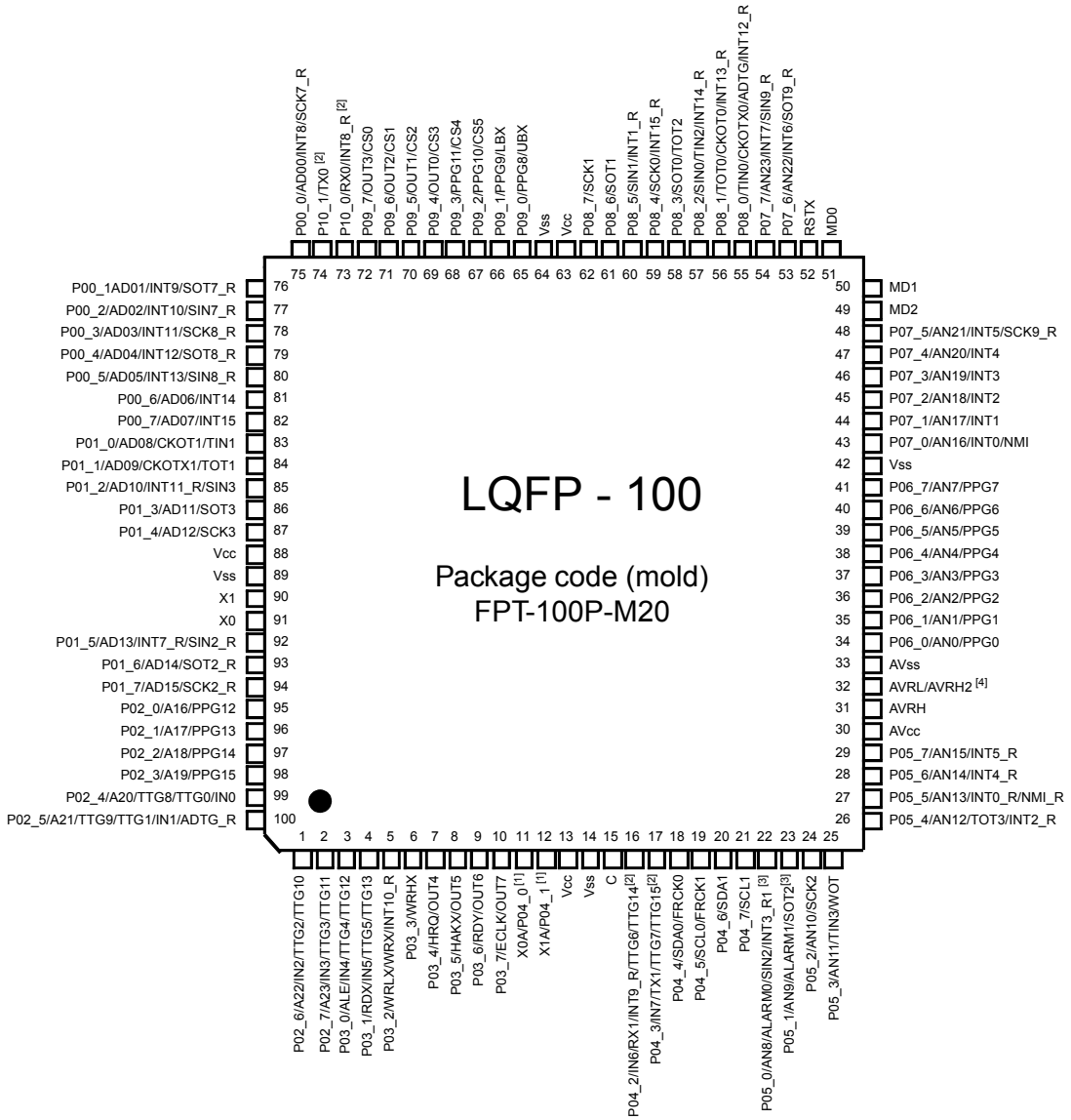
[2]: Flash B only available on MB96F34xCyy, MB96F34xHyy or MB96F34xTyy
Data Flash A only available on MB96F34xDyy or MB96F34xFyy

[3]: CAN interfaces are not available on MB96(F)34xAyy or MB96(F)34xCyy
CAN1 is not available on MB96F345Dyy or MB96F345Fyy

[4]: Alarm comparator is not available on MB96F345Dyy or MB96F345Fyy

[5]: A/D converter reference voltage switch is not available on MB96F345Dyy or MB96F345Fyy

Figure 3. Pin assignment of MB96(F)34x (FPT-100P-M20)



[1]: MB96(F)34xyWy: X0A, X1A
MB96(F)34xySy: P04_0, P04_1

[2]: TX0, RX0, TX1, RX1 are not available on MB96(F)34xAyy or MB96(F)34xCyy
TX1, RX1 are not available on MB96F345Dyy or MB96F345Fyy

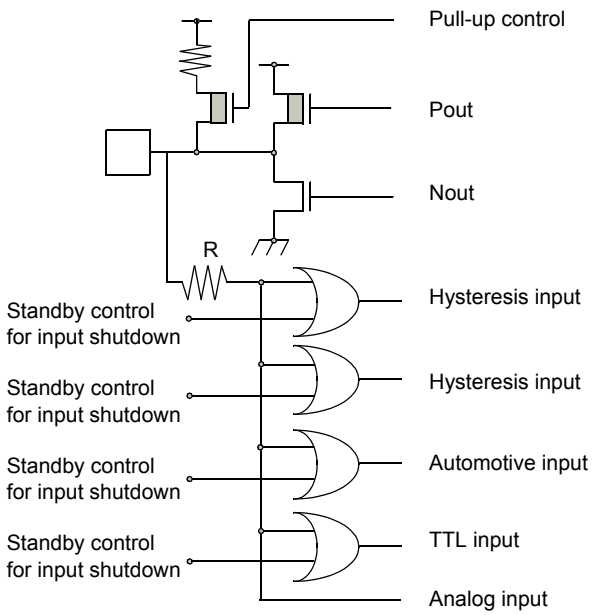
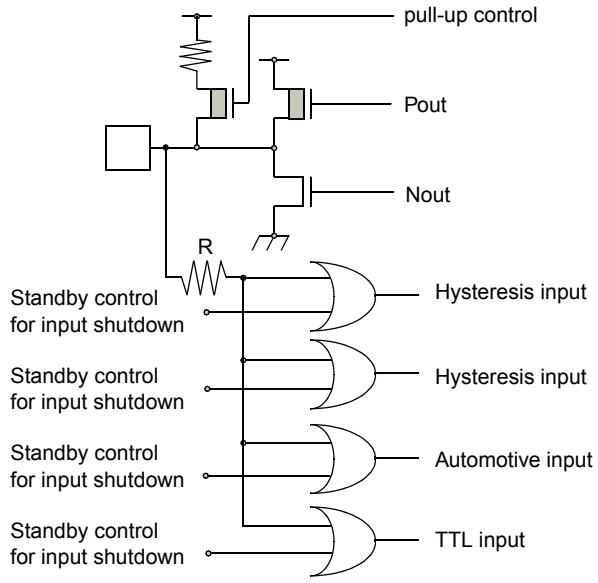
[3]: ALARM0, ALARM1 are not available on MB96F345Dyy or MB96F345Fyy

[4]: AVRH2 is not available on MB96F345Dyy or MB96F345Fyy

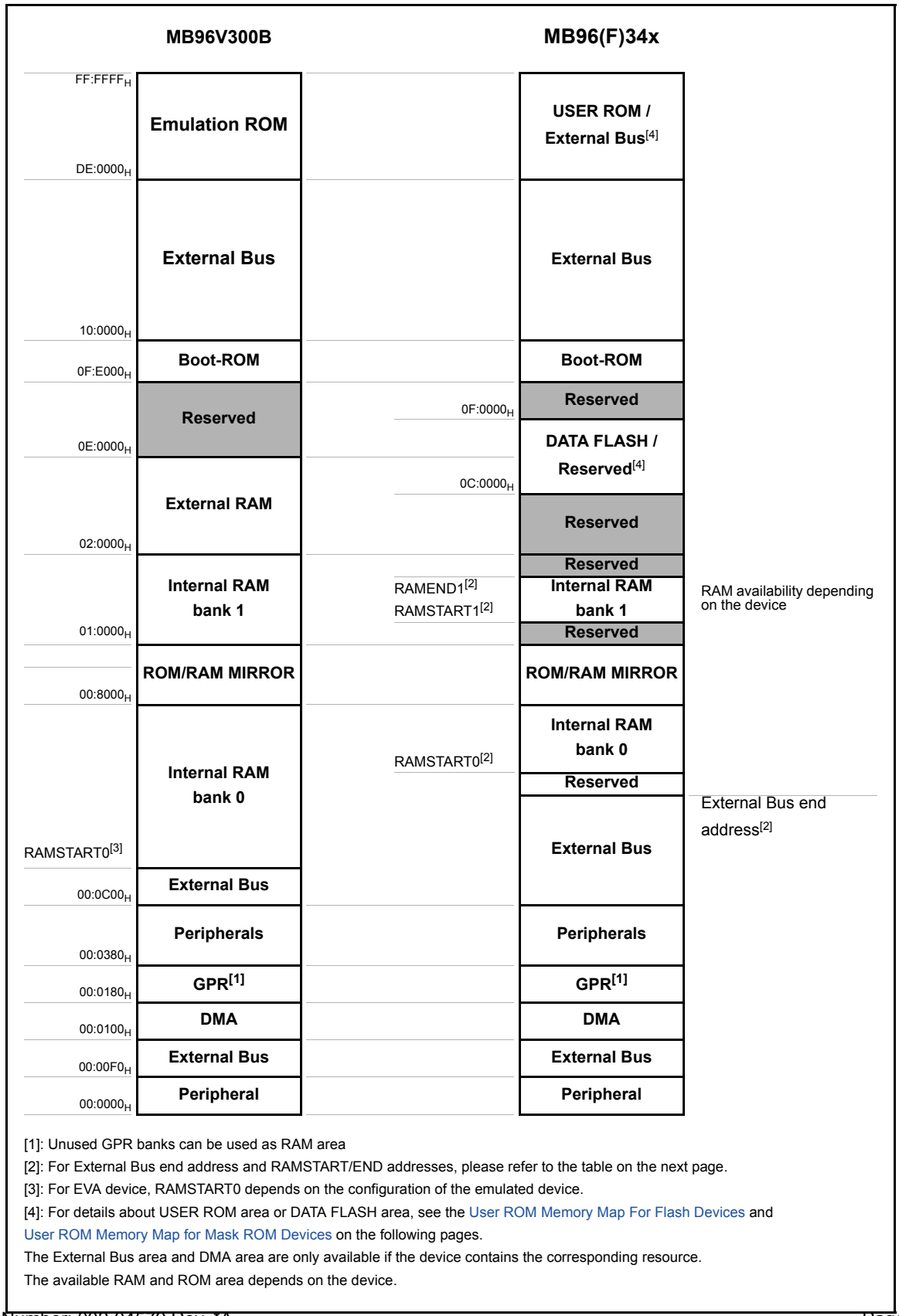
(FPT-100P-M20)

Remark:

MB96(F)34x products are pin-compatible to F^{2}MC-16LX family MB90340 series.

Type	Circuit	Remarks
I		■ CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) ■ 2 different CMOS hysteresis inputs with input shutdown function * ■ Automotive input with input shutdown function ■ TTL input with input shutdown function * ■ Programmable pull-up resistor: 50kΩ approx. ■ Analog input *MB96F345Dyy or MB96F345Fyy: Only Automotive input and CMOS hysteresis input (0.7/0.3) are supported
N		■ CMOS level output (I_{OL} = 3mA, I_{OH} = -3mA) ■ 2 different CMOS hysteresis inputs with input shutdown function * ■ Automotive input with input shutdown function ■ TTL input with input shutdown function * ■ Programmable pull-up resistor: 50kΩ approx. *MB96F345Dyy or MB96F345Fyy: Only Automotive input and CMOS hysteresis input (0.7/0.3) are supported

7. Memory Map



[1]: Unused GPR banks can be used as RAM area

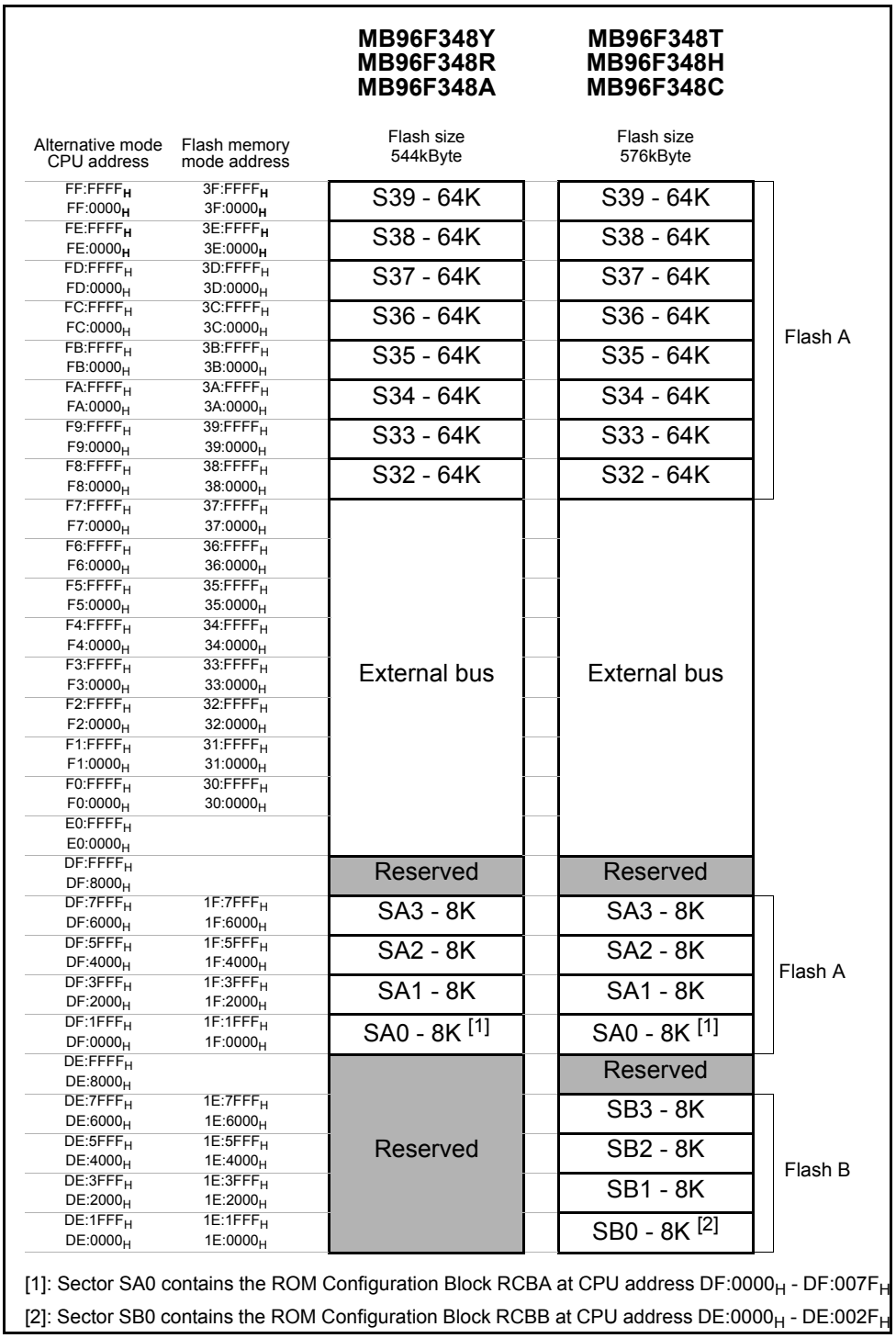
[2]: For External Bus end address and RAMSTART/END addresses, please refer to the table on the next page.

[3]: For EVA device, RAMSTART0 depends on the configuration of the emulated device.

[4]: For details about USER ROM area or DATA FLASH area, see the User ROM Memory Map For Flash Devices and User ROM Memory Map for Mask ROM Devices on the following pages.

The External Bus area and DMA area are only available if the device contains the corresponding resource.

The available RAM and ROM area depends on the device.



[1]: Sector SA0 contains the ROM Configuration Block RCBA at CPU address DF:0000$_H$ - DF:007F$_H$

[2]: Sector SB0 contains the ROM Configuration Block RCBB at CPU address DE:0000$_H$ - DE:002F$_H$

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$0000A1_H$	PPG4 - Duty cycle register			W
$0000A2_H$	PPG4 - Control status register Low	PCNL4	PCN4	R/W
$0000A3_H$	PPG4 - Control status register High	PCNH4		R/W
$0000A4_H$	PPG5 - Timer register		PTMR5	R
$0000A5_H$	PPG5 - Timer register			R
$0000A6_H$	PPG5 - Period setting register		PCSR5	W
$0000A7_H$	PPG5 - Period setting register			W
$0000A8_H$	PPG5 - Duty cycle register		PDUT5	W
$0000A9_H$	PPG5 - Duty cycle register			W
$0000AA_H$	PPG5 - Control status register Low	PCNL5	PCN5	R/W
$0000AB_H$	PPG5 - Control status register High	PCNH5		R/W
$0000AC_H$	I2C0 - Bus Status Register	IBSR0		R
$0000AD_H$	I2C0 - Bus Control Register	IBCR0		R/W
$0000AE_H$	I2C0 - Ten bit Slave address Register Low	ITBAL0	ITBA0	R/W
$0000AF_H$	I2C0 - Ten bit Slave address Register High	ITBAH0		R/W
$0000B0_H$	I2C0 - Ten bit Address mask Register Low	ITMKL0	ITMK0	R/W
$0000B1_H$	I2C0 - Ten bit Address mask Register High	ITMKH0		R/W
$0000B2_H$	I2C0 - Seven bit Slave address Register	ISBA0		R/W
$0000B3_H$	I2C0 - Seven bit Address mask Register	ISMK0		R/W
$0000B4_H$	I2C0 - Data Register	IDAR0		R/W
$0000B5_H$	I2C0 - Clock Control Register	ICCR0		R/W
$0000B6_H$	I2C1 - Bus Status Register	IBSR1		R
$0000B7_H$	I2C1 - Bus Control Register	IBCR1		R/W
$0000B8_H$	I2C1 - Ten bit Slave address Register Low	ITBAL1	ITBA1	R/W
$0000B9_H$	I2C1 - Ten bit Slave address Register High	ITBAH1		R/W
$0000BA_H$	I2C1 - Ten bit Address mask Register Low	ITMKL1	ITMK1	R/W
$0000BB_H$	I2C1 - Ten bit Address mask Register High	ITMKH1		R/W
$0000BC_H$	I2C1 - Seven bit Slave address Register	ISBA1		R/W
$0000BD_H$	I2C1 - Seven bit Address mask Register	ISMK1		R/W
$0000BE_H$	I2C1 - Data Register	IDAR1		R/W
$0000BF_H$	I2C1 - Clock Control Register	ICCR1		R/W
$0000C0_H$	USART0 - Serial Mode Register	SMR0		R/W

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000114_H	DMA2 - I/O register address pointer low byte	IOAL2	IOA2	R/W
000115_H	DMA2 - I/O register address pointer high byte	IOAH2		R/W
000116_H	DMA2 - Data counter low byte	DCTL2	DCT2	R/W
000117_H	DMA2 - Data counter high byte	DCTH2		R/W
000118_H	DMA3 - Buffer address pointer low byte	BAPL3		R/W
000119_H	DMA3 - Buffer address pointer middle byte	BAPM3		R/W
$00011A_H$	DMA3 - Buffer address pointer high byte	BAPH3		R/W
$00011B_H$	DMA3 - DMA control register	DMACS3		R/W
$00011C_H$	DMA3 - I/O register address pointer low byte	IOAL3	IOA3	R/W
$00011D_H$	DMA3 - I/O register address pointer high byte	IOAH3		R/W
$00011E_H$	DMA3 - Data counter low byte	DCTL3	DCT3	R/W
$00011F_H$	DMA3 - Data counter high byte	DCTH3		R/W
000120_H	DMA4 - Buffer address pointer low byte	BAPL4		R/W
000121_H	DMA4 - Buffer address pointer middle byte	BAPM4		R/W
000122_H	DMA4 - Buffer address pointer high byte	BAPH4		R/W
000123_H	DMA4 - DMA control register	DMACS4		R/W
000124_H	DMA4 - I/O register address pointer low byte	IOAL4	IOA4	R/W
000125_H	DMA4 - I/O register address pointer high byte	IOAH4		R/W
000126_H	DMA4 - Data counter low byte	DCTL4	DCT4	R/W
000127_H	DMA4 - Data counter high byte	DCTH4		R/W
000128_H	DMA5 - Buffer address pointer low byte	BAPL5		R/W
000129_H	DMA5 - Buffer address pointer middle byte	BAPM5		R/W
$00012A_H$	DMA5 - Buffer address pointer high byte	BAPH5		R/W
$00012B_H$	DMA5 - DMA control register	DMACS5		R/W
$00012C_H$	DMA5 - I/O register address pointer low byte	IOAL5	IOA5	R/W
$00012D_H$	DMA5 - I/O register address pointer high byte	IOAH5		R/W
$00012E_H$	DMA5 - Data counter low byte	DCTL5	DCT5	R/W
$00012F_H$	DMA5 - Data counter high byte	DCTH5		R/W
000130_H-$00017F_H$	Reserved			-
000180_H-$00037F_H$	CPU - General Purpose registers (RAM access)	GPR_RAM		R/W
000380_H	DMA0 - Interrupt select	DISEL0		R/W
000381_H	DMA1 - Interrupt select	DISEL1		R/W

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000382_H	DMA2 - Interrupt select	DISEL2		R/W
000383_H	DMA3 - Interrupt select	DISEL3		R/W
000384_H	DMA4 - Interrupt select	DISEL4		R/W
000385_H	DMA5 - Interrupt select	DISEL5		R/W
000386_H-$00038F_H$	Reserved			-
000390_H	DMA - Status register low byte	DSRL	DSR	R/W
000391_H	DMA - Status register high byte	DSRH		R/W
000392_H	DMA - Stop status register low byte	DSSRL	DSSR	R/W
000393_H	DMA - Stop status register high byte	DSSRH		R/W
000394_H	DMA - Enable register low byte	DERL	DER	R/W
000395_H	DMA - Enable register high byte	DERH		R/W
000396_H-$00039F_H$	Reserved			-
$0003A0_H$	Interrupt level register	ILR	ICR	R/W
$0003A1_H$	Interrupt index register	IDX		R/W
$0003A2_H$	Interrupt vector table base register Low	TBRL	TBR	R/W
$0003A3_H$	Interrupt vector table base register High	TBRH		R/W
$0003A4_H$	Delayed Interrupt register	DIRR		R/W
$0003A5_H$	Non Maskable Interrupt register	NMI		R/W
$0003A6_H$-$0003AB_H$	Reserved			-
$0003AC_H$	EDSU communication interrupt selection Low	EDSU2L	EDSU2	R/W
$0003AD_H$	EDSU communication interrupt selection High	EDSU2H		R/W
$0003AE_H$	ROM mirror control register	ROMM		R/W
$0003AF_H$	EDSU configuration register	EDSU		R/W
$0003B0_H$	Memory patch control/status register ch 0/1		PFCS0	R/W
$0003B1_H$	Memory patch control/status register ch 0/1			R/W
$0003B2_H$	Memory patch control/status register ch 2/3		PFCS1	R/W
$0003B3_H$	Memory patch control/status register ch 2/3			R/W
$0003B4_H$	Memory patch control/status register ch 4/5		PFCS2	R/W
$0003B5_H$	Memory patch control/status register ch 4/5			R/W
$0003B6_H$	Memory patch control/status register ch 6/7		PFCS3	R/W
$0003B7_H$	Memory patch control/status register ch 6/7			R/W
$0003B8_H$	Memory Patch function - Patch address 0 low	PFAL0		R/W

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000407_H	PLL Control register High	PLLCRH		R/W
000408_H	RC clock timer control register	RCTCR		R/W
000409_H	Main clock timer control register	MCTCR		R/W
$00040A_H$	Sub clock timer control register	SCTCR		R/W
$00040B_H$	Reset cause and clock status register with clear function	RCCSRC		R
$00040C_H$	Reset configuration register	RCR		R/W
$00040D_H$	Reset cause and clock status register	RCCSR		R
$00040E_H$	Watch dog timer configuration register	WDTC		R/W
$00040F_H$	Watch dog timer clear pattern register	WDTCP		W
000410_H-000414_H	Reserved			-
000415_H	Clock output activation register	COAR		R/W
000416_H	Clock output configuration register 0	COCR0		R/W
000417_H	Clock output configuration register 1	COCR1		R/W
000418_H	Clock Modulator control register	CMCR		R/W
000419_H	Reserved			-
$00041A_H$	Clock Modulator Parameter register Low	CMPRL	CMPR	R/W
$00041B_H$	Clock Modulator Parameter register High	CMPRH		R/W
$00041C_H$-$00042B_H$	Reserved			-
$00042C_H$	Voltage Regulator Control register	VRCR		R/W
$00042D_H$	Clock Input and LVD Control Register	CILCR		R/W
$00042E_H$-$00042F_H$	Reserved			-
000430_H	I/O Port P00 - Data Direction Register	DDR00		R/W
000431_H	I/O Port P01 - Data Direction Register	DDR01		R/W
000432_H	I/O Port P02 - Data Direction Register	DDR02		R/W
000433_H	I/O Port P03 - Data Direction Register	DDR03		R/W
000434_H	I/O Port P04 - Data Direction Register	DDR04		R/W
000435_H	I/O Port P05 - Data Direction Register	DDR05		R/W
000436_H	I/O Port P06 - Data Direction Register	DDR06		R/W
000437_H	I/O Port P07 - Data Direction Register	DDR07		R/W
000438_H	I/O Port P08 - Data Direction Register	DDR08		R/W
000439_H	I/O Port P09 - Data Direction Register	DDR09		R/W
$00043A_H$	I/O Port P10 - Data Direction Register	DDR10		R/W

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000715_H	CAN0 - IF1 Mask 1 Register High	IF1MSK1H0		R/W
000716_H	CAN0 - IF1 Mask 2 Register Low	IF1MSK2L0	IF1MSK20	R/W
000717_H	CAN0 - IF1 Mask 2 Register High	IF1MSK2H0		R/W
000718_H	CAN0 - IF1 Arbitration 1 Register Low	IF1ARB1L0	IF1ARB10	R/W
000719_H	CAN0 - IF1 Arbitration 1 Register High	IF1ARB1H0		R/W
$00071A_H$	CAN0 - IF1 Arbitration 2 Register Low	IF1ARB2L0	IF1ARB20	R/W
$00071B_H$	CAN0 - IF1 Arbitration 2 Register High	IF1ARB2H0		R/W
$00071C_H$	CAN0 - IF1 Message Control Register Low	IF1MCTRL0	IF1MCTR0	R/W
$00071D_H$	CAN0 - IF1 Message Control Register High	IF1MCTRH0		R/W
$00071E_H$	CAN0 - IF1 Data A1 Low	IF1DTA1L0	IF1DTA10	R/W
$00071F_H$	CAN0 - IF1 Data A1 High	IF1DTA1H0		R/W
000720_H	CAN0 - IF1 Data A2 Low	IF1DTA2L0	IF1DTA20	R/W
000721_H	CAN0 - IF1 Data A2 High	IF1DTA2H0		R/W
000722_H	CAN0 - IF1 Data B1 Low	IF1DTB1L0	IF1DTB10	R/W
000723_H	CAN0 - IF1 Data B1 High	IF1DTB1H0		R/W
000724_H	CAN0 - IF1 Data B2 Low	IF1DTB2L0	IF1DTB20	R/W
000725_H	CAN0 - IF1 Data B2 High	IF1DTB2H0		R/W
000726_H-$00073F_H$	Reserved			-
000740_H	CAN0 - IF2 Command request register Low	IF2CREQL0	IF2CREQ0	R/W
000741_H	CAN0 - IF2 Command request register High	IF2CREQH0		R/W
000742_H	CAN0 - IF2 Command Mask register Low	IF2CMSKL0	IF2CMSK0	R/W
000743_H	CAN0 - IF2 Command Mask register High (reserved)	IF2CMSKH0		R
000744_H	CAN0 - IF2 Mask 1 Register Low	IF2MSK1L0	IF2MSK10	R/W
000745_H	CAN0 - IF2 Mask 1 Register High	IF2MSK1H0		R/W
000746_H	CAN0 - IF2 Mask 2 Register Low	IF2MSK2L0	IF2MSK20	R/W
000747_H	CAN0 - IF2 Mask 2 Register High	IF2MSK2H0		R/W
000748_H	CAN0 - IF2 Arbitration 1 Register Low	IF2ARB1L0	IF2ARB10	R/W
000749_H	CAN0 - IF2 Arbitration 1 Register High	IF2ARB1H0		R/W
$00074A_H$	CAN0 - IF2 Arbitration 2 Register Low	IF2ARB2L0	IF2ARB20	R/W
$00074B_H$	CAN0 - IF2 Arbitration 2 Register High	IF2ARB2H0		R/W
$00074C_H$	CAN0 - IF2 Message Control Register Low	IF2MCTRL0	IF2MCTR0	R/W
$00074D_H$	CAN0 - IF2 Message Control Register High	IF2MCTRH0		R/W

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000822_H	CAN1 - IF1 Data B1 Low	IF1DTB1L1	IF1DTB11	R/W
000823_H	CAN1 - IF1 Data B1 High	IF1DTB1H1		R/W
000824_H	CAN1 - IF1 Data B2 Low	IF1DTB2L1	IF1DTB21	R/W
000825_H	CAN1 - IF1 Data B2 High	IF1DTB2H1		R/W
000826_H-$00083F_H$	Reserved			-
000840_H	CAN1 - IF2 Command request register Low	IF2CREQL1	IF2CREQ1	R/W
000841_H	CAN1 - IF2 Command request register High	IF2CREQH1		R/W
000842_H	CAN1 - IF2 Command Mask register Low	IF2CMSKL1	IF2CMSK1	R/W
000843_H	CAN1 - IF2 Command Mask register High (reserved)	IF2CMSKH1		R
000844_H	CAN1 - IF2 Mask 1 Register Low	IF2MSK1L1	IF2MSK11	R/W
000845_H	CAN1 - IF2 Mask 1 Register High	IF2MSK1H1		R/W
000846_H	CAN1 - IF2 Mask 2 Register Low	IF2MSK2L1	IF2MSK21	R/W
000847_H	CAN1 - IF2 Mask 2 Register High	IF2MSK2H1		R/W
000848_H	CAN1 - IF2 Arbitration 1 Register Low	IF2ARB1L1	IF2ARB11	R/W
000849_H	CAN1 - IF2 Arbitration 1 Register High	IF2ARB1H1		R/W
$00084A_H$	CAN1 - IF2 Arbitration 2 Register Low	IF2ARB2L1	IF2ARB21	R/W
$00084B_H$	CAN1 - IF2 Arbitration 2 Register High	IF2ARB2H1		R/W
$00084C_H$	CAN1 - IF2 Message Control Register Low	IF2MCTRL1	IF2MCTR1	R/W
$00084D_H$	CAN1 - IF2 Message Control Register High	IF2MCTRH1		R/W
$00084E_H$	CAN1 - IF2 Data A1 Low	IF2DTA1L1	IF2DTA11	R/W
$00084F_H$	CAN1 - IF2 Data A1 High	IF2DTA1H1		R/W
000850_H	CAN1 - IF2 Data A2 Low	IF2DTA2L1	IF2DTA21	R/W
000851_H	CAN1 - IF2 Data A2 High	IF2DTA2H1		R/W
000852_H	CAN1 - IF2 Data B1 Low	IF2DTB1L1	IF2DTB11	R/W
000853_H	CAN1 - IF2 Data B1 High	IF2DTB1H1		R/W
000854_H	CAN1 - IF2 Data B2 Low	IF2DTB2L1	IF2DTB21	R/W
000855_H	CAN1 - IF2 Data B2 High	IF2DTB2H1		R/W
000856_H-$00087F_H$	Reserved			-
000880_H	CAN1 - Transmission Request 1 Register Low	TREQR1L1	TREQR11	R
000881_H	CAN1 - Transmission Request 1 Register High	TREQR1H1		R
000882_H	CAN1 - Transmission Request 2 Register Low	TREQR2L1	TREQR21	R
000883_H	CAN1 - Transmission Request 2 Register High	TREQR2H1		R

14. Electrical Characteristics

14.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	V_{SS} - 0.3	V_{SS} + 6.0	V	
	AV_{CC}	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_{CC} = AV_{CC}$ [1]
AD Converter voltage references	AVRH, AVRL	V_{SS} - 0.3	V_{SS} + 6.0	V	$AV_{CC} \geq AVRH$, $AV_{CC} \geq AVRL$, $AVRH > AVRL$, $AVRL \geq AV_{SS}$
Input voltage	V_I	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_I \leq V_{CC}$ + 0.3V [2]
Output voltage	V_O	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_O \leq V_{CC}$ + 0.3V [2]
Maximum Clamp Current	I_{CLAMP}	-4.0	+4.0	mA	Applicable to general purposeI/O pins [3]
Total Maximum Clamp Current	$\Sigma\|I_{CLAMP}\|$	-	40	mA	Applicable to general purposeI/O pins [3]
“L” level maximum output current	I_{OL1}	-	15	mA	Normal outputs with driving strength set to 5mA
“L” level average output current	I_{OLAV1}	-	5	mA	Normal outputs with driving strength set to 5mA
“L” level maximum overall output current	ΣI_{OL1}	-	100	mA	Normal outputs
“L” level average overall output current	ΣI_{OLAV1}	-	50	mA	Normal outputs
”H” level maximum output current	I_{OH1}	-	-15	mA	Normal outputs with driving strength set to 5mA
”H” level average output current	I_{OHAV1}	-	-5	mA	Normal outputs with driving strength set to 5mA
”H” level maximum overall output current	ΣI_{OH1}	-	-100	mA	Normal outputs
”H” level average overall output current	ΣI_{OHAV1}	-	-50	mA	Normal outputs
Permitted Power dissipation (Flash devices in QFP package) [4]	P_D	-	430[5]	mW	T_A=105°C
		-	750[5]	mW	T_A=90°C
		-	540[5]	mW	T_A=125°C, no Flash program/erase [6]
Permitted Power dissipation (MB96F346/F347/F348 in LQFP package) [4]	P_D	-	375[5]	mW	T_A=105°C
		-	750[5]	mW	T_A=85°C
		-	470[5]	mW	T_A=125°C, no Flash program/erase [6]
		-	560[5]	mW	T_A=120°C, no Flash program/erase [6]
Permitted Power dissipation (MB96F345 in LQFP package) [4]	P_D	-	335[5]	mW	T_A=105°C
		-	670[5]	mW	T_A=85°C
		-	840[5]	mW	T_A=75°C
		-	420[5]	mW	T_A=125°C, no Flash program/erase [6]
		-	590[5]	mW	T_A=115°C, no Flash program/erase [6]

14.4.8 Bus Timing (Read)

(T_A = –40°C to +125°C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

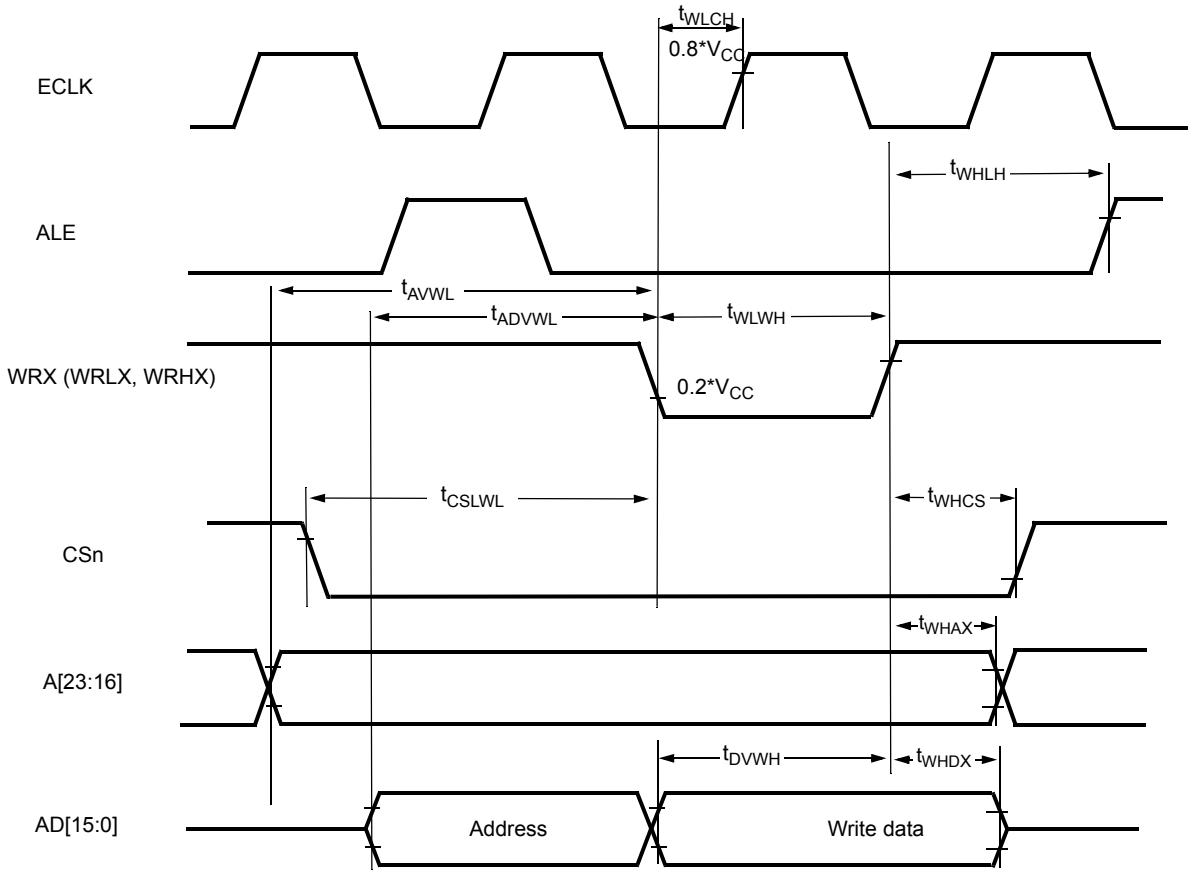
Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
ALE pulse width	t_{LHLL}	ALE	EACL:STS=0 and EACL:ACE=0	$t_{CYC}/2 - 5$	-	ns	
			EACL:STS=1	$t_{CYC} - 5$	-		
			EACL:STS=0 and EACL:ACE=1	$3t_{CYC}/2 - 5$	-		
Valid address ⇒ ALE ↓ time	t_{AVLL}	ALE, A[23:16],	EACL:STS=0 and EACL:ACE=0	$t_{CYC} - 15$	-	ns	
			EACL:STS=1 and EACL:ACE=0	$3t_{CYC}/2 - 15$	-		
			EACL:STS=0 and EACL:ACE=1	$2t_{CYC} - 15$	-		
			EACL:STS=1 and EACL:ACE=1	$5t_{CYC}/2 - 15$	-		
	t_{ADVLL}	ALE,AD[15:0]	EACL:STS=0 and EACL:ACE=0	$t_{CYC}/2 - 15$	-	ns	
			EACL:STS=1 and EACL:ACE=0	$t_{CYC} - 15$	-		
			EACL:STS=0 and EACL:ACE=1	$3t_{CYC}/2 - 15$	-		
			EACL:STS=1 and EACL:ACE=1	$2t_{CYC} - 15$	-		
ALE ↓ ⇒ Address valid time	t_{LLAX}	ALE, AD[15:0]	EACL:STS=0	$t_{CYC}/2 - 15$	-	ns	
			EACL:STS=1	-15	-		
Valid address ⇒ RDX ↓ time	t_{AVRL}	RDX, A[23:16]	EACL:ACE=0	$3t_{CYC}/2 - 15$	-	ns	
			EACL:ACE=1	$5t_{CYC}/2 - 15$	-		
	t_{ADVRL}	RDX, AD[15:0]	EACL:ACE=0	$t_{CYC} - 15$	-	ns	
			EACL:ACE=1	$2t_{CYC} - 15$	-		
Valid address ⇒ Valid data input	t_{AVDV}	A[23:16], AD[15:0]	EACL:ACE=0	-	$3t_{CYC} - 55$	ns	w/o cycle extension
			EACL:ACE=1	-	$4t_{CYC} - 55$		
	t_{ADVDV}	AD[15:0]	EACL:ACE=0	-	$5t_{CYC}/2 - 55$	ns	w/o cycle extension
			EACL:ACE=1	-	$7t_{CYC}/2 - 55$		
RDX pulse width	t_{RLRH}	RDX	-	$3\ t_{CYC}/2 - 5$	-	ns	w/o cycle extension
RDX ↓ ⇒ Valid data input	t_{RLDV}	RDX, AD[15:0]	-	-	$3\ t_{CYC}/2 - 50$	ns	w/o cycle extension
RDX ↑ ⇒ Data hold time	t_{RHDX}	RDX, AD[15:0]	-	0	-	ns	
Address valid ⇒ Data hold time	t_{AXDX}	A[23:16], AD[15:0]	-	0	-	ns	

(T_A = –40°C to +125°C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
RDX ↑ ⇒ ALE ↑ time	t_{RHLH}	RDX, ALE	EACL:STS=1 and EACL:ACE=1	$3t_{CYC}/2 - 10$	-	ns	
			other ECL:STS, EACL:ACE setting	$t_{CYC}/2 - 10$	-		
Valid address ⇒ ECLK ↑ time	t_{AVCH}	A[23:16], ECLK	-	$t_{CYC} - 15$	-	ns	
	t_{ADVCH}	AD[15:0], ECLK		$t_{CYC}/2 - 15$	-		
RDX ↓ ⇒ ECLK ↑ time	t_{RLCH}	RDX, ECLK	-	$t_{CYC}/2 - 10$	-	ns	
ALE ↓ ⇒ RDX ↓ time	t_{LLRL}	ALE, RDX	EACL:STS=0	$t_{CYC}/2 - 10$	-	ns	
			EACL:STS=1	– 10	-		
ECLK↑ ⇒ Valid data input	t_{CHDV}	AD[15:0], ECLK	-	-	$t_{CYC} - 50$	ns	

(T_A = –40°C to +125°C, V_{CC} = 3.0 to 4.5V, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
ALE pulse width	t_{LHLL}	ALE	EACL:STS=0 and EACL:ACE=0	$t_{CYC}/2 - 8$	-	ns	
			EACL:STS=1	$t_{CYC} - 8$	-		
			EACL:STS=0 and EACL:ACE=1	$3t_{CYC}/2 - 8$	-		
Valid address ⇒ ALE ↓ time	t_{AVLL}	ALE, A[23:16],	EACL:STS=0 and EACL:ACE=0	$t_{CYC} - 20$	-	ns	
			EACL:STS=1 and EACL:ACE=0	$3t_{CYC}/2 - 20$	-		
			EACL:STS=0 and EACL:ACE=1	$2t_{CYC} - 20$	-		
			EACL:STS=1 and EACL:ACE=1	$5t_{CYC}/2 - 20$	-		
	t_{ADVLL}	ALE, AD[15:0]	EACL:STS=0 and EACL:ACE=0	$t_{CYC}/2 - 20$	-	ns	
			EACL:STS=1 and EACL:ACE=0	$t_{CYC} - 20$	-		
			EACL:STS=0 and EACL:ACE=1	$3t_{CYC}/2 - 20$	-		
			EACL:STS=1 and EACL:ACE=1	$2t_{CYC} - 20$	-		
ALE ↓ ⇒ Address valid time	t_{LLAX}	ALE, AD[15:0]	EACL:STS=0	$t_{CYC}/2 - 20$	-	ns	
			EACL:STS=1	-20	-		
Valid address ⇒ RDX ↓ time	t_{AVRL}	RDX, A[23:16]	EACL:ACE=0	$3t_{CYC}/2 - 20$	-	ns	
			EACL:ACE=1	$5t_{CYC}/2 - 20$	-		
	t_{ADVRL}	RDX, AD[15:0]	EACL:ACE=0	$t_{CYC} - 20$	-	ns	
			EACL:ACE=1	$2t_{CYC} - 20$	-		



Refer to the Hardware Manual for detailed Timing Charts

14.4.10 Ready Input Timing

(T_A = –40°C to +125°C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Test Condition	Rated Value		Units	Remarks
				Min	Max		
RDY setup time	t_{RYHS}	RDY	-	35	-	ns	
RDY hold time	t_{RYHH}	RDY		0	-	ns	

(T_A = –40°C to +125°C, V_{CC} = 3.0 to 4.5V, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Test Condition	Rated Value		Units	Remarks
				Min	Max		
RDY setup time	t_{RYHS}	RDY	-	45	-	ns	
RDY hold time	t_{RYHH}	RDY		0	-	ns	

Note: If the RDY setup time is insufficient, use the auto-ready function.

14.4.13 I²C Timing

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V,V_{SS} = AV_{SS} =0V)

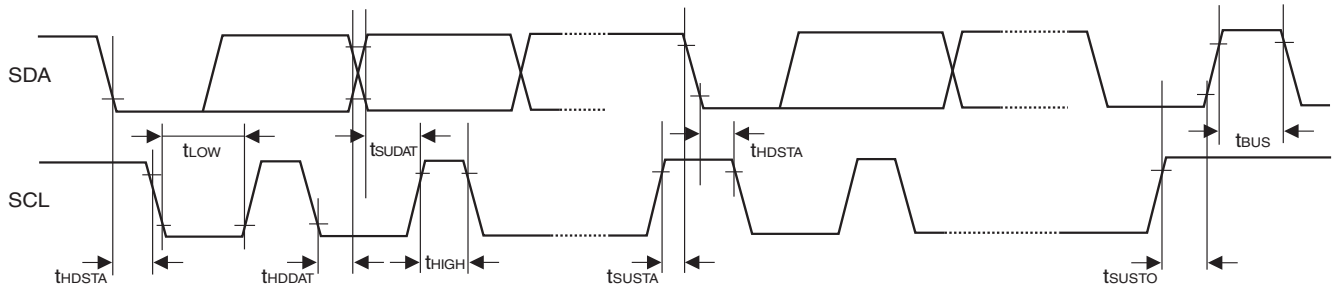
Parameter	Symbol	Condition	Standard-mode		Fast-mode[4]		Unit
			Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	R = 1.7 kΩ, C = 50 pF[1]	0	100	0	400	kHz
Hold time (repeated) START condition SDA↓→SCL¬	t_{HDSTA}		4.0	-	0.6	-	µs
"L" width of the SCL clock	t_{LOW}		4.7	-	1.3	-	µs
"H" width of the SCL clock	t_{HIGH}		4.0	-	0.6	-	µs
Set-up time for a repeated START condition SCL↓→SDA↑	t_{SUSTA}		4.7	-	0.6	-	µs
Data hold timeSCL↑→SDA↑↓	t_{HDDAT}		0	3.45[2]	0	0.9[3]	µs
Data set-up timeSDA↑↓→SCL↑	t_{SUDAT}		250	-	100	-	ns
Set-up time for STOP conditionSCL↑→SDA↑	t_{SUSTO}		4.0	-	0.6	-	µs
Bus free time between a STOP and START condition	t_{BUS}		4.7	-	1.3	-	µs

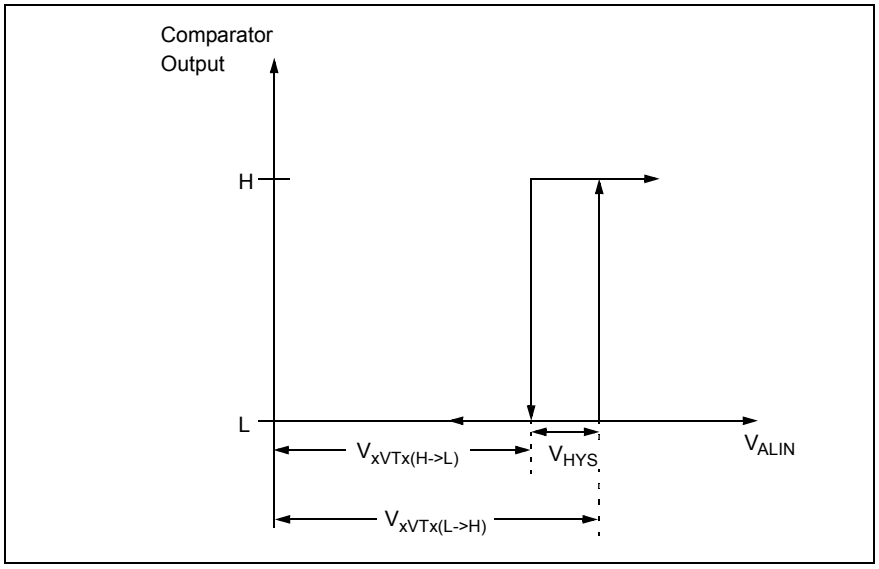
[1] : R,C: Pull-up resistor and load capacitor of the SCL and SDA lines.

[2]: The maximum t_{HDDAT} have only to be met if the device does not stretch the "L" width (t_{LOW}) of the SCL signal.

[3] : A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement t_{SUDAT}≥ 250 ns must then be met.

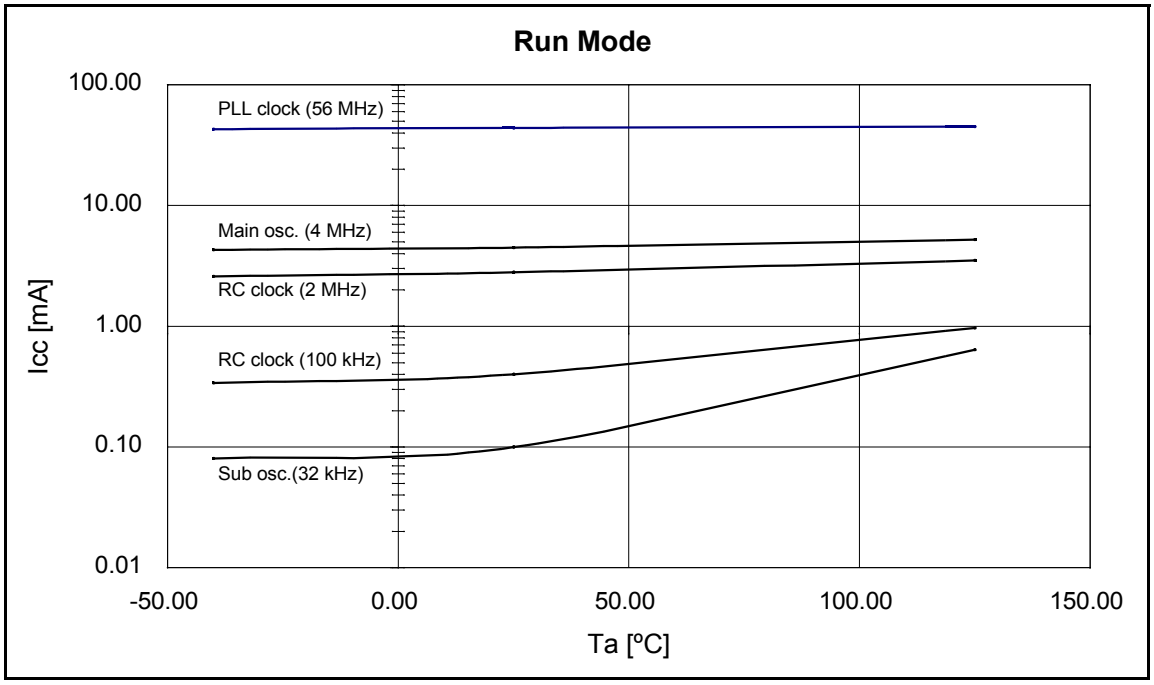
[4] : For use at over 100 kHz, set the peripheral clock 1 to at least 6 MHz.

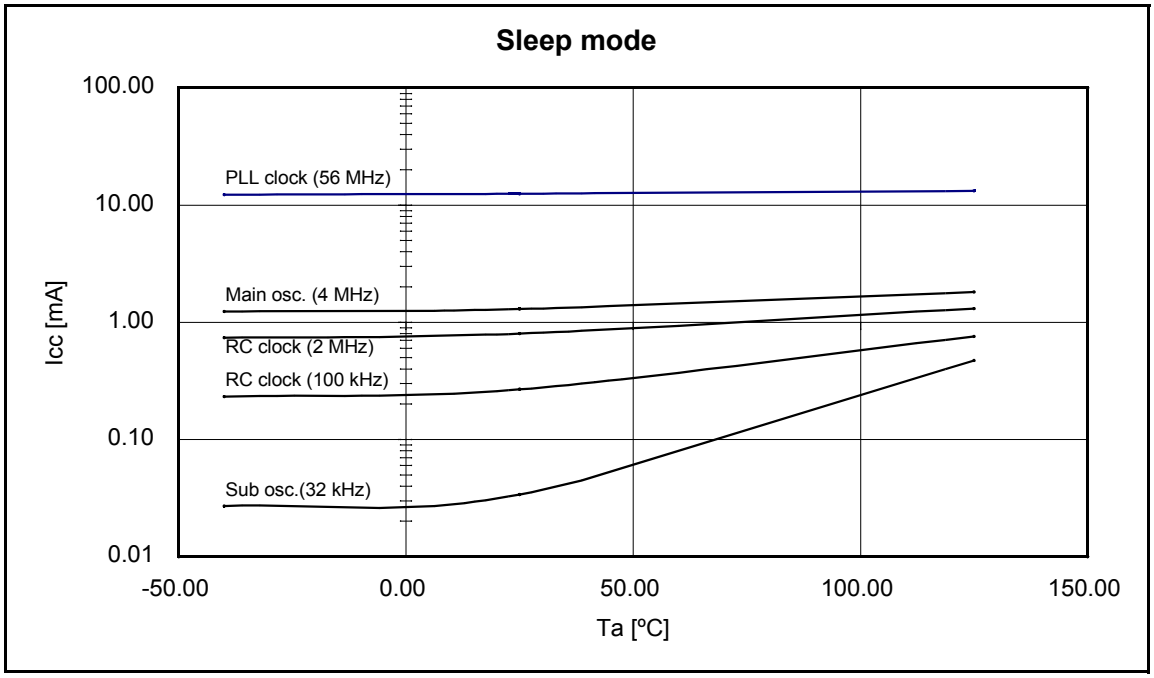



Comparator
Output
H
L
$V_{xVTx(H->L)}$
V_{HYS}
V_{ALIN}
$V_{xVTx(L->H)}$

15. Example Characteristics

The diagrams below show the characteristics of one measured sample with typical process parameters.





19. Revision History

Revision	Date	Modification
Prelim 1	2007-05-07	Creation
Prelim 2	2007-05-10	External bus hold timing update
Prelim 3	2007-05-23	Electrical characteristics updates
Prelim 4	2007-08-02	Electrical characteristics updates, Product lineup, changes and ordering information
Prelim 5	2007-09-12	Addition of the electrical characteristic examples and the LVD characteristics specifications, updates of the DC characteristics. Pin circuit type drawing modifications.
Prelim 6	2007-11-21	LVD typo correction. Update of the DC characteristics. Typos corrections.
Prelim 7	2007-12-04	Absolute maximum rating asterisks numbering corrected. Typos page 59: Hardware -> Hardware. IO map table regenerated. Typos corrections. IO circuit drawings modified. Renaming of the Main/Satellite Flash into Flash memory A/B. Memory map reworked.
Prelim 8	2008-02-04	■ Satellite Flash -> 32kB Data Flash ■ MB96345 added (under development) ■ MB96F348 TSA/HSA/TWA/HWA removed (outdated devices) ■ Block diagram and pin assignment corrected (existing resource pins) ■ Pin function table corrected ■ I/O circuit type diagrams corrected ■ Memory map cleaned up ■ "Flash sector configuration" replaced by corrected "User ROM Memory map for Flash devices", “ROM configuration” replaced by “User ROM Memory map for Mask ROM devices” ■ Parallel Flash programming pinning removed ■ IO map table regenerated: ❒ Port register: Naming style corrected ❒ Memory control registers renamed (Main/Sat -> A/B) ❒ addresses after 000BFFh removed ■ Absolute maximum ratings: Pd and Ta specified more precisely ■ oscillator input levels in oscillation mode with external clock added ■ Run and Sleep mode currents: 96/48MHz and 72/36MHz settings added ■ Run mode current spec in 48/24MHz mode corrected ■ Maximum CLKS1/2 frequency for all devices correctly specified ■ Maximum CLKP2 for MB96F34xY/R/Axx corrected ■ External bus timings: missing conditions added and readability improved ■ Alarm comparator spec updated (transition voltages defined) ■ MB96V300A removed ■ Ordering information updated ■ Typos and formatting corrected

20. Main Changes in this Edition

Page	Section	Change Results
89	Electrical Characteristics 14.5. Analog Digital Converter	Corrected "Value" and "Unit" of Zero reading voltage. (AVRL - 1.5 → AVRL - 1.5 LSB AVRL + 0.5 → AVRL + 0.5 LSB AVRL + 2.5 → AVRL + 2.5 LSB LSB → V) Corrected "Value" and "Unit" of Full scale reading voltage. (AVRH - 3.5 → AVRH - 3.5 LSB AVRH - 1.5 → AVRH - 1.5 LSB AVRH + 0.5 → AVRH + 0.5 LSB LSB → V)

NOTE: Please see "Document History" for later revised information.

Document History

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Document Title: MB96345/346, MB96F345, MB96F346/F347/F348, F^{2}MC-16FX, MB96340 Series, 16-bit Proprietary Microcontroller Datasheet **Document Number: 002-04579**				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	_	AKIH	06/17/2009	Migrated to Cypress and assigned document number 002-04579. No change to document contents or format.
*A	5198948	AKIH	04/04/2016	Updated to Cypress template