# Infineon Technologies - MB96F347ASBPMC-GSE2 Datasheet

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Discontinued at Digi-Key |
| Core Processor | F²MC-16FX |
| Core Size | 16-Bit |
| Speed | 56MHz |
| Connectivity | CANbus, EBI/EMI, I²C, LINbus, SCI, UART/USART |
| Peripherals | DMA, LVD, LVR, POR, PWM, WDT |
| Number of I/O | 82 |
| Program Memory Size | 416KB (416K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 5.5V |
| Data Converters | A/D 24x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | 100-LQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/mb96f347asbpmc-gse2 |

# Features

| Feature | Description |
|---|---|
| Technology | ■ 0.18μm CMOS |
| CPU | ■ F$^2$MC-16FX CPU<br>■ Up to 56 MHz internal, 17.8 ns instruction cycle time<br>■ Optimized instruction set for controller applications (bit, byte, word and long-word data types; 23 different addressing modes; barrel shift; variety of pointers)<br>■ 8-byte instruction execution queue<br>■ Signed multiply (16-bit × 16-bit) and divide (32-bit/16-bit) instructions available |
| System clock | ■ On-chip PLL clock multiplier (x1 - x25, x1 when PLL stop)<br>■ 3 MHz - 16 MHz external crystal oscillator clock (maximum frequency when using ceramic resonator depends on Q-factor).<br>■ Up to 56 MHz external clock for devices with fast clock input feature<br>■ 32-100 kHz subsystem quartz clock<br>■ 100kHz/2MHz internal RC clock for quick and safe startup, oscillator stop detection, watchdog<br>■ Clock source selectable from main- and subclock oscillator (part number suffix “W”) and on-chip RC oscillator, independently for CPU and 2 clock domains of peripherals.<br>■ Low Power Consumption - 13 operating modes : (different Run, Sleep, Timer modes, Stop mode)<br>■ Clock modulator |
| On-chip voltage regulator | ■ Internal voltage regulator supports reduced internal MCU voltage, offering low EMI and low power consumption figures |
| Low voltage reset | ■ Reset is generated when supply voltage is below minimum. |
| Code Security | ■ Protects ROM content from unintended read-out |
| Memory Patch Function | ■ Replaces ROM content<br>■ Can also be used to implement embedded debug support |
| DMA | ■ Automatic transfer function independent of CPU, can be assigned freely to resources |
| Interrupts | ■ Fast Interrupt processing<br>■ 8 programmable priority levels<br>■ Non-Maskable Interrupt (NMI) |
| Timers | ■ Three independent clock timers (23-bit RC clock timer, 23-bit Main clock timer, 17-bit Sub clock timer)<br>■ Watchdog Timer |
| CAN | ■ Supports CAN protocol version 2.0 part A and B<br>■ ISO16845 certified<br>■ Bit rates up to 1 Mbit/s<br>■ 32 message objects<br>■ Each message object has its own identifier mask<br>■ Programmable FIFO mode (concatenation of message objects)<br>■ Maskable interrupt<br>■ Disabled Automatic Retransmission mode for Time Triggered CAN applications<br>■ Programmable loop-back mode for self-test operation |
| USART | ■ Full duplex USARTs (SCI/LIN)<br>■ Wide range of baud rate settings using a dedicated reload timer<br>■ Special synchronous options for adapting to different synchronous serial protocols<br>■ LIN functionality working either as master or slave LIN device |

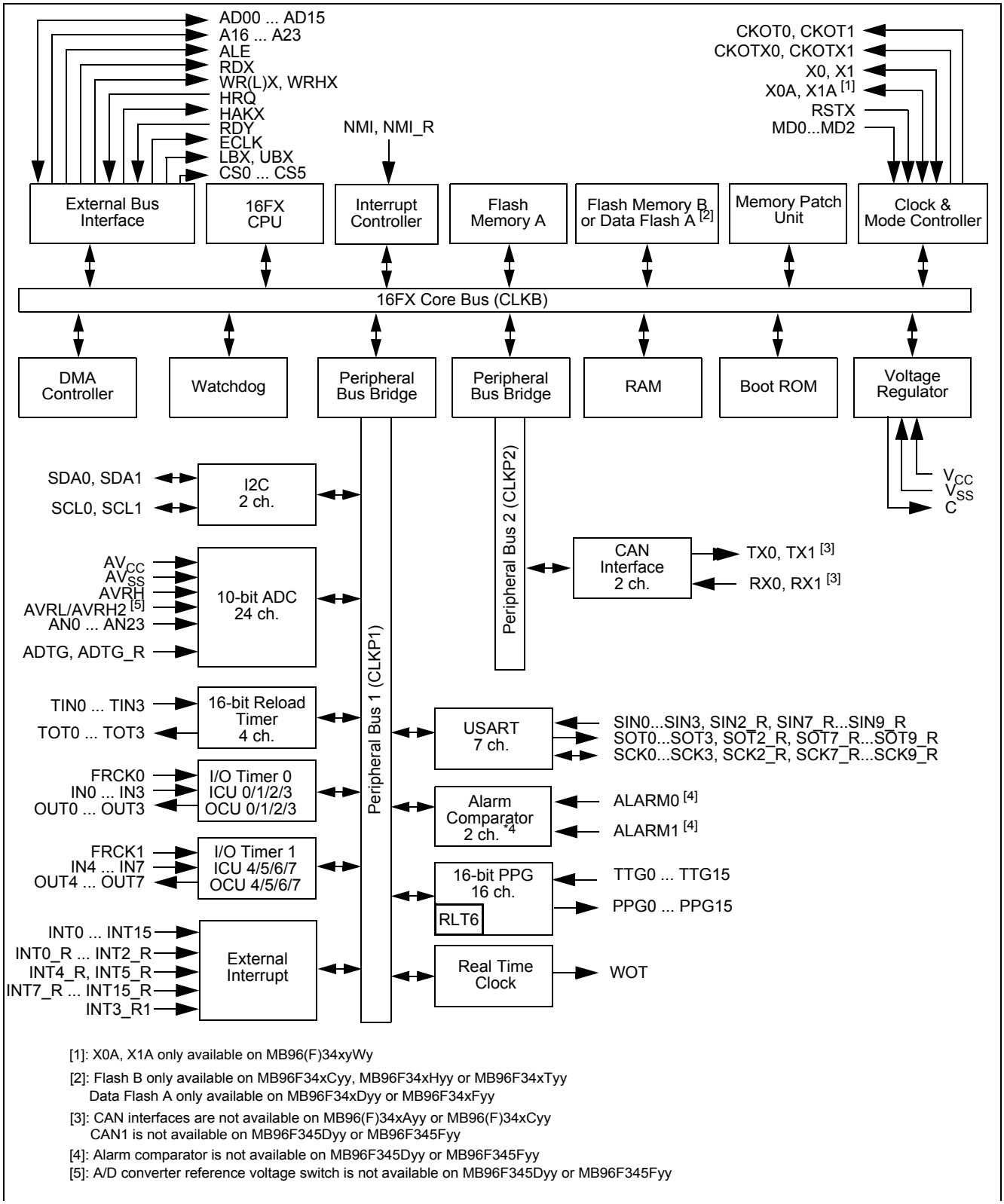
| Feature | Description |
|---|---|
| Alarm comparator | ■ Monitors an external voltage and generates an interrupt in case of a voltage lower or higher than the defined thresholds<br>■ Threshold voltages defined externally or generated internally<br>■ Status is readable, interrupts can be masked separately |
| I/O Ports | ■ Virtually all external pins can be used as general purpose I/O<br>■ All push-pull outputs (except when used as I2C SDA/SCL line)<br>■ Bit-wise programmable as input/output or peripheral signal<br>■ Bit-wise programmable input enable<br>■ Bit-wise programmable input levels: Automotive / CMOS-Schmitt trigger / TTL (TTL levels not supported by all devices)<br>■ Bit-wise programmable pull-up resistor<br>■ Bit-wise programmable output driving strength for EMI optimization |
| Packages | ■ 100-pin plastic QFP and LQFP |
| Flash Memory | ■ Supports automatic programming, Embedded Algorithm<br>■ Write/Erase/Erase-Suspend/Resume commands<br>■ A flag indicating completion of the algorithm<br>■ Number of erase cycles: 10,000 times<br>■ Data retention time: 20 years<br>■ Erase can be performed on each sector individually<br>■ Sector protection<br>■ Flash Security feature to protect the content of the Flash<br>■ Low voltage detection during Flash erase |

# 1. Product Lineup

| Features | | MB96V300B | MB96(F)34x |
|---|---|---|---|
| Product type | | Evaluation sample | Flash product: MB96F34x Mask ROM product: MB9634x |
| Product options | | | |
| YS | | NA | Low voltage reset persistently on / Single clock |
| RS | | | Low voltage reset can be disabled / Single clock |
| YW | | | Low voltage reset persistently on / Dual clock |
| RW | | | Low voltage reset can be disabled / Dual clock |
| TS | | | indep. 32KB Flash / Low voltage reset persistently on / Single clock |
| HS | | | indep. 32KB Flash / Low voltage reset can be disabled / Single clock |
| TW | | | indep. 32KB Flash / Low voltage reset persistently on / Dual clock |
| HW | | | indep. 32KB Flash / Low voltage reset can be disabled / Dual clock |
| FS | | | 64KB Data Flash / Low voltage reset persistently on / Single clock |
| DS | | | 64KB Data Flash / Low voltage reset can be disabled / Single clock |
| FW | | | 64KB Data Flash / Low voltage reset persistently on / Dual clock |
| DW | | | 64KB Data Flash / Low voltage reset can be disabled / Dual clock |
| AS | | | No CAN / Low voltage reset can be disabled / Single clock devices |
| CS | | | No CAN / indep. 32KB Flash / Low voltage reset can be disabled / Single clock |
| AW | | | No CAN / Low voltage reset can be disabled / Dual clock |
| CW | | | No CAN / indep. 32KB Flash / Low voltage reset can be disabled / Dual clock |
| Flash/ROM | RAM | | |
| 160KB | 8KB | ROM/Flash memory emulation by external RAM, 92KB internal RAM | MB96345Y [1], MB96345R [1] |
| 224KB [Flash A: 160KB, Data Flash A: 64KB] | 8KB | | MB96F345F [1], MB96F345D [1] |
| 288KB | 16KB | | MB96F346Y, MB96346Y [1], MB96F346R, MB96346R [1], MB96F346A |
| 416KB | 16KB | | MB96F347Y, MB96F347R, MB96F347A |
| 544KB | 24KB | | MB96F348Y, MB96F348R, MB96F348A |
| 576KB [Flash A: 544KB, Flash B: 32KB] | 24KB | | MB96F348T, MB96F348H, MB96F348C |
| Package | | BGA416 | FPT-100P-M20 FPT-100P-M22 |
| DMA | | 16 channels | 6 channels |
| USART | | 10 channels | 7 channels |

## 2. Block Diagram

**Figure 1. Block diagram of MB96(F)34x**




[1]: X0A, X1A only available on MB96(F)34xyWy

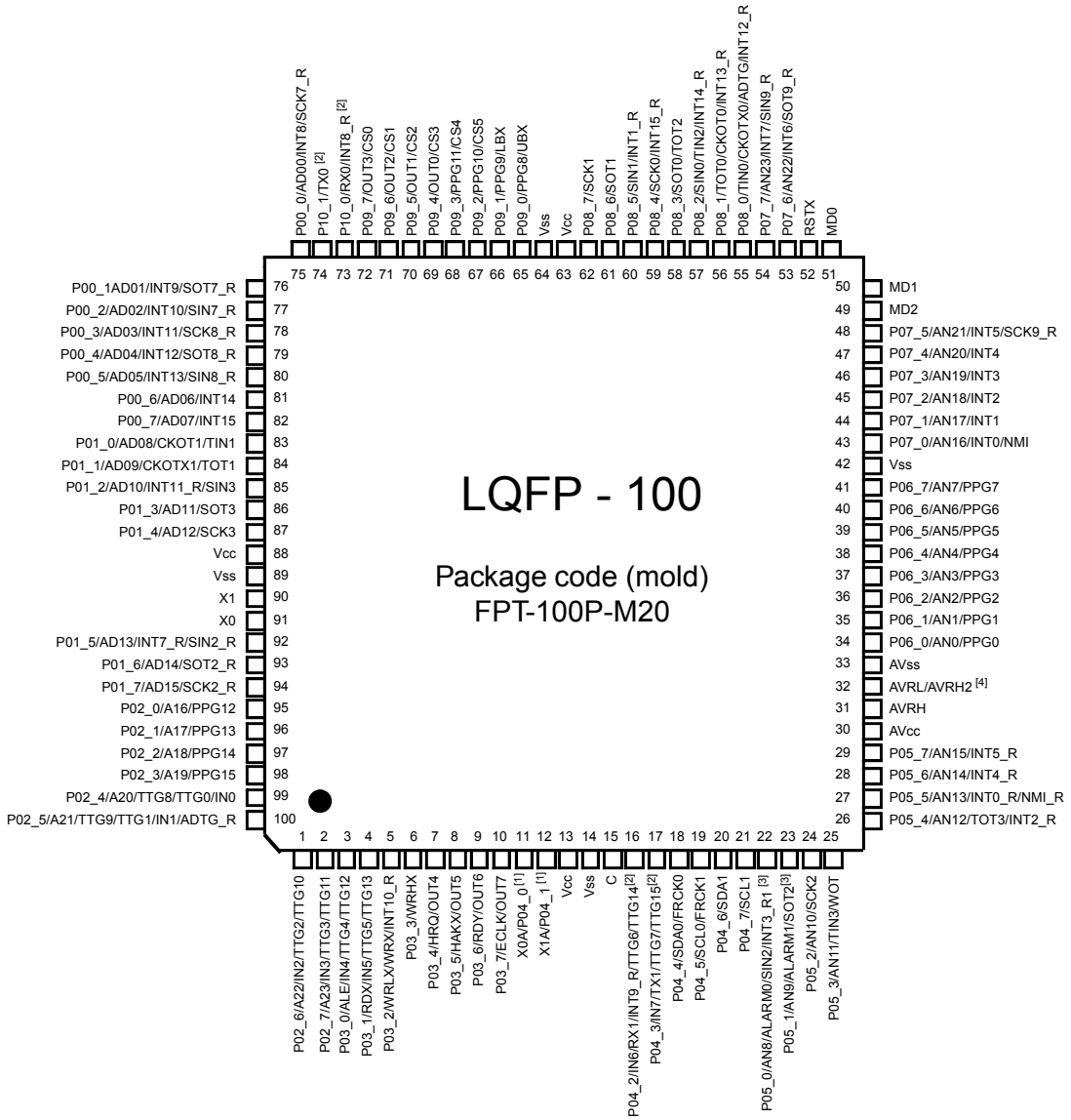
[2]: Flash B only available on MB96F34xCyy, MB96F34xHyy or MB96F34xTyy
Data Flash A only available on MB96F34xDyy or MB96F34xFyy

[3]: CAN interfaces are not available on MB96(F)34xAyy or MB96(F)34xCyy
CAN1 is not available on MB96F345Dyy or MB96F345Fyy

[4]: Alarm comparator is not available on MB96F345Dyy or MB96F345Fyy

[5]: A/D converter reference voltage switch is not available on MB96F345Dyy or MB96F345Fyy

**Figure 3. Pin assignment of MB96(F)34x (FPT-100P-M20)**




[1]: MB96(F)34xyWy: X0A, X1A
MB96(F)34xySy: P04_0, P04_1

[2]: TX0, RX0, TX1, RX1 are not available on MB96(F)34xAyy or MB96(F)34xCyy
TX1, RX1 are not available on MB96F345Dyy or MB96F345Fyy

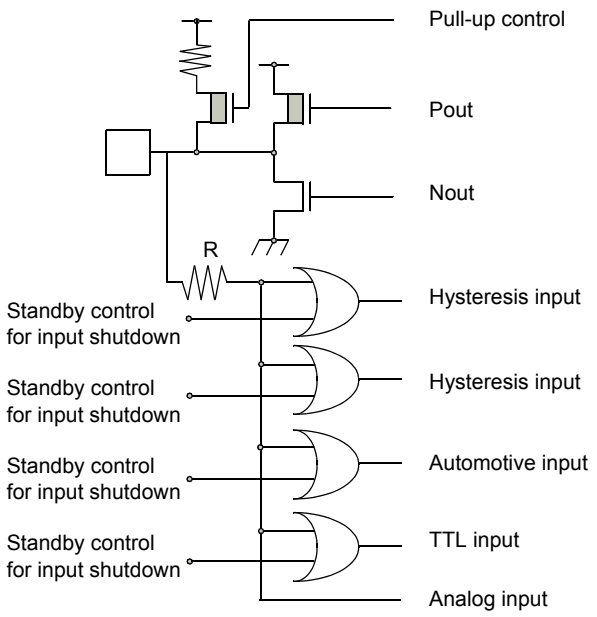
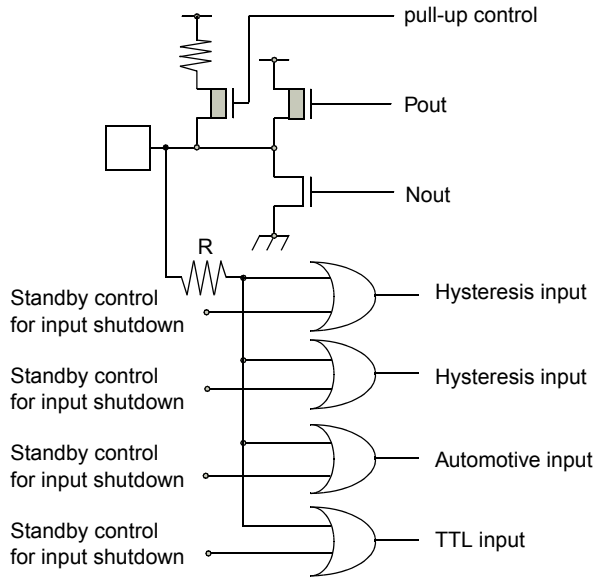
[3]: ALARM0, ALARM1 are not available on MB96F345Dyy or MB96F345Fyy

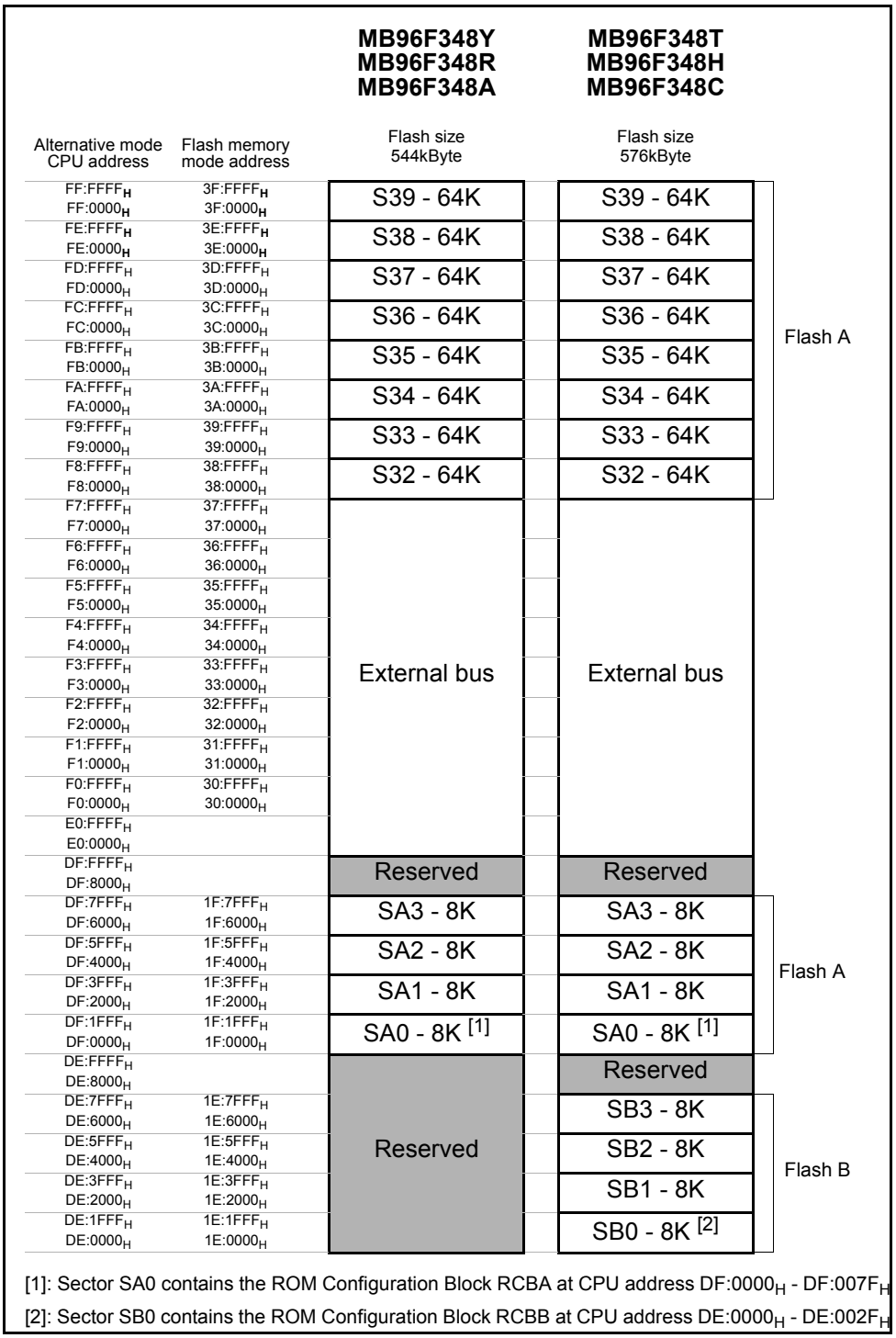
[4]: AVRH2 is not available on MB96F345Dyy or MB96F345Fyy

(FPT-100P-M20)

**Remark:**

MB96(F)34x products are pin-compatible to F$^2$MC-16LX family MB90340 series.

| Type | Circuit | Remarks |
|---|---|---|
| I |  | ■ CMOS level output (programmable $I_{OL}$ = 5mA, $I_{OH}$ = -5mA and $I_{OL}$ = 2mA, $I_{OH}$ = -2mA)<br>■ 2 different CMOS hysteresis inputs with input shutdown function *<br>■ Automotive input with input shutdown function<br>■ TTL input with input shutdown function *<br>■ Programmable pull-up resistor: 50kΩ approx.<br>■ Analog input<br>*MB96F345Dyy or MB96F345Fyy: Only Automotive input and CMOS hysteresis input (0.7/0.3) are supported |
| N |  | ■ CMOS level output ($I_{OL}$ = 3mA, $I_{OH}$ = -3mA)<br>■ 2 different CMOS hysteresis inputs with input shutdown function *<br>■ Automotive input with input shutdown function<br>■ TTL input with input shutdown function *<br>■ Programmable pull-up resistor: 50kΩ approx.<br>*MB96F345Dyy or MB96F345Fyy: Only Automotive input and CMOS hysteresis input (0.7/0.3) are supported |




[1]: Sector SA0 contains the ROM Configuration Block RCBA at CPU address DF:0000$_H$ - DF:007F$_H$

[2]: Sector SB0 contains the ROM Configuration Block RCBB at CPU address DE:0000$_H$ - DE:002F$_H$

**Table 4: I/O map MB96(F)34x**

| Address | Register | Abbreviation 8-bit access | Abbreviation 16-bit access | Access |
|---|---|---|---|---|
| $00004B_H$ | ICU3 - Capture Register High | IPCPH3 | | R |
| $00004C_H$ | ICU4/ICU5 - Control Status Register | ICS45 | | R/W |
| $00004D_H$ | ICU4/ICU5 - Edge register | ICE45 | | R/W |
| $00004E_H$ | ICU4 - Capture Register Low | IPCPL4 | IPCP4 | R |
| $00004F_H$ | ICU4 - Capture Register High | IPCPH4 | | R |
| $000050_H$ | ICU5 - Capture Register Low | IPCPL5 | IPCP5 | R |
| $000051_H$ | ICU5 - Capture Register High | IPCPH5 | | R |
| $000052_H$ | ICU6/ICU7 - Control Status Register | ICS67 | | R/W |
| $000053_H$ | ICU6/ICU7 - Edge register | ICE67 | | R/W |
| $000054_H$ | ICU6 - Capture Register Low | IPCPL6 | IPCP6 | R |
| $000055_H$ | ICU6 - Capture Register High | IPCPH6 | | R |
| $000056_H$ | ICU7 - Capture Register Low | IPCPL7 | IPCP7 | R |
| $000057_H$ | ICU7 - Capture Register High | IPCPH7 | | R |
| $000058_H$ | EXTINT0 - External Interrupt Enable Register | ENIR0 | | R/W |
| $000059_H$ | EXTINT0 - External Interrupt Interrupt request Register | EIRR0 | | R/W |
| $00005A_H$ | EXTINT0 - External Interrupt Level Select Low | ELVRL0 | ELVR0 | R/W |
| $00005B_H$ | EXTINT0 - External Interrupt Level Select High | ELVRH0 | | R/W |
| $00005C_H$ | EXTINT1 - External Interrupt Enable Register | ENIR1 | | R/W |
| $00005D_H$ | EXTINT1 - External Interrupt Interrupt request Register | EIRR1 | | R/W |
| $00005E_H$ | EXTINT1 - External Interrupt Level Select Low | ELVRL1 | ELVR1 | R/W |
| $00005F_H$ | EXTINT1 - External Interrupt Level Select High | ELVRH1 | | R/W |
| $000060_H$ | RLT0 - Timer Control Status Register Low | TMCSRL0 | TMCSR0 | R/W |
| $000061_H$ | RLT0 - Timer Control Status Register High | TMCSRH0 | | R/W |
| $000062_H$ | RLT0 - Reload Register - for writing | | TMRLR0 | W |
| $000062_H$ | RLT0 - Reload Register - for reading | | TMR0 | R |
| $000063_H$ | RLT0 - Reload Register - for writing | | | W |
| $000063_H$ | RLT0 - Reload Register - for reading | | | R |
| $000064_H$ | RLT1 - Timer Control Status Register Low | TMCSRL1 | TMCSR1 | R/W |
| $000065_H$ | RLT1 - Timer Control Status Register High | TMCSRH1 | | R/W |
| $000066_H$ | RLT1 - Reload Register - for writing | | TMRLR1 | W |
| $000066_H$ | RLT1 - Reload Register - for reading | | TMR1 | R |
| $000067_H$ | RLT1 - Reload Register - for writing | | | W |

**Table 4: I/O map MB96(F)34x**

| Address | Register | Abbreviation 8-bit access | Abbreviation 16-bit access | Access |
|---|---|---|---|---|
| $000081_H$ | PPG1 - Timer register | | | R |
| $000082_H$ | PPG1 - Period setting register | | PCSR1 | W |
| $000083_H$ | PPG1 - Period setting register | | | W |
| $000084_H$ | PPG1 - Duty cycle register | | PDUT1 | W |
| $000085_H$ | PPG1 - Duty cycle register | | | W |
| $000086_H$ | PPG1 - Control status register Low | PCNL1 | PCN1 | R/W |
| $000087_H$ | PPG1 - Control status register High | PCNH1 | | R/W |
| $000088_H$ | PPG2 - Timer register | | PTMR2 | R |
| $000089_H$ | PPG2 - Timer register | | | R |
| $00008A_H$ | PPG2 - Period setting register | | PCSR2 | W |
| $00008B_H$ | PPG2 - Period setting register | | | W |
| $00008C_H$ | PPG2 - Duty cycle register | | PDUT2 | W |
| $00008D_H$ | PPG2 - Duty cycle register | | | W |
| $00008E_H$ | PPG2 - Control status register Low | PCNL2 | PCN2 | R/W |
| $00008F_H$ | PPG2 - Control status register High | PCNH2 | | R/W |
| $000090_H$ | PPG3 - Timer register | | PTMR3 | R |
| $000091_H$ | PPG3 - Timer register | | | R |
| $000092_H$ | PPG3 - Period setting register | | PCSR3 | W |
| $000093_H$ | PPG3 - Period setting register | | | W |
| $000094_H$ | PPG3 - Duty cycle register | | PDUT3 | W |
| $000095_H$ | PPG3 - Duty cycle register | | | W |
| $000096_H$ | PPG3 - Control status register Low | PCNL3 | PCN3 | R/W |
| $000097_H$ | PPG3 - Control status register High | PCNH3 | | R/W |
| $000098_H$ | PPG7-PPG4 - General Control register 1 Low | GCN1L1 | GCN11 | R/W |
| $000099_H$ | PPG7-PPG4 - General Control register 1 High | GCN1H1 | | R/W |
| $00009A_H$ | PPG7-PPG4 - General Control register 2 Low | GCN2L1 | GCN21 | R/W |
| $00009B_H$ | PPG7-PPG4 - General Control register 2 High | GCN2H1 | | R/W |
| $00009C_H$ | PPG4 - Timer register | | PTMR4 | R |
| $00009D_H$ | PPG4 - Timer register | | | R |
| $00009E_H$ | PPG4 - Period setting register | | PCSR4 | W |
| $00009F_H$ | PPG4 - Period setting register | | | W |
| $0000A0_H$ | PPG4 - Duty cycle register | | PDUT4 | W |

**Table 5: Interrupt vector table MB96(F)34x**

| Vector number | Offset in vector table | Vector name | Cleared by DMA | Index in ICR to program | Description |
|---|---|---|---|---|---|
| 90 | $294_H$ | LINT7 | Yes | 90 | LIN USART 7 TX |
| 91 | $290_H$ | LINR8 | Yes | 91 | LIN USART 8 RX |
| 92 | $28C_H$ | LINT8 | Yes | 92 | LIN USART 8 TX |
| 93 | $288_H$ | LINR9 | Yes | 93 | LIN USART 9 RX |
| 94 | $284_H$ | LINT9 | Yes | 94 | LIN USART 9 TX |
| 95 | $280_H$ | RTC0 | No | 95 | Real Timer Clock |
| 96 | $27C_H$ | CAL0 | No | 96 | Clock Calibration Unit |
| 97 | $278_H$ | DFLASH_A | Yes | 97 | Data Flash A<br>(only MB96F345Dyy, MB96F345Fyy) |

# 13. Handling Devices

**Special care is required for the following when handling the device:**

- Latch-up prevention
- Unused pins handling
- External clock usage
- Unused sub clock signal
- Notes on PLL clock mode operation
- Power supply pins ($V_{CC}$/$V_{SS}$)
- Crystal oscillator circuit
- Turn on sequence of power supply to A/D converter and analog inputs
- Pin handling when not using the A/D converter
- Notes on energization
- Stabilization of power supply voltage
- Serial communication
- Handling of Data Flash

## 13.1 Latch-up prevention

CMOS IC chips may suffer latch-up under the following conditions:

- A voltage higher than $V_{CC}$ or lower than $V_{SS}$ is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between $V_{CC}$ pins and $V_{SS}$ pins.
- The $AV_{CC}$ power supply is applied before the $V_{CC}$ voltage.

Latch-up may increase the power supply current dramatically, causing thermal damages to the device.

For the same reason, extra care is required to not let the analog power-supply voltage ($AV_{CC}$, AVRH) exceed the digital power-supply voltage.

## 13.2 Unused pins handling

Unused input pins can be left open when the input is disabled (corresponding bit of Port Input Enable register PIER = 0).

Leaving unused input pins open when the input is enabled may result in misbehavior and possible permanent damage of the device. They must therefore be pulled up or pulled down through resistors. To prevent latch-up, those resistors should be more than 2 kΩ.

Unused bidirectional pins can be set either to the output state and be then left open, or to the input state with either input disabled or external pull-up/pull-down resistor as described above.

## 13.3 External clock usage

The permitted frequency range of an external clock depends on the oscillator type and configuration. See AC Characteristics for detailed modes and frequency limits. Single and opposite phase external clocks must be connected as follows:

| Parameter | Symbol | Rating | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Permitted Power dissipation (Mask ROM devices) [4] | $P_D$ | - | 350 | mW | $T_A$=105°C |
| | | - | 360 | mW | $T_A$=125°C [6] |
| Operating ambient temperature | $T_A$ | 0 | +70 | °C | MB96V300B |
| | | -40 | +105 | | |
| | | -40 | +125 | | [6] |
| Storage temperature | $T_{STG}$ | -55 | +150 | °C | |

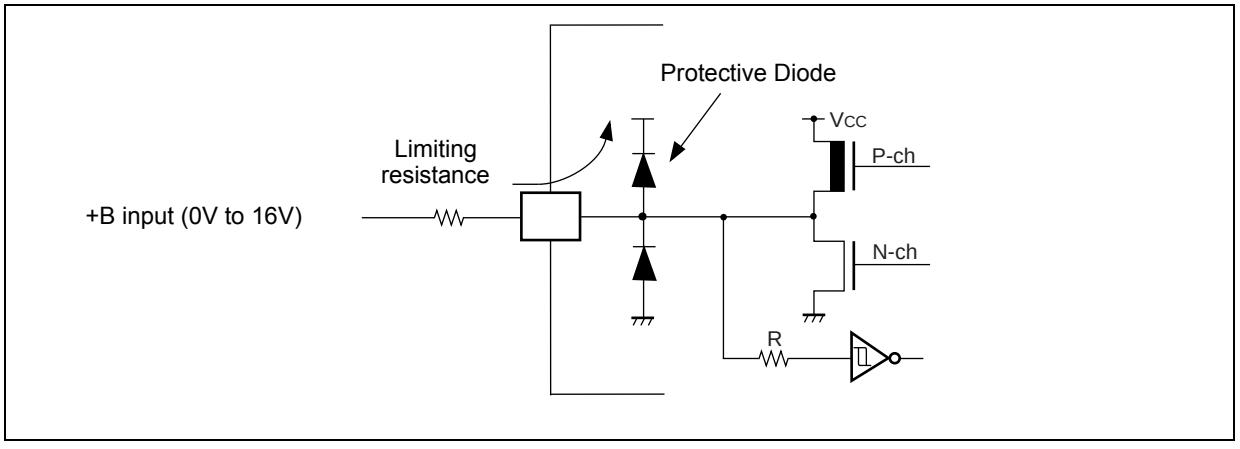
[1]: $AV_{CC}$ and $V_{CC}$ must be set to the same voltage. It is required that $AV_{CC}$ does not exceed $V_{CC}$ and that the voltage at the analog inputs does not exceed $AV_{CC}$ neither when the power is switched on.

[2]: $V_I$ and $V_O$ should not exceed $V_{CC}$ + 0.3 V. $V_I$ should also not exceed the specified ratings. However if the maximum current to/from a input is limited by some means with external components, the $I_{CLAMP}$ rating supersedes the $V_I$ rating. Input/output voltages of standard ports depend on $V_{CC}$.

[3]:

- Applicable to all general purpose I/O pins (Pnn_m)
- Use within recommended operating conditions.
- Use at DC voltage (current)
- The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the $V_{CC}$ pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the Power reset (except devices with persistent low voltage reset in internal vector mode).

**Sample recommended circuits**:



[4]: The maximum permitted power dissipation depends on the ambient temperature, the air flow velocity and the thermal conductance of the package on the PCB.The actual power dissipation depends on the customer application and can be calculated as follows:
$P_D = P_{IO} + P_{INT}$
$P_{IO} = \Sigma (V_{OL} * I_{OL} + V_{OH} * I_{OH})$ (IO load power dissipation, sum is performed on all IO ports)
$P_{INT} = V_{CC} * (I_{CC} + I_A)$ (internal power dissipation)
$I_{CC}$ is the total core current consumption into $V_{CC}$ as described in the “DC characteristics” and depends on the selected operation mode and clock frequency and the usage of functions like Flash programming or the clock modulator.$I_A$ is the analog current consumption into $AV_{CC}$.

[5]: Worst case value for a package mounted on single layer PCB at specified $T_A$ without air flow.

[6]: Please contact Cypress for reliability limitations when using under these conditions.

**WARNING:** Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed any of these ratings.

## 14.2 Recommended Operating Conditions

| Parameter | Symbol | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Power supply voltage | $V_{CC}$ | 3.0 | - | 5.5 | V | |
| Smoothing capacitor at C pin | $C_S$ | 3.5 | 4.7 - 10 | 15 | µF | Use a low inductance capacitor (for example X7R ceramic capacitor) |

**WARNING:** The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

## 14.3 DC characteristics

($T_A$ = -40°C to 125°C, $V_{CC}$ = $AV_{CC}$ = 3.0V to 5.5V, $V_{SS}$ = $AV_{SS}$ = 0V)

| Parameter | Symbol | Pin | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Input H voltage | $V_{IH}$ | Port inputs Pnn_m | CMOS Hysteresis 0.8/0.2 input selected | 0.8 $V_{CC}$ | - | $V_{CC}$ + 0.3 | V | |
| | | | CMOS Hysteresis 0.7/0.3 input selected | 0.7 $V_{CC}$ | - | $V_{CC}$ + 0.3 | V | $V_{CC} \geq 4.5V$ |
| | | | | 0.74 $V_{CC}$ | - | $V_{CC}$ + 0.3 | V | $V_{CC} < 4.5V$ |
| | | | AUTOMOTIVE Hysteresis input selected | 0.8 $V_{CC}$ | - | $V_{CC}$ + 0.3 | V | |
| | | | TTL input selected | 2.0 | - | $V_{CC}$ + 0.3 | V | |
| | $V_{IHX0F}$ | X0 | External clock in “Fast Clock Input mode” | 0.8 $V_{CC}$ | - | $V_{CC}$ + 0.3 | V | Not available in MB96F34xY/R/AxA |
| | $V_{IHX0S}$ | X0,X1, X0A,X1A | External clock in “oscillation mode” | 2.5 | - | $V_{CC}$ + 0.3 | V | |
| | $V_{IHR}$ | RSTX | - | 0.8 $V_{CC}$ | - | $V_{CC}$ + 0.3 | V | CMOS Hysteresis input |
| | $V_{IHM}$ | MD2-MD0 | - | $V_{CC}$ - 0.3 | - | $V_{CC}$ + 0.3 | V | |
| Input L voltage | $V_{IL}$ | Port inputs Pnn_m | CMOS Hysteresis 0.8/0.2 input selected | $V_{SS}$ - 0.3 | - | 0.2 $V_{CC}$ | V | |
| | | | CMOS Hysteresis 0.7/0.3 input selected | $V_{SS}$ - 0.3 | - | 0.3 $V_{CC}$ | V | |
| | | | AUTOMOTIVE Hysteresis input selected | $V_{SS}$ - 0.3 | - | 0.5 $V_{CC}$ | V | $V_{CC} \geq 4.5V$ |
| | | | | $V_{SS}$ - 0.3 | - | 0.46 $V_{CC}$ | | $V_{CC} < 4.5V$ |
| | | | TTL input selected | $V_{SS}$ - 0.3 | - | 0.8 | V | |
| | $V_{ILX0F}$ | X0 | External clock in “Fast Clock Input mode” | $V_{SS}$ - 0.3 | - | 0.2 $V_{CC}$ | V | Not available in MB96F34xY/R/AxA |
| | $V_{ILX0S}$ | X0,X1, X0A,X1A | External clock in “oscillation mode” | $V_{SS}$ - 0.3 | - | 0.4 | V | |
| | $V_{ILR}$ | RSTX | - | $V_{SS}$ - 0.3 | - | 0.2 $V_{CC}$ | V | CMOS Hysteresis input |
| | $V_{ILM}$ | MD2-MD0 | - | $V_{SS}$ - 0.3 | - | $V_{SS}$ + 0.3 | V | |
| Output H voltage | $V_{OH2}$ | Normal outputs | $4.5V \leq V_{CC} \leq 5.5V$, $I_{OH}$ = -2mA / $3.0V \leq V_{CC} < 4.5V$, $I_{OH}$ = -1.6mA | $V_{CC}$ - 0.5 | - | - | V | Driving strength set to 2mA |
| | $V_{OH5}$ | Normal outputs | $4.5V \leq V_{CC} \leq 5.5V$, $I_{OH}$ = -5mA / $3.0V \leq V_{CC} < 4.5V$, $I_{OH}$ = -3mA | $V_{CC}$ - 0.5 | - | - | V | Driving strength set to 5mA |
| | $V_{OH3}$ | 3mA outputs | $4.5V \leq V_{CC} \leq 5.5V$, $I_{OH}$ = -3mA / $3.0V \leq V_{CC} < 4.5V$, $I_{OH}$ = -2mA | $V_{CC}$ - 0.5 | - | - | V | |

### 14.4.8 Bus Timing (Read)

($T_A$ = –40°C to +125°C, $V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = 0.0 V, $IO_{drive}$ = 5mA, $C_L$ = 50pF)

| Parameter | Symbol | Pin | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| ALE pulse width | $t_{LHLL}$ | ALE | EACL:STS=0 and EACL:ACE=0 | $t_{CYC}/2 - 5$ | - | ns | |
| | | | EACL:STS=1 | $t_{CYC} - 5$ | - | | |
| | | | EACL:STS=0 and EACL:ACE=1 | $3t_{CYC}/2 - 5$ | - | | |
| Valid address ⇒ ALE ↓ time | $t_{AVLL}$ | ALE, A[23:16], | EACL:STS=0 and EACL:ACE=0 | $t_{CYC} - 15$ | - | ns | |
| | | | EACL:STS=1 and EACL:ACE=0 | $3t_{CYC}/2 - 15$ | - | | |
| | | | EACL:STS=0 and EACL:ACE=1 | $2t_{CYC} - 15$ | - | | |
| | | | EACL:STS=1 and EACL:ACE=1 | $5t_{CYC}/2 - 15$ | - | | |
| | $t_{ADVLL}$ | ALE,AD[15:0] | EACL:STS=0 and EACL:ACE=0 | $t_{CYC}/2 - 15$ | - | ns | |
| | | | EACL:STS=1 and EACL:ACE=0 | $t_{CYC} - 15$ | - | | |
| | | | EACL:STS=0 and EACL:ACE=1 | $3t_{CYC}/2 - 15$ | - | | |
| | | | EACL:STS=1 and EACL:ACE=1 | $2t_{CYC} - 15$ | - | | |
| ALE ↓ ⇒ Address valid time | $t_{LLAX}$ | ALE, AD[15:0] | EACL:STS=0 | $t_{CYC}/2 - 15$ | - | ns | |
| | | | EACL:STS=1 | -15 | - | | |
| Valid address ⇒ RDX ↓ time | $t_{AVRL}$ | RDX, A[23:16] | EACL:ACE=0 | $3t_{CYC}/2 - 15$ | - | ns | |
| | | | EACL:ACE=1 | $5t_{CYC}/2 - 15$ | - | | |
| | $t_{ADVRL}$ | RDX, AD[15:0] | EACL:ACE=0 | $t_{CYC} - 15$ | - | ns | |
| | | | EACL:ACE=1 | $2t_{CYC} - 15$ | - | | |
| Valid address ⇒ Valid data input | $t_{AVDV}$ | A[23:16], AD[15:0] | EACL:ACE=0 | - | $3t_{CYC} - 55$ | ns | w/o cycle extension |
| | | | EACL:ACE=1 | - | $4t_{CYC} - 55$ | | |
| | $t_{ADVDV}$ | AD[15:0] | EACL:ACE=0 | - | $5t_{CYC}/2 - 55$ | ns | w/o cycle extension |
| | | | EACL:ACE=1 | - | $7t_{CYC}/2 - 55$ | | |
| RDX pulse width | $t_{RLRH}$ | RDX | - | $3\ t_{CYC}/2 - 5$ | - | ns | w/o cycle extension |
| RDX ↓ ⇒ Valid data input | $t_{RLDV}$ | RDX, AD[15:0] | - | - | $3\ t_{CYC}/2 - 50$ | ns | w/o cycle extension |
| RDX ↑ ⇒ Data hold time | $t_{RHDX}$ | RDX, AD[15:0] | - | 0 | - | ns | |
| Address valid ⇒ Data hold time | $t_{AXDX}$ | A[23:16], AD[15:0] | - | 0 | - | ns | |

### 14.4.9 Bus Timing (Write)

($T_A$ = –40°C to +125°C, $V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = 0.0 V, $IO_{drive}$ = 5mA, $C_L$ = 50pF)

| Parameter | Symbol | Pin | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Valid address ⇒ WRX ↓ time | $t_{AVWL}$ | WRX, WRLX, WRHX, A[23:16] | EACL:ACE=0 | $3t_{CYC}/2 - 15$ | - | ns | |
| | | | EACL:ACE=1 | $5t_{CYC}/2 - 15$ | - | | |
| | $t_{ADVWL}$ | WRX, WRLX, WRHX, AD[15:0] | EACL:ACE=0 | $t_{CYC} - 15$ | - | ns | |
| | | | EACL:ACE=1 | $2t_{CYC} - 15$ | - | | |
| WRX pulse width | $t_{WLWH}$ | WRX, WRXL, WRHX | - | $t_{CYC} - 5$ | - | ns | w/o cycle extension |
| Valid data output ⇒ WRX ↑ time | $t_{DVWH}$ | WRX, WRLX, WRHX, AD[15:0] | - | $t_{CYC} - 20$ | - | ns | w/o cycle extension |
| WRX ↑ ⇒ Data hold time | $t_{WHDX}$ | WRX, WRLX, WRHX, AD[15:0] | - | $t_{CYC}/2 - 15$ | - | ns | |
| WRX ↑ ⇒ Address valid time | $t_{WHAX}$ | WRX, WRLX, WRHX, A[23:16] | - | $t_{CYC}/2 - 15$ | - | ns | |
| WRX ↑ ⇒ ALE ↑ time | $t_{WHLH}$ | WRX, WRLX, WRHX, ALE | EBM:ACE=1 and EACL:STS=1 | $2t_{CYC} - 10$ | - | ns | |
| | | | other EBM:ACE and EACL:STS setting | $t_{CYC} - 10$ | - | | |
| WRX ↓ ⇒ ECLK ↑ time | $t_{WLCH}$ | WRX, WRLX, WRHX, ECLK | - | $t_{CYC}/2 - 10$ | - | ns | |
| CSn ⇒ WRX time | $t_{CSLWL}$ | WRX, WRLX, WRHX, CSn | EACL:ACE=0 | - | $3t_{CYC}/2 - 15$ | ns | |
| | | | EACL:ACE=1 | - | $5t_{CYC}/2 - 15$ | | |
| WRX ⇒ CSn time | $t_{WHCSH}$ | WRX, WRLX, WRHX, CSn | - | $t_{CYC}/2 - 15$ | - | ns | |

($T_A$ = –40°C to +125°C, $V_{CC}$ = 3.0 to 4.5V, $V_{SS}$ = 0.0 V, $IO_{drive}$ = 5mA, $C_L$ = 50pF)

| Parameter | Symbol | Pin | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Valid address ⇒ WRX ↓ time | $t_{AVWL}$ | WRX, WRLX, WRHX, A[23:16] | EACL:ACE=0 | $3t_{CYC}/2 - 20$ | - | ns | |
| | | | EACL:ACE=1 | $5t_{CYC}/2 - 20$ | - | | |
| | $t_{ADVWL}$ | WRX, WRLX, WRHX, AD[15:0] | EACL:ACE=0 | $t_{CYC} - 20$ | - | ns | |
| | | | EACL:ACE=1 | $2t_{CYC} - 20$ | - | | |

($T_A$ = −40°C to +125°C, $V_{CC}$ = 3.0 to 4.5V, $V_{SS}$ = 0.0 V, $IO_{drive}$ = 5mA, $C_L$ = 50pF)

| Parameter | Symbol | Pin | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| WRX pulse width | $t_{WLWH}$ | WRX, WRXL, WRHX | - | $t_{CYC}$ − 8 | - | ns | w/o cycle extension |
| Valid data output ⇒ WRX ↑ time | $t_{DVWH}$ | WRX, WRLX, WRHX, AD[15:0] | - | $t_{CYC}$ − 25 | - | ns | w/o cycle extension |
| WRX ↑ ⇒ Data hold time | $t_{WHDX}$ | WRX, WRLX, WRHX, AD[15:0] | - | $t_{CYC}/2$ − 20 | - | ns | |
| WRX ↑ ⇒ Address valid time | $t_{WHAX}$ | WRX, WRLX, WRHX, A[23:16] | - | $t_{CYC}/2$ − 20 | - | ns | |
| WRX ↑ ⇒ ALE ↑ time | $t_{WHLH}$ | WRX, WRLX, WRHX, ALE | EBM:ACE=1 and EACL:STS=1 | $2t_{CYC}$ − 15 | - | ns | |
| | | | other EBM:ACE and EACL:STS setting | $t_{CYC}$ − 15 | - | | |
| WRX ↓ ⇒ ECLK ↑ time | $t_{WLCH}$ | WRX, WRLX, WRHX, ECLK | - | $t_{CYC}/2$ − 15 | - | ns | |
| CSn ⇒ WRX time | $t_{CSLWL}$ | WRX, WRLX, WRHX, CSn | EACL:ACE=0 | - | $3t_{CYC}/2$ − 20 | ns | |
| | | | EACL:ACE=1 | - | $5t_{CYC}/2$ − 20 | | |
| WRX ⇒ CSn time | $t_{WHCSH}$ | WRX, WRLX, WRHX, CSn | - | $t_{CYC}/2$ − 20 | - | ns | |

### 14.4.12 USART timing

**WARNING**: The values given below are for an I/O driving strength $IO_{drive}$ = 5mA. If $IO_{drive}$ is 2mA, all the maximum output timing described in the different tables must then be increased by 10ns.

($T_A$ = -40°C to 125°C, $V_{CC}$ = 3.0V to 5.5V, $V_{SS}$ = $AV_{SS}$ = 0V, $IO_{drive}$ = 5mA, $C_L$ = 50pF)

| Parameter | Symbol | Pin | Condition | $V_{CC}$ = $AV_{CC}$= 4.5V to 5.5V | | $V_{CC}$ = $AV_{CC}$= 3.0V to 4.5V | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| Serial clock cycle time | $t_{SCYCI}$ | SCKn | Internal Shift Clock Mode | 4 $t_{CLKP1}$ | - | 4 $t_{CLKP1}$ | - | ns |
| SCK ↓→ SOT delay time | $t_{SLOVI}$ | SCKn, SOTn | | -20 | +20 | -30 | +30 | ns |
| SOT → SCK ↑ delay time | $t_{OVSHI}$ | SCKn, SOTn | | N*$t_{CLKP1}$ - 20 [1] | - | N*$t_{CLKP1}$ - 30 [1] | - | ns |
| Valid SIN → SCK ↑ | $t_{IVSHI}$ | SCKn, SINn | | $t_{CLKP1}$ + 45 | - | $t_{CLKP1}$ + 55 | - | ns |
| SCK ↑→ Valid SIN hold time | $t_{SHIXI}$ | SCKn, SINn | | 0 | - | 0 | - | ns |
| Serial clock “L” pulse width | $t_{SLSHE}$ | SCKn | External Shift Clock Mode | $t_{CLKP1}$ + 10 | - | $t_{CLKP1}$ + 10 | - | ns |
| Serial clock “H” pulse width | $t_{SHSLE}$ | SCKn | | $t_{CLKP1}$ + 10 | - | $t_{CLKP1}$ + 10 | - | ns |
| SCK ↓→ SOT delay time | $t_{SLOVE}$ | SCKn, SOTn | | - | 2 $t_{CLKP1}$ + 45 | - | 2 $t_{CLKP1}$ + 55 | ns |
| Valid SIN → SCK ↑ | $t_{IVSHE}$ | SCKn, SINn | | $t_{CLKP1}$/2 + 10 | - | $t_{CLKP1}$/2 + 10 | - | ns |
| SCK ↑→ Valid SIN hold time | $t_{SHIXE}$ | SCKn, SINn | | $t_{CLKP1}$ + 10 | - | $t_{CLKP1}$ + 10 | - | ns |
| SCK fall time | $t_{FE}$ | SCKn | | - | 20 | - | 20 | ns |
| SCK rise time | $t_{RE}$ | SCKn | | - | 20 | - | 20 | ns |

**Notes**:

- AC characteristic in CLK synchronized mode.
- $C_L$ is the load capacity value of pins when testing.
- Depending on the used machine clock frequency, the maximum possible baud rate can be limited by some parameters. These parameters are shown in “MB96300 Super series HARDWARE MANUAL”.
- $t_{CLKP1}$ is the cycle time of the peripheral clock 1 (CLKP1), Unit : ns

[1]: Parameter N depends on $t_{SCYCI}$ and can be calculated as follows:

- if $t_{SCYCI}$ = 2*k*$t_{CLKP1}$, then N = k, where k is an integer > 2
- if $t_{SCYCI}$ = (2*k+1)*$t_{CLKP1}$, then N = k+1, where k is an integer > 1

Examples:

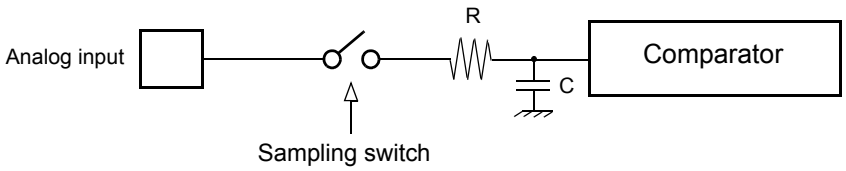
| $t_{SCYCI}$ | N |
|---|---|
| 4*$t_{CLKP1}$ | 2 |
| 5*$t_{CLKP1}$, | 3 |
| 7*$t_{CLKP1}$, | 4 |
| ... | ... |

### 14.5.2 Notes on A/D Converter Section

■ About the external impedance of the analog input and the sampling time of the A/D converter (with sample and hold circuit):

If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision.

Analog input circuit model:




**Reference value:**
C = 8.5 pF (Max)

To satisfy the A/D conversion precision standard, the relationship between the external impedance and minimum sampling time must be considered and then either the resistor value and operating frequency must be adjusted or the external impedance must be decreased so that the sampling time ($T_{samp}$) is longer than the minimum value. Usually, this value is set to 7$\tau$, where $\tau$ = RC. If the external input resistance ($R_{ext}$) connected to the analog input is included, the sampling time is expressed as follows:

$T_{samp}$ [min] = 7 × ($R_{ext}$ + 2.6kΩ) × C for 4.5 ≤ $AV_{cc}$ ≤ 5.5

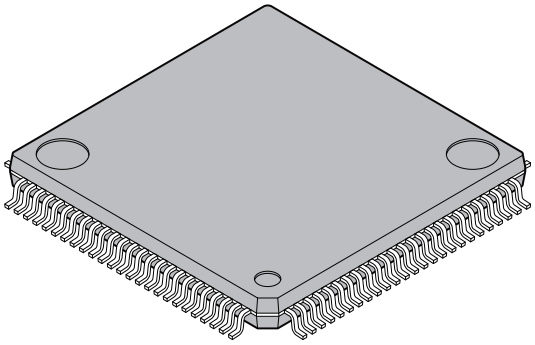
$T_{samp}$ [min] = 7 × ($R_{ext}$ + 12.1kΩ) × C for 3.0 ≤ $AV_{cc}$ ≤ 4.5

If the sampling time cannot be sufficient, connect a capacitor of about 0.1 μF to the analog input pin.

■ About the error

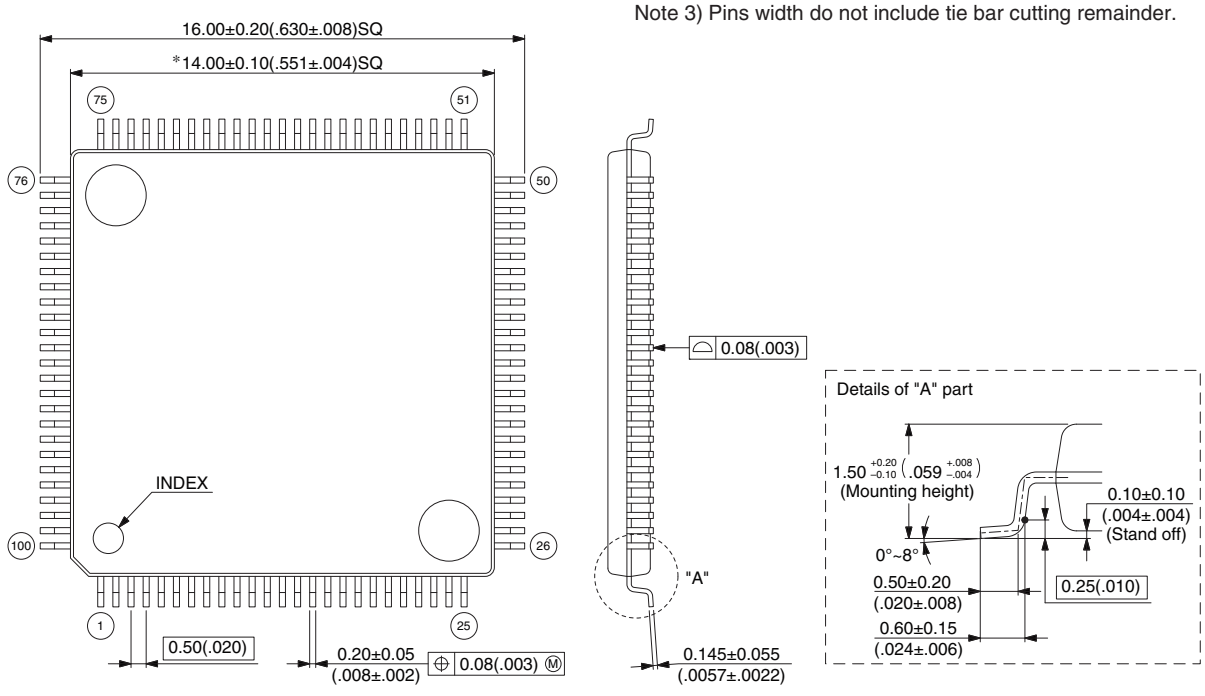
The accuracy gets worse as |AVRH - AVRL| becomes smaller.

# 16. Package Dimension MB96(F)34x LQFP 100P

| 100-pin plastic LQFP | | |
|---|---|---|
|  | Lead pitch | 0.50 mm |
| | Package width × package length | 14.0 mm × 14.0 mm |
| | Lead shape | Gullwing |
| | Sealing method | Plastic mold |
| | Mounting height | 1.70 mm Max |
| | Weight | 0.65 g |
| (FPT-100P-M20) | Code (Reference) | P-LFQFP100-14×14-0.50 |

100-pin plastic LQFP
(FPT-100P-M20)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.






Dimensions in mm (inches).
Note: The values in parentheses are reference values