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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

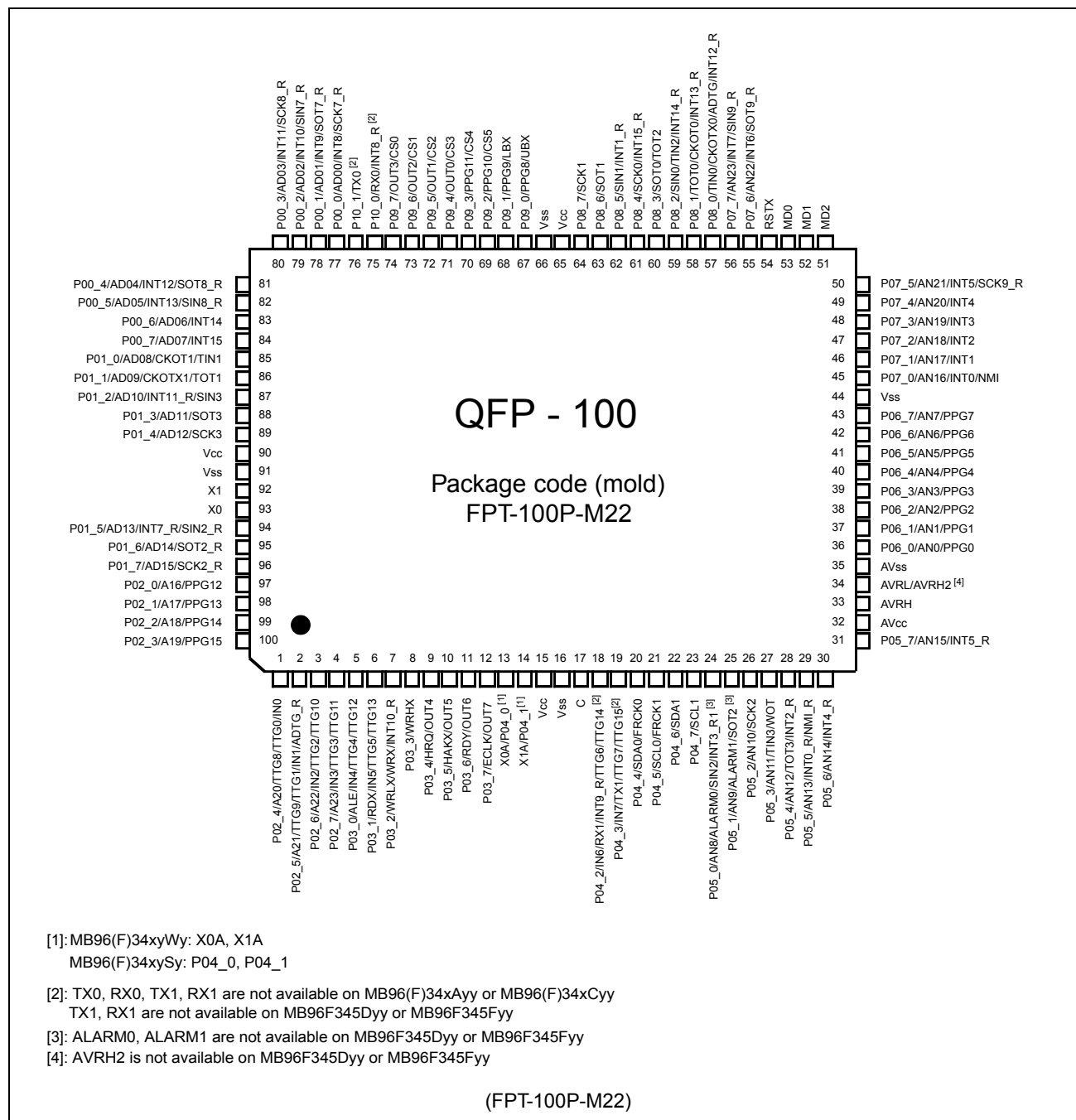
Details

Product Status	Obsolete
Core Processor	F ² MC-16FX
Core Size	16-Bit
Speed	56MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, LVR, POR, PWM, WDT
Number of I/O	82
Program Memory Size	416KB (416K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-PQFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f347asbpqc-gse2

Feature	Description
Alarm comparator	■ Monitors an external voltage and generates an interrupt in case of a voltage lower or higher than the defined thresholds ■ Threshold voltages defined externally or generated internally ■ Status is readable, interrupts can be masked separately
I/O Ports	■ Virtually all external pins can be used as general purpose I/O ■ All push-pull outputs (except when used as I2C SDA/SCL line) ■ Bit-wise programmable as input/output or peripheral signal ■ Bit-wise programmable input enable ■ Bit-wise programmable input levels: Automotive / CMOS-Schmitt trigger / TTL (TTL levels not supported by all devices) ■ Bit-wise programmable pull-up resistor ■ Bit-wise programmable output driving strength for EMI optimization
Packages	■ 100-pin plastic QFP and LQFP
Flash Memory	■ Supports automatic programming, Embedded Algorithm ■ Write/Erase/Erase-Suspend/Resume commands ■ A flag indicating completion of the algorithm ■ Number of erase cycles: 10,000 times ■ Data retention time: 20 years ■ Erase can be performed on each sector individually ■ Sector protection ■ Flash Security feature to protect the content of the Flash ■ Low voltage detection during Flash erase

3. Pin Assignments

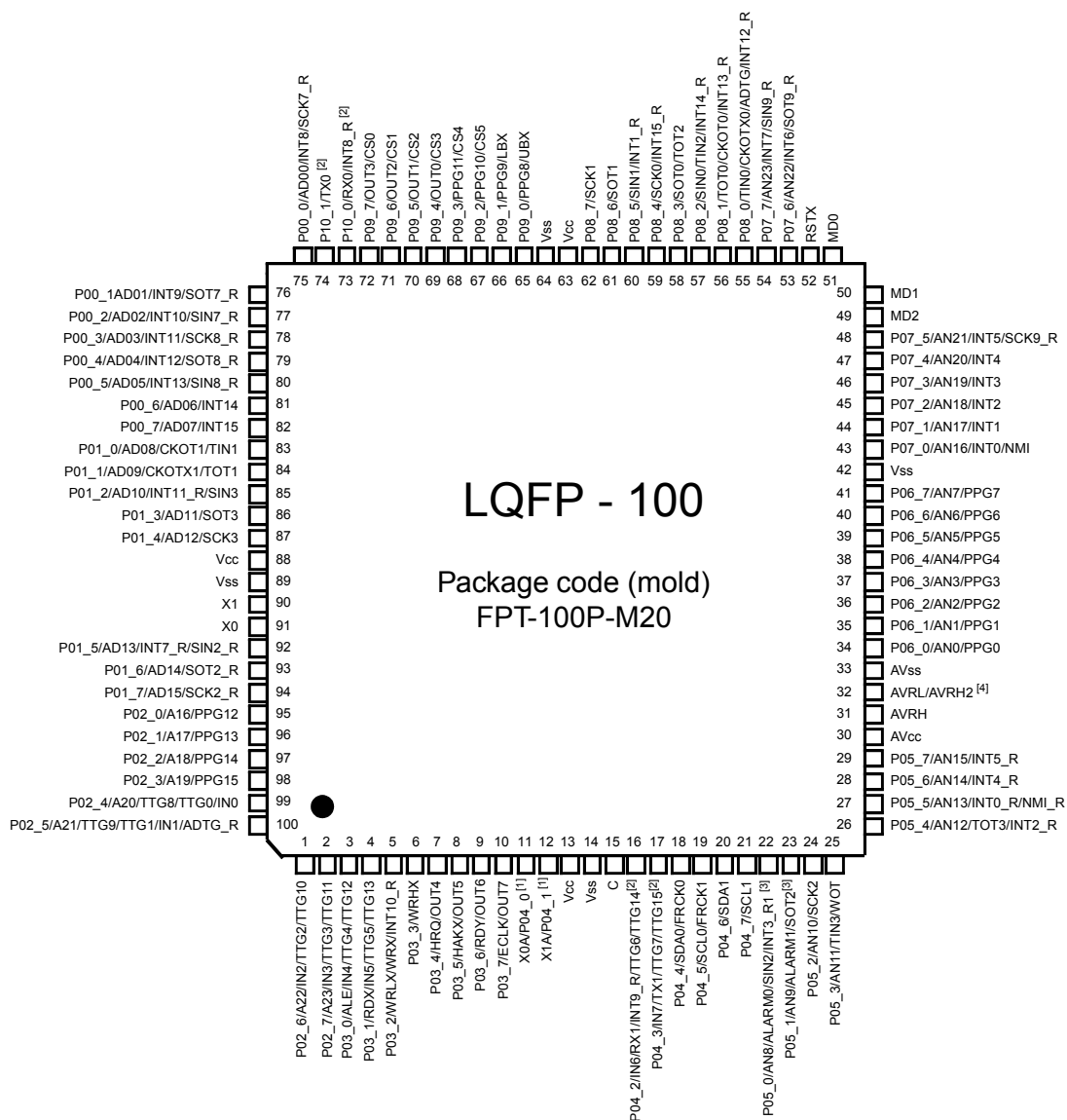
Figure 2. Pin assignment of MB96(F)34x (FPT-100P-M22)



Remark:

MB96(F)34x products are pin-compatible to F²MC-16LX family MB90340 series.

Figure 3. Pin assignment of MB96(F)34x (FPT-100P-M20)



5. Pin Circuit Type

Table 2: Pin circuit types

FPT-100P-M20		FPT-100P-M22	
Pin no.	Circuit type ^[1]	Pin no.	Circuit type ^[1]
1-10	H	1-12	H
11,12	B ^[2]	13, 14	B ^[2]
11,12	H ^[3]	13, 14	H ^[3]
13,14	Supply	15,16	Supply
15	F	17	F
16,17	H	18,19	H
18-21	N	20-23	N
22-29	I	24-31	I
30	Supply	32	Supply
31-32	G	33-34	G
33	Supply	35	Supply
34 to 41	I	36 to 43	I
42	Supply	44	Supply
43 to 48	I	45 to 50	I
49 to 51	C	51 to 53	C
52	E	54	E
53 to 54	I	55 to 56	I
55 to 62	H	57 to 64	H
63, 64	Supply	65, 66	Supply
65 to 87	H	67 to 89	H
88,89	Supply	90, 91	Supply
90, 91	A	92, 93	A
92-100	H	94 to 100	H

[1]: Please refer to “[I/O Circuit Type](#)” for details on the I/O circuit types

[2]: Devices with suffix “W”

[3]: Devices without suffix “W”

7. Memory Map

MB96V300B			MB96(F)34x		
FF:FFFF _H	Emulation ROM		USER ROM / External Bus^[4]		
DE:0000 _H					
	External Bus		External Bus		
10:0000 _H					
0F:E000 _H	Boot-ROM		Boot-ROM		
	Reserved	0F:0000 _H	Reserved		
0E:0000 _H			DATA FLASH / Reserved^[4]		
	External RAM	0C:0000 _H	Reserved		
02:0000 _H			Reserved		
	Internal RAM bank 1	RAMEND1 ^[2] RAMSTART1 ^[2]	Internal RAM bank 1		RAM availability depending on the device
01:0000 _H			Reserved		
	ROM/RAM MIRROR		ROM/RAM MIRROR		
00:8000 _H					
	Internal RAM bank 0	RAMSTART0 ^[2]	Internal RAM bank 0		
			Reserved		
RAMSTART0 ^[3]			External Bus		External Bus end address ^[2]
00:0C00 _H	External Bus				
	Peripherals		Peripherals		
00:0380 _H					
00:0180 _H	GPR^[1]		GPR^[1]		
00:0100 _H	DMA		DMA		
00:00F0 _H	External Bus		External Bus		
00:0000 _H	Peripheral		Peripheral		

[1]: Unused GPR banks can be used as RAM area

[2]: For External Bus end address and RAMSTART/END addresses, please refer to the table on the next page.

[3]: For EVA device, RAMSTART0 depends on the configuration of the emulated device.

[4]: For details about USER ROM area or DATA FLASH area, see the [User ROM Memory Map For Flash Devices](#) and [User ROM Memory Map for Mask ROM Devices](#) on the following pages.

The External Bus area and DMA area are only available if the device contains the corresponding resource.

The available RAM and ROM area depends on the device.

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000067 _H	RLT1 - Reload Register - for reading			R
000068 _H	RLT2 - Timer Control Status Register Low	TMCSRL2	TMCSR2	R/W
000069 _H	RLT2 - Timer Control Status Register High	TMCSRH2		R/W
00006A _H	RLT2 - Reload Register - for writing		TMRLR2	W
00006A _H	RLT2 - Reload Register - for reading		TMR2	R
00006B _H	RLT2 - Reload Register - for writing			W
00006B _H	RLT2 - Reload Register - for reading			R
00006C _H	RLT3 - Timer Control Status Register Low	TMCSRL3	TMCSR3	R/W
00006D _H	RLT3 - Timer Control Status Register High	TMCSRH3		R/W
00006E _H	RLT3 - Reload Register - for writing		TMRLR3	W
00006E _H	RLT3 - Reload Register - for reading		TMR3	R
00006F _H	RLT3 - Reload Register - for writing			W
00006F _H	RLT3 - Reload Register - for reading			R
000070 _H	RLT6 - Timer Control Status Register Low (dedic. RLT for PPG)	TMCSRL6	TMCSR6	R/W
000071 _H	RLT6 - Timer Control Status Register High (dedic. RLT for PPG)	TMCSRH6		R/W
000072 _H	RLT6 - Reload Register (dedic. RLT for PPG) - for writing		TMRLR6	W
000072 _H	RLT6 - Reload Register (dedic. RLT for PPG) - for reading		TMR6	R
000073 _H	RLT6 - Reload Register (dedic. RLT for PPG) - for writing			W
000073 _H	RLT6 - Reload Register (dedic. RLT for PPG) - for reading			R
000074 _H	PPG3-PPG0 - General Control register 1 Low	GCN1L0	GCN10	R/W
000075 _H	PPG3-PPG0 - General Control register 1 High	GCN1H0		R/W
000076 _H	PPG3-PPG0 - General Control register 2 Low	GCN2L0	GCN20	R/W
000077 _H	PPG3-PPG0 - General Control register 2 High	GCN2H0		R/W
000078 _H	PPG0 - Timer register		PTMR0	R
000079 _H	PPG0 - Timer register			R
00007A _H	PPG0 - Period setting register		PCSR0	W
00007B _H	PPG0 - Period setting register			W
00007C _H	PPG0 - Duty cycle register		PDUT0	W
00007D _H	PPG0 - Duty cycle register			W
00007E _H	PPG0 - Control status register Low	PCNL0	PCN0	R/W
00007F _H	PPG0 - Control status register High	PCNH0		R/W
000080 _H	PPG1 - Timer register		PTMR1	R

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0003D9 _H	Memory Patch function - Patch data 4 High	PFDH4		R/W
0003DA _H	Memory Patch function - Patch data 5 Low	PFDL5	PFD5	R/W
0003DB _H	Memory Patch function - Patch data 5 High	PFDH5		R/W
0003DC _H	Memory Patch function - Patch data 6 Low	PFDL6	PFD6	R/W
0003DD _H	Memory Patch function - Patch data 6 High	PFDH6		R/W
0003DE _H	Memory Patch function - Patch data 7 Low	PFDL7	PFD7	R/W
0003DF _H	Memory Patch function - Patch data 7 High	PFDH7		R/W
0003E0 _H	Data Flash Control and Status register A	DFCSA		R/W
0003E1 _H	Data Flash Write command sequencer Control register A	DFWCA		R/W
0003E2 _H	Data Flash Write command sequencer Status register A	DFWSA		R/W
0003E3 _H -0003F0 _H	Reserved			-
0003F1 _H	Memory Control Status Register A	MCSRA		R/W
0003F2 _H	Memory Timing Configuration Register A Low	MTCRAL	MTCRA	R/W
0003F3 _H	Memory Timing Configuration Register A High	MTCRAH		R/W
0003F4 _H	Reserved			-
0003F5 _H	Memory Control Status Register B	MCSR B		R/W
0003F6 _H	Memory Timing Configuration Register B Low	MTCRBL	MTCRB	R/W
0003F7 _H	Memory Timing Configuration Register B High	MTCRBH		R/W
0003F8 _H	Flash Memory Write Control register 0	FMWC0		R/W
0003F9 _H	Flash Memory Write Control register 1	FMWC1		R/W
0003FA _H	Flash Memory Write Control register 2	FMWC2		R/W
0003FB _H	Flash Memory Write Control register 3	FMWC3		R/W
0003FC _H	Flash Memory Write Control register 4	FMWC4		R/W
0003FD _H	Flash Memory Write Control register 5	FMWC5		R/W
0003FE _H -0003FF _H	Reserved			-
000400 _H	Standby Mode control register	SMCR		R/W
000401 _H	Clock select register	CKSR		R/W
000402 _H	Clock Stabilization select register	CKSSR		R/W
000403 _H	Clock monitor register	CKMR		R
000404 _H	Clock Frequency control register Low	CKFCRL	CKFCR	R/W
000405 _H	Clock Frequency control register High	CKFCRH		R/W
000406 _H	PLL Control register Low	PLLCRL	PLLCR	R/W

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0006EB _H	External Bus - Area configuration register 5 High	EACH5		R/W
0006EC _H	External Bus - Area select register 2	EAS2		R/W
0006ED _H	External Bus - Area select register 3	EAS3		R/W
0006EE _H	External Bus - Area select register 4	EAS4		R/W
0006EF _H	External Bus - Area select register 5	EAS5		R/W
0006F0 _H	External Bus - Mode register	EBM		R/W
0006F1 _H	External Bus - Clock and Function register	EBCF		R/W
0006F2 _H	External Bus - Address output enable register 0	EBAE0		R/W
0006F3 _H	External Bus - Address output enable register 1	EBAE1		R/W
0006F4 _H	External Bus - Address output enable register 2	EBAE2		R/W
0006F5 _H	External Bus - Control signal register	EBCS		R/W
0006F6 _H -0006FF _H	Reserved			-
000700 _H	CAN0 - Control register Low	CTRLRL0	CTRLR0	R/W
000701 _H	CAN0 - Control register High (reserved)	CTRLRH0		R
000702 _H	CAN0 - Status register Low	STATRL0	STATR0	R/W
000703 _H	CAN0 - Status register High (reserved)	STATRH0		R
000704 _H	CAN0 - Error Counter Low (Transmit)	ERRCNTL0	ERRCNT0	R
000705 _H	CAN0 - Error Counter High (Receive)	ERRCNTH0		R
000706 _H	CAN0 - Bit Timing Register Low	BTRL0	BTR0	R/W
000707 _H	CAN0 - Bit Timing Register High	BTRH0		R/W
000708 _H	CAN0 - Interrupt Register Low	INTRL0	INTR0	R
000709 _H	CAN0 - Interrupt Register High	INTRH0		R
00070A _H	CAN0 - Test Register Low	TESTRL0	TESTR0	R/W
00070B _H	CAN0 - Test Register High (reserved)	TESTRH0		R
00070C _H	CAN0 - BRP Extension register Low	BRPERL0	BRPER0	R/W
00070D _H	CAN0 - BRP Extension register High (reserved)	BRPERH0		R
00070E _H -00070F _H	Reserved			-
000710 _H	CAN0 - IF1 Command request register Low	IF1CREQL0	IF1CREQ0	R/W
000711 _H	CAN0 - IF1 Command request register High	IF1CREQH0		R/W
000712 _H	CAN0 - IF1 Command Mask register Low	IF1CMSKL0	IF1CMSK0	R/W
000713 _H	CAN0 - IF1 Command Mask register High (reserved)	IF1CMSKH0		R
000714 _H	CAN0 - IF1 Mask 1 Register Low	IF1MSK1L0	IF1MSK10	R/W

12. Interrupt Vector Table

Table 5: Interrupt vector table MB96(F)34x

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
0	3FC _H	CALLV0	No	-	
1	3F8 _H	CALLV1	No	-	
2	3F4 _H	CALLV2	No	-	
3	3F0 _H	CALLV3	No	-	
4	3EC _H	CALLV4	No	-	
5	3E8 _H	CALLV5	No	-	
6	3E4 _H	CALLV6	No	-	
7	3E0 _H	CALLV7	No	-	
8	3DC _H	RESET	No	-	
9	3D8 _H	INT9	No	-	
10	3D4 _H	EXCEPTION	No	-	
11	3D0 _H	NMI	No	-	Non-Maskable Interrupt
12	3CC _H	DLY	No	12	Delayed Interrupt
13	3C8 _H	RC_TIMER	No	13	RC Timer
14	3C4 _H	MC_TIMER	No	14	Main Clock Timer
15	3C0 _H	SC_TIMER	No	15	Sub Clock Timer
16	3BC _H	RESERVED	No	16	Reserved
17	3B8 _H	EXTINT0	Yes	17	External Interrupt 0
18	3B4 _H	EXTINT1	Yes	18	External Interrupt 1
19	3B0 _H	EXTINT2	Yes	19	External Interrupt 2
20	3AC _H	EXTINT3	Yes	20	External Interrupt 3
21	3A8 _H	EXTINT4	Yes	21	External Interrupt 4
22	3A4 _H	EXTINT5	Yes	22	External Interrupt 5
23	3A0 _H	EXTINT6	Yes	23	External Interrupt 6
24	39C _H	EXTINT7	Yes	24	External Interrupt 7
25	398 _H	EXTINT8	Yes	25	External Interrupt 8
26	394 _H	EXTINT9	Yes	26	External Interrupt 9
27	390 _H	EXTINT10	Yes	27	External Interrupt 10
28	38C _H	EXTINT11	Yes	28	External Interrupt 11
29	388 _H	EXTINT12	Yes	29	External Interrupt 12

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Permitted Power dissipation (Mask ROM devices) ^[4]	P_D	-	350	mW	$T_A=105^{\circ}\text{C}$
		-	360	mW	$T_A=125^{\circ}\text{C}$ [6]
Operating ambient temperature	T_A	0	+70	$^{\circ}\text{C}$	MB96V300B
		-40	+105		
		-40	+125		[6]
Storage temperature	T_{STG}	-55	+150	$^{\circ}\text{C}$	

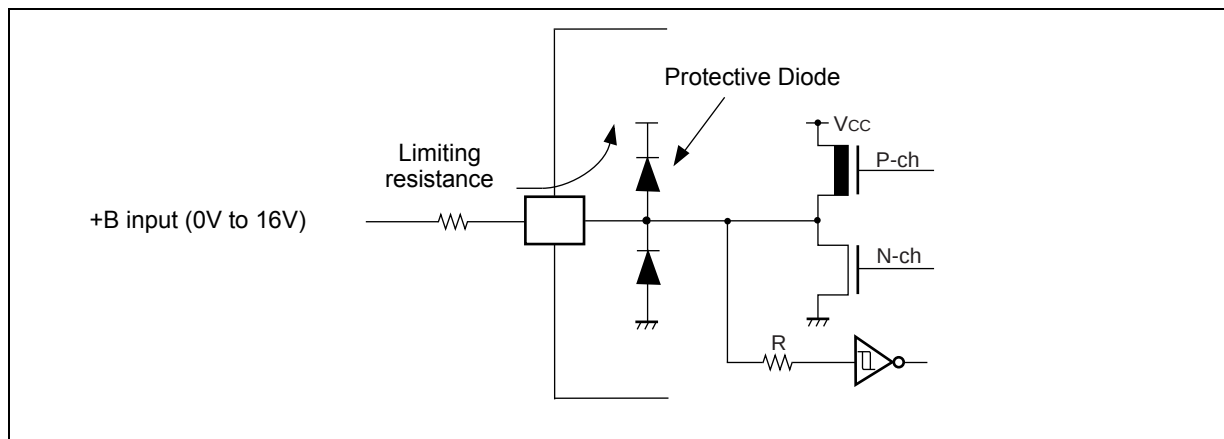
[1]: AV_{CC} and V_{CC} must be set to the same voltage. It is required that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} neither when the power is switched on.

[2]: V_I and V_O should not exceed $V_{CC} + 0.3\text{ V}$. V_I should also not exceed the specified ratings. However if the maximum current to/from a input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating. Input/output voltages of standard ports depend on V_{CC} .

[3]:

- Applicable to all general purpose I/O pins (Pnn_m)
- Use within recommended operating conditions.
- Use at DC voltage (current)
- The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the Power reset (except devices with persistent low voltage reset in internal vector mode).

Sample recommended circuits:



($T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = 0\text{V}$)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Run modes ^[1]	I_{CCRCH}	RC Run mode with $CLKS1/2 = CLKB = CLKP1/2 = 2\text{MHz}$ (CLKMC, CLKPLL and CLKSC stopped)	+25°C	2.9	4	mA	Flash devices at 1 Flash wait state
			+125°C	3.5	6.5		
			+25°C	1.7	2.7	mA	MB96345/346 at 1 ROM wait state
			+125°C	2.3	4.7		
	I_{CCRCL}	RC Run mode with $CLKS1/2 = CLKB = CLKP1/2 = 100\text{kHz}$, SMCR:LPMS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)	+25°C	0.4	0.6	mA	MB96F346/F347/F348 at 1 Flash wait state
			+125°C	0.9	3.5		
			+25°C	0.18	0.3	mA	MB96F345 at 1 Flash wait state
			+125°C	0.68	3.3		
		RC Run mode with $CLKS1/2 = CLKB = CLKP1/2 = 100\text{kHz}$, SMCR:LPMS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode, no Flash programming/erasing allowed)	+25°C	0.4	0.6	mA	MB96345/346 at 1 ROM wait state
			+125°C	0.9	2.4		
			+25°C	0.15	0.25	mA	Flash devices at 1 Flash wait state
			+125°C	0.65	3.2		
			+25°C	0.15	0.25	mA	MB96345/346 at 1 ROM wait state
			+125°C	0.65	2.1		
	I_{CCSUB}	Sub Run mode with $CLKS1/2 = CLKB = CLKP1/2 = 32\text{kHz}$ (CLKMC, CLKPLL and CLKRC stopped, no Flash programming/erasing allowed)	+25°C	0.1	0.2	mA	Flash devices at 1 Flash wait state
			+125°C	0.6	3		
			+25°C	0.1	0.2	mA	MB96345/346 at 1 ROM wait state
			+125°C	0.6	2		

14.4.2 Internal Clock timing

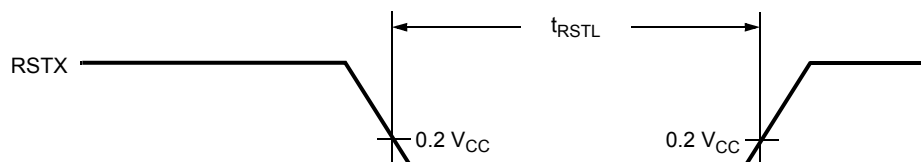
($T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = 0\text{V}$)

Parameter	Symbol	Core Voltage Settings				Unit	Remarks
		1.8V		1.9V			
		Min	Max	Min	Max		
Internal System clock frequency (CLKS1 and CLKS2)	f _{CLKS1} , f _{CLKS2}	0	92	0	96	MHz	Others than below
		0	86	0	96	MHz	MB96F348T/H/CxB/C
		0	72	0	80	MHz	MB96F345
		0	68	0	74	MHz	MB96F34xY/R/Axx
Internal CPU clock frequency (CLKB), internal peripheral clock frequency (CLKP1)	f _{CLKB} , f _{CLKP1}	0	52	0	56	MHz	Others than below
		0	36	0	40	MHz	MB96F345
Internal peripheral clock frequency (CLKP2)	f _{CLKP2}	0	28	0	32	MHz	Others than below
		0	26	0	28	MHz	MB96F34xY/R/Axx

14.4.3 External Reset timing

($T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = 0\text{V}$)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Reset input time	t_{RSTL}	RSTX	500	-	-	ns	

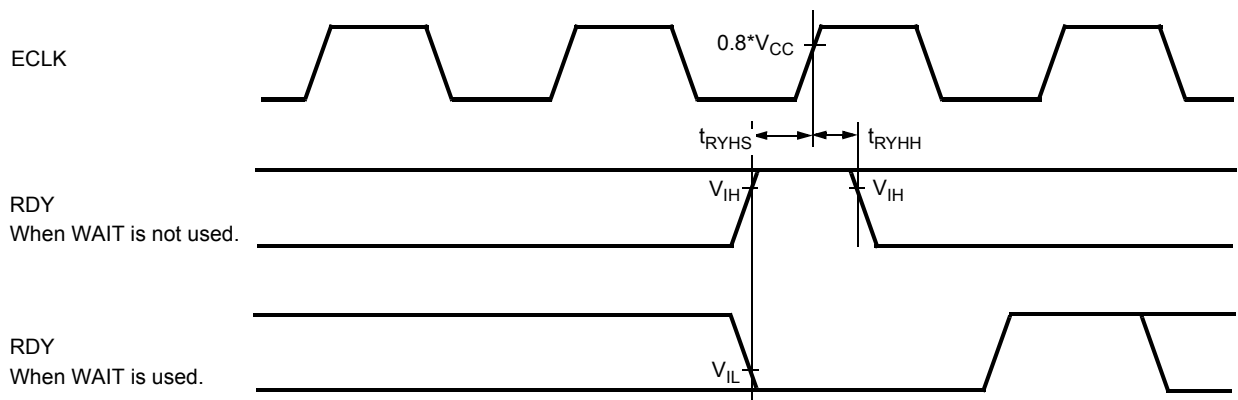


($T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 3.0$ to 4.5V , $V_{SS} = 0.0\text{V}$, $I_{Odrive} = 5\text{mA}$, $C_L = 50\text{pF}$)

Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
Valid address $\Rightarrow$ Valid data input	t_{AVDV}	A[23:16], AD[15:0]	EACL:ACE=0	-	$3t_{CYC} - 60$	ns	w/o cycle extension
			EACL:ACE=1	-	$4t_{CYC} - 60$		
	$t_{ADV DV}$	AD[15:0]	EACL:ACE=0	-	$5t_{CYC}/2 - 60$	ns	w/o cycle extension
			EACL:ACE=1	-	$7t_{CYC}/2 - 60$		
RDX pulse width	t_{RLRH}	RDX	-	$3t_{CYC}/2 - 8$	-	ns	w/o cycle extension
RDX $\downarrow \Rightarrow$ Valid data input	t_{RLDV}	RDX, AD[15:0]	-	-	$3t_{CYC}/2 - 55$	ns	w/o cycle extension
RDX $\uparrow \Rightarrow$ Data hold time	t_{RHDX}	RDX, AD[15:0]	-	0	-	ns	
Address valid $\Rightarrow$ Data hold time	t_{AXDX}	A[23:16]	-	0	-	ns	
RDX $\uparrow \Rightarrow$ ALE $\uparrow$ time	t_{RHLH}	RDX, ALE	EACL:STS=1 and EACL:ACE=1	$3t_{CYC}/2 - 15$	-	ns	
			other ECL:STS, EA-CL:ACE setting	$t_{CYC}/2 - 15$	-		
Valid address $\Rightarrow$ ECLK $\uparrow$ time	t_{AVCH}	A[23:16], ECLK	-	$t_{CYC} - 20$	-	ns	
	t_{ADVCH}	AD[15:0], ECLK		$t_{CYC}/2 - 20$	-		
RDX $\downarrow \Rightarrow$ ECLK $\uparrow$ time	t_{RLCH}	RDX, ECLK	-	$t_{CYC}/2 - 15$	-	ns	
ALE $\downarrow \Rightarrow$ RDX $\downarrow$ time	t_{LLRL}	ALE, RDX	EACL:STS=0	$t_{CYC}/2 - 15$	-	ns	
			EACL:STS=1	- 15	-		
ECLK $\uparrow \Rightarrow$ Valid data input	t_{CHDV}	AD[15:0], ECLK	-	-	$t_{CYC} - 55$	ns	

($T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 3.0$ to 4.5V , $V_{SS} = 0.0\text{V}$, $I_{Odrive} = 5\text{mA}$, $C_L = 50\text{pF}$)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
WRX pulse width	t_{WLWH}	WRX, WRXL, WRHX	-	$t_{CYC} - 8$	-	ns	w/o cycle extension
Valid data output $\Rightarrow$ WRX $\uparrow$ time	t_{DVWH}	WRX, WRLX, WRHX, AD[15:0]	-	$t_{CYC} - 25$	-	ns	w/o cycle extension
WRX $\uparrow \Rightarrow$ Data hold time	t_{WHDX}	WRX, WRLX, WRHX, AD[15:0]	-	$t_{CYC}/2 - 20$	-	ns	
WRX $\uparrow \Rightarrow$ Address valid time	t_{WHAX}	WRX, WRLX, WRHX, A[23:16]	-	$t_{CYC}/2 - 20$	-	ns	
WRX $\uparrow \Rightarrow$ ALE $\uparrow$ time	t_{WHLH}	WRX, WRLX, WRHX, ALE	EBM:ACE=1 and EACL:STS=1	$2t_{CYC} - 15$	-	ns	
			other EBM:ACE and EACL:STS setting	$t_{CYC} - 15$	-		
WRX $\downarrow \Rightarrow$ ECLK $\uparrow$ time	t_{WLCH}	WRX, WRLX, WRHX, ECLK	-	$t_{CYC}/2 - 15$	-	ns	
CSn $\Rightarrow$ WRX time	t_{CSLWL}	WRX, WRLX, WRHX, CSn	EACL:ACE=0	-	$3t_{CYC}/2 - 20$	ns	
			EACL:ACE=1	-	$5t_{CYC}/2 - 20$		
WRX $\Rightarrow$ CSn time	t_{WHCSH}	WRX, WRLX, WRHX, CSn	-	$t_{CYC}/2 - 20$	-	ns	



Refer to the Hardware Manual for detailed Timing Charts

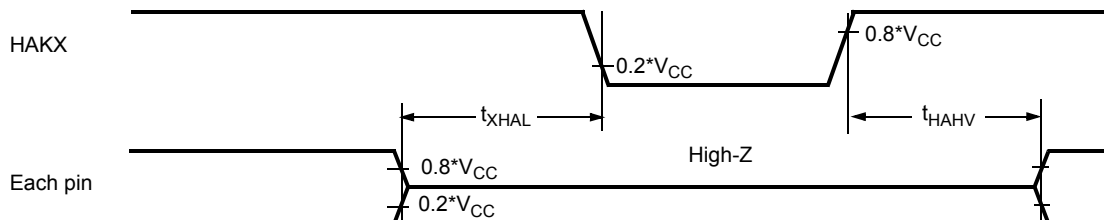
14.4.11 Hold Timing

(T_A = -40°C to +125°C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, I_{Odrive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min	Max		
Pin floating ⇒ HAKX ↓ time	t _{XHAL}	HAKX	-	t _{CYC} - 20	t _{CYC} + 20	ns	
HAKX ↑ time ⇒ Pin valid time	t _{HAHV}	HAKX		t _{CYC} - 20	t _{CYC} + 20	ns	

(T_A = -40°C to +125°C, V_{CC} = 3.0 to 4.5V, V_{SS} = 0.0 V, I_{Odrive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min	Max		
Pin floating ⇒ HAKX ↓ time	t _{XHAL}	HAKX	-	t _{CYC} - 25	t _{CYC} + 25	ns	
HAKX ↑ time ⇒ Pin valid time	t _{HAHV}	HAKX		t _{CYC} - 25	t _{CYC} + 25	ns	



Refer to the Hardware Manual for detailed Timing Charts

14.7 Low Voltage Detector Characteristics

($T_A = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$, $V_{CC} = AV_{CC} = 3.0\text{V} - 5.5\text{V}$, $V_{SS} = AV_{SS} = 0\text{V}$)

Parameter	Symbol	Value [1]		Value [2]		Unit	Remarks
		Min	Max	Min	Max		
Stabilization time	$T_{LVDSTAB}$	-	75	-	110	μs	After power-up or change of detection level
Level 0	V_{DL0}	2.7	2.9	2.65	2.95	V	CILCR:LVL[3:0]="0000"
Level 1	V_{DL1}	2.9	3.1	2.85	3.2	V	CILCR:LVL[3:0]="0001"
Level 2	V_{DL2}	3.1	3.3	3.05	3.4	V	CILCR:LVL[3:0]="0010"
Level 3	V_{DL3}	3.5	3.75	3.45	3.85	V	CILCR:LVL[3:0]="0011"
Level 4	V_{DL4}	3.6	3.85	3.55	3.95	V	CILCR:LVL[3:0]="0100"
Level 5	V_{DL5}	3.7	3.95	3.65	4.1	V	CILCR:LVL[3:0]="0101"
Level 6	V_{DL6}	3.8	4.05	3.75	4.2	V	CILCR:LVL[3:0]="0110"
Level 7	V_{DL7}	3.9	4.15	3.85	4.3	V	CILCR:LVL[3:0]="0111"
Level 8	V_{DL8}	4.0	4.25	3.95	4.4	V	CILCR:LVL[3:0]="1000"
Level 9	V_{DL9}	4.1	4.35	4.05	4.5	V	CILCR:LVL[3:0]="1001"
Level 10	V_{DL10}	not used		not used			
Level 11	V_{DL11}	not used		not used			
Level 12	V_{DL12}	not used		not used			
Level 13	V_{DL13}	not used		not used			
Level 14	V_{DL14}	not used		not used			
Level 15	V_{DL15}	not used		not used			

[1]: valid for all devices except devices listed under "[2]"

[2]: valid for: MB96F345

CILCR:LVL[3:0] are the low voltage detector level select bits of the CILCR register.

Levels 10 to 15 are not used in this device.

For correct detection, the slope of the voltage level must satisfy $\left| \frac{dV}{dt} \right| \leq 0.004 \frac{V}{\mu\text{s}}$.

Faster variations are regarded as noise and may not be detected.

The functional operation of the MCU is guaranteed down to the minimum low voltage detection level of $V_{CC} = 2.7\text{V}$. The electrical characteristics however are only valid in the specified range (usually down to 3.0V).

15. Example Characteristics

The diagrams below show the characteristics of one measured sample with typical process parameters.

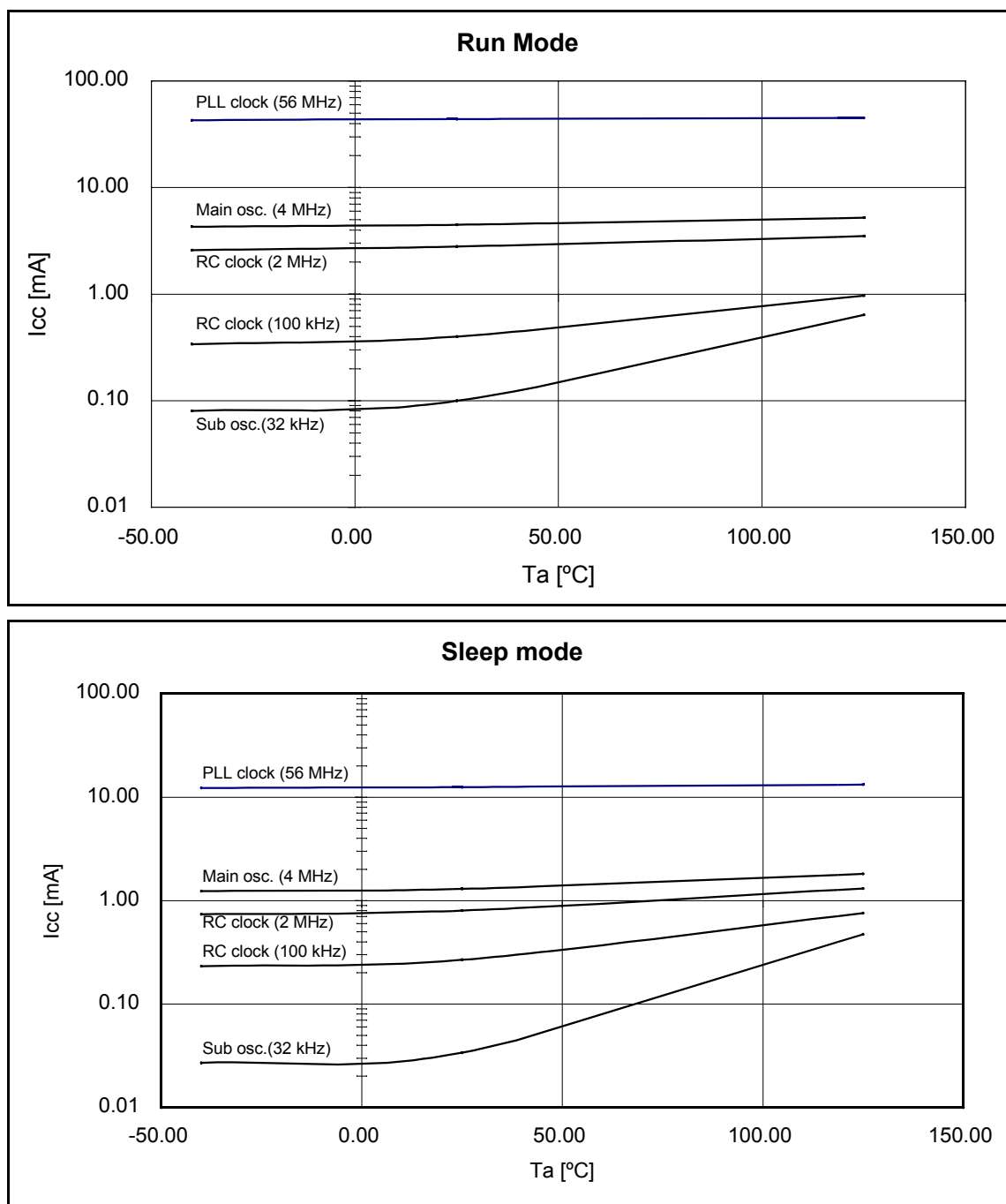


Table 6: Used settings

Mode	Selected Source Clock	Clock/Regulator Settings
Timer mode	PLL	CLKMC = 4 MHz, CLKPLL = 56 MHz (System clocks are stopped in this mode) Regulator in High Power Mode, Core Voltage = 1.9 V
	Main osc.	CLKMC = 4 MHz (System clocks are stopped in this mode) Regulator in High Power Mode, Core Voltage = 1.8 V
	RC clock fast	CLKRC = 2 MHz (System clocks are stopped in this mode) Regulator in High Power Mode, Core Voltage = 1.8 V
	RC clock slow	CLKRC = 100 kHz (System clocks are stopped in this mode) Regulator in High Power Mode, Core Voltage = 1.8 V
	Sub osc.	CLKSC = 100 kHz (System clocks are stopped in this mode) Regulator in Low Power Mode A, Core Voltage = 1.8 V
Stop mode	stopped	(All clocks are stopped in this mode) Regulator in Low Power Mode B, Core Voltage = 1.8 V

19. Revision History

Revision	Date	Modification
Prelim 1	2007-05-07	Creation
Prelim 2	2007-05-10	External bus hold timing update
Prelim 3	2007-05-23	Electrical characteristics updates
Prelim 4	2007-08-02	Electrical characteristics updates, Product lineup, changes and ordering information
Prelim 5	2007-09-12	Addition of the electrical characteristic examples and the LVD characteristics specifications, updates of the DC characteristics. Pin circuit type drawing modifications.
Prelim 6	2007-11-21	LVD typo correction. Update of the DC characteristics. Typos corrections.
Prelim 7	2007-12-04	Absolute maximum rating asterisks numbering corrected. Typos page 59: Hardware -> Hardware. IO map table regenerated. Typos corrections. IO circuit drawings modified. Renaming of the Main/Satellite Flash into Flash memory A/B. Memory map reworked.
Prelim 8	2008-02-04	■ Satellite Flash -> 32kB Data Flash ■ MB96345 added (under development) ■ MB96F348 TSA/HSA/TWA/HWA removed (outdated devices) ■ Block diagram and pin assignment corrected (existing resource pins) ■ Pin function table corrected ■ I/O circuit type diagrams corrected ■ Memory map cleaned up ■ "Flash sector configuration" replaced by corrected "User ROM Memory map for Flash devices", "ROM configuration" replaced by "User ROM Memory map for Mask ROM devices" ■ Parallel Flash programming pinning removed ■ IO map table regenerated: □ Port register: Naming style corrected □ Memory control registers renamed (Main/Sat -> A/B) □ addresses after 000BFFh removed ■ Absolute maximum ratings: Pd and Ta specified more precisely ■ oscillator input levels in oscillation mode with external clock added ■ Run and Sleep mode currents: 96/48MHz and 72/36MHz settings added ■ Run mode current spec in 48/24MHz mode corrected ■ Maximum CLKS1/2 frequency for all devices correctly specified ■ Maximum CLKP2 for MB96F34xY/R/Axx corrected ■ External bus timings: missing conditions added and readability improved ■ Alarm comparator spec updated (transition voltages defined) ■ MB96V300A removed ■ Ordering information updated ■ Typos and formatting corrected

Revision	Date	Modification
9	2009-01-09	■ Format adjusted to official Cypress datasheet standard (mainly style changes and official notes and disclaimer added) ■ Numbering of Electrical Characteristics subchapters automated ■ Note about devices under development modified ■ I/O map: Note added about reserved addresses ■ ICCSPLL for CLKS1=96MHz mode: increased by 1mA ■ Serial programming interface: Note about handshaking pins improved ■ specified AD converter channel offset to 4LSB ■ package code of MB96V300 corrected in ordering information ■ Added voltage condition to pull-up resistance spec ■ Lineup: Term "Data Flash" replaced by "independent 32KB Flash" ■ Ordering information: column "Independent 32KB Data Flash" replaced by new column "Flash/ROM", column "Remarks" removed ■ Official package dimension drawing with additional notes added ■ Empty pages removed ■ Alarm comparator: Power supply current max values increased, comparison time reduced, mode transition time and power-up stabilization time newly added ■ Handling devices: Notes added about Serial communication and about using ceramic resonators. ■ Feature list and AC Characteristics: 16MHz maximum frequency is valid for crystal oscillators. For resonators, maximum frequency depends on Q-factor ■ AC characteristics: PLL phase skew spec added, CLKVCO min=64MHz ■ VOL3 spec improved: spec valid for 3mA load for full Vcc range ■ MB96F345 added ■ Preliminary DC spec of MB96345/346 added ■ Permitted power dissipation of Flash devices in QFP package improved ■ C-Pin cap spec updated: 4.7uF-10uF capacitor with tolerance permitted ■ "Preliminary" watermark removed
10	To be released	■ I/O map: IOABK0-5 added at address 000A00H-000A05H ■ Ordering Information: Suffix "A" added to all MB96F345 device versions ■ AD converter I_{AIN} spec improved: 1uA valid up to 105deg, 1.2uA above 105deg