Infineon Technologies - MB96F347RSAPQC-GSE2 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

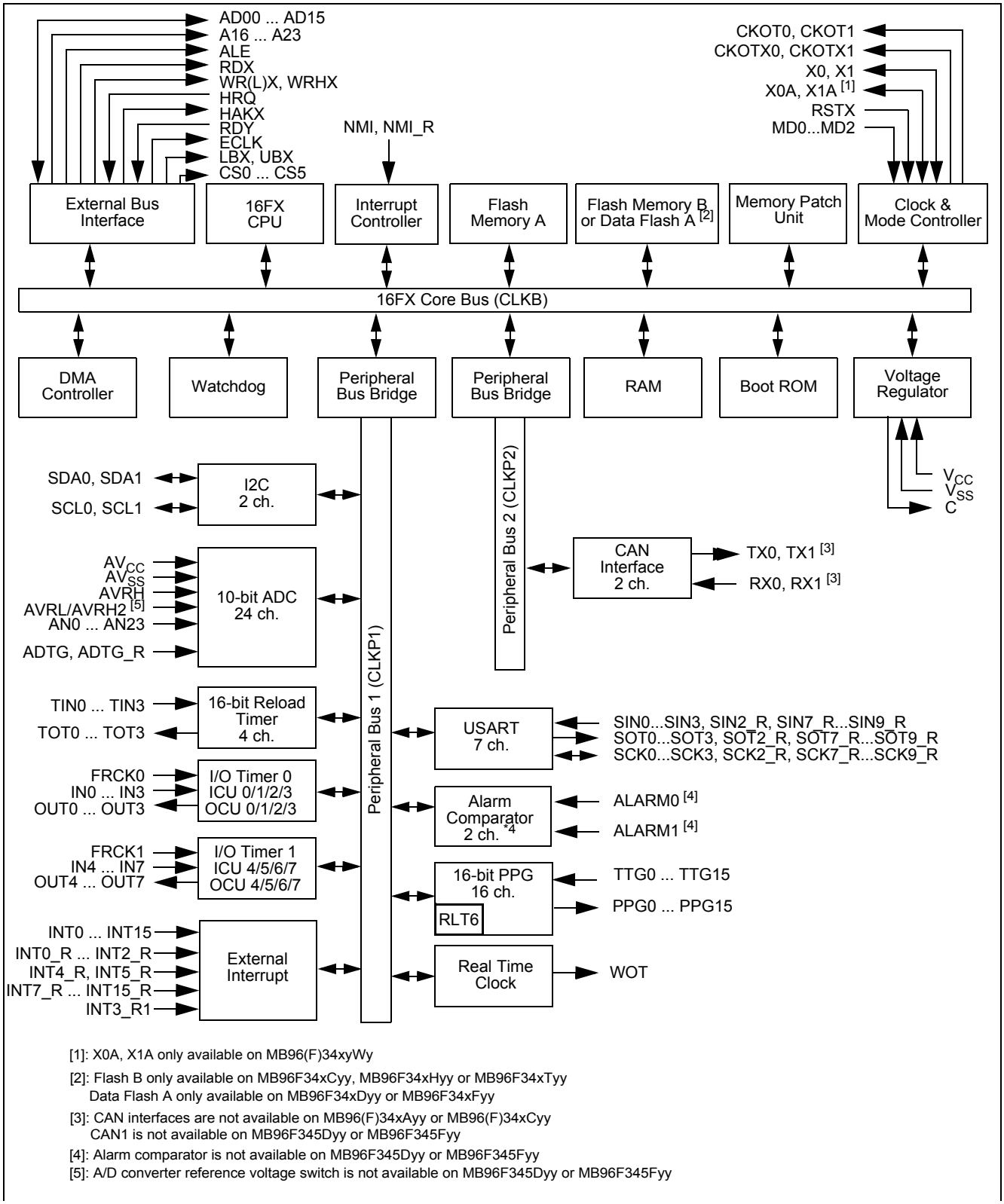
Details	
Product Status	Obsolete
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	56MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, LVR, POR, PWM, WDT
Number of I/O	82
Program Memory Size	416KB (416K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-PQFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f347rsapqc-gse2

Feature	Description
Alarm comparator	■ Monitors an external voltage and generates an interrupt in case of a voltage lower or higher than the defined thresholds ■ Threshold voltages defined externally or generated internally ■ Status is readable, interrupts can be masked separately
I/O Ports	■ Virtually all external pins can be used as general purpose I/O ■ All push-pull outputs (except when used as I2C SDA/SCL line) ■ Bit-wise programmable as input/output or peripheral signal ■ Bit-wise programmable input enable ■ Bit-wise programmable input levels: Automotive / CMOS-Schmitt trigger / TTL (TTL levels not supported by all devices) ■ Bit-wise programmable pull-up resistor ■ Bit-wise programmable output driving strength for EMI optimization
Packages	■ 100-pin plastic QFP and LQFP
Flash Memory	■ Supports automatic programming, Embedded Algorithm ■ Write/Erase/Erase-Suspend/Resume commands ■ A flag indicating completion of the algorithm ■ Number of erase cycles: 10,000 times ■ Data retention time: 20 years ■ Erase can be performed on each sector individually ■ Sector protection ■ Flash Security feature to protect the content of the Flash ■ Low voltage detection during Flash erase

Contents

2. Block Diagram

Figure 1. Block diagram of MB96(F)34x



[1]: X0A, X1A only available on MB96(F)34xyWy

[2]: Flash B only available on MB96F34xCyy, MB96F34xHyy or MB96F34xTyy
Data Flash A only available on MB96F34xDyy or MB96F34xFyy

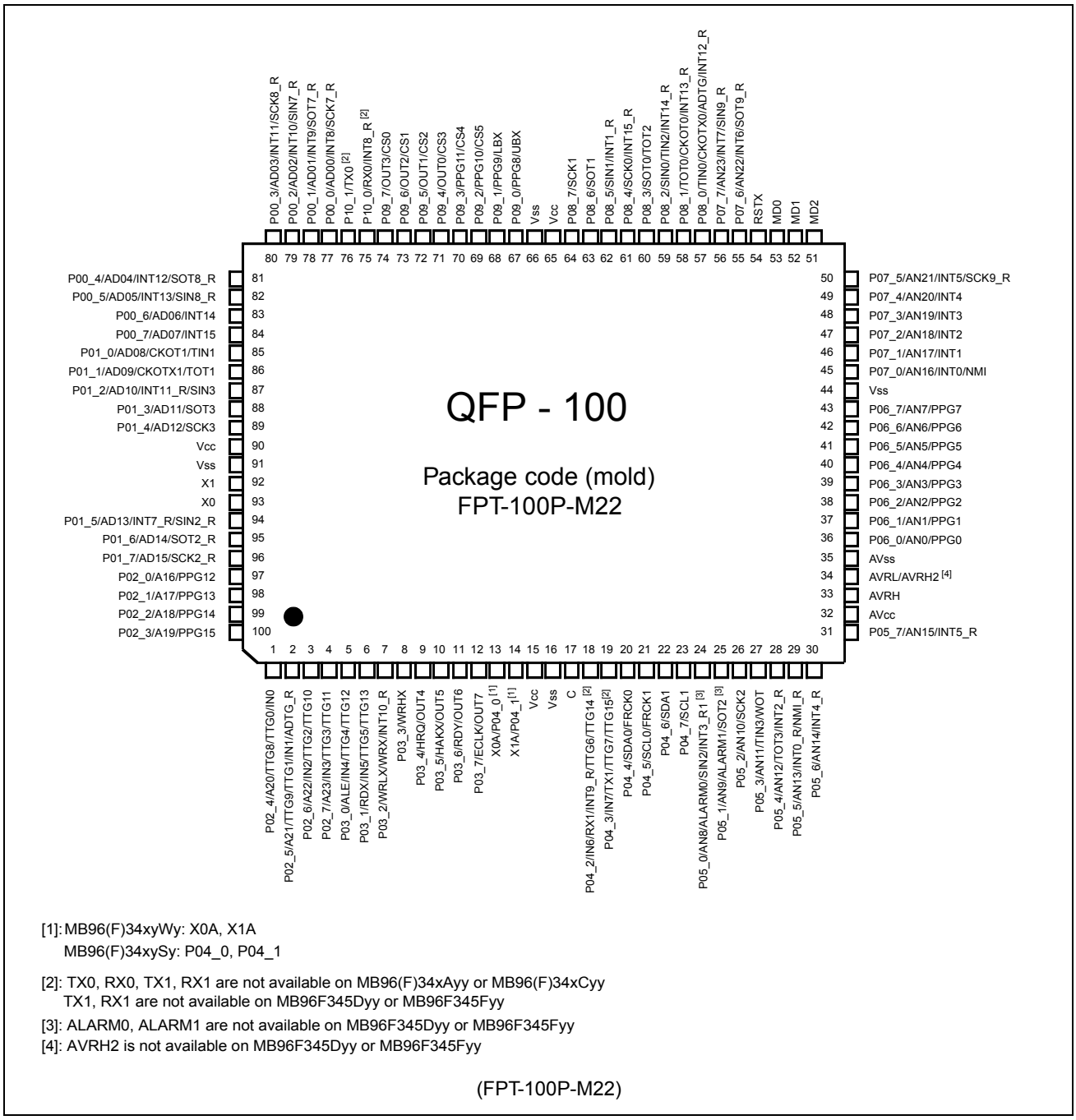
[3]: CAN interfaces are not available on MB96(F)34xAyy or MB96(F)34xCyy
CAN1 is not available on MB96F345Dyy or MB96F345Fyy

[4]: Alarm comparator is not available on MB96F345Dyy or MB96F345Fyy

[5]: A/D converter reference voltage switch is not available on MB96F345Dyy or MB96F345Fyy

3. Pin Assignments

Figure 2. Pin assignment of MB96(F)34x (FPT-100P-M22)



[1]: MB96(F)34xyWy: X0A, X1A
MB96(F)34xySy: P04_0, P04_1

[2]: TX0, RX0, TX1, RX1 are not available on MB96(F)34xAyy or MB96(F)34xCyy
TX1, RX1 are not available on MB96F345Dyy or MB96F345Fyy

[3]: ALARM0, ALARM1 are not available on MB96F345Dyy or MB96F345Fyy

[4]: AVRH2 is not available on MB96F345Dyy or MB96F345Fyy

(FPT-100P-M22)

Remark:

MB96(F)34x products are pin-compatible to F^{2}MC-16LX family MB90340 series.

4. Pin Function Description

Table 1: Pin Function description

Pin name	Feature	Description
ADn	External bus	External bus interface (multiplexed mode) address output and data input/output
ADTG	ADC	A/D converter trigger input
ADTG_R	ADC	Relocated A/D converter trigger input
ALARMn	Alarm comparator	Alarm Comparator n input
ALE	External bus	External bus Address Latch Enable output
An	External bus	External bus address output
ANn	ADC	A/D converter channel n input
AV_{CC}	Supply	Analog circuits power supply
AVRH	ADC	A/D converter high reference voltage input
AVRH2	ADC	Alternative A/D converter high reference voltage input
AVRL	ADC	A/D converter low reference voltage input
AV_{SS}	Supply	Analog circuits power supply
C	Voltage regulator	Internally regulated power supply stabilization capacitor pin
CKOTn	Clock output function	Clock Output function n output
CKOTXn	Clock output function	Clock Output function n inverted output
ECLK	External bus	External bus clock output
CSn	External bus	External bus chip select n output
FRCKn	Free Running Timer	Free Running Timer n input
HAKX	External bus	External bus Hold Acknowledge
HRQ	External bus	External bus Hold Request
INn	ICU	Input Capture Unit n input
INTn	External Interrupt	External Interrupt n input
INTn_R	External Interrupt	Relocated External Interrupt n input
LBX	External bus	External Bus Interface Lower Byte select strobe output
MDn	Core	Input pins for specifying the operating mode.
NMI	External Interrupt	Non-Maskable Interrupt input
NMI_R	External Interrupt	Relocated Non-Maskable Interrupt input
OUTn	OCU	Output Compare Unit n waveform output
Pxx_n	GPIO	General purpose IO
PPGn	PPG	Programmable Pulse Generator n output
RDX	External bus	External bus interface read strobe output

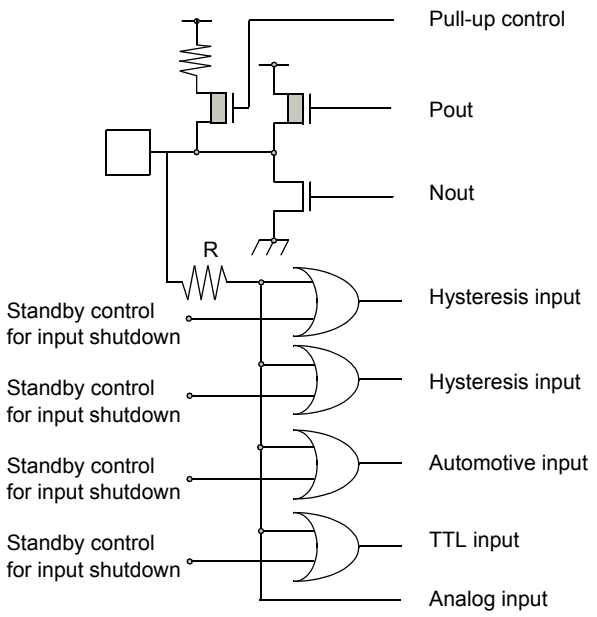
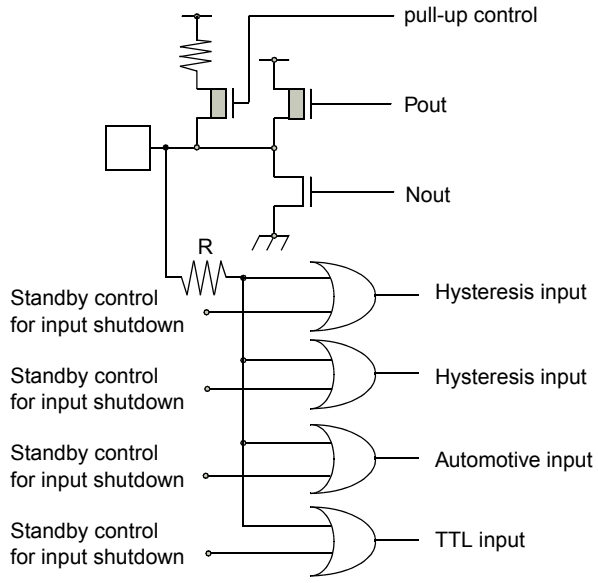
Type	Circuit	Remarks
I		■ CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) ■ 2 different CMOS hysteresis inputs with input shutdown function * ■ Automotive input with input shutdown function ■ TTL input with input shutdown function * ■ Programmable pull-up resistor: 50kΩ approx. ■ Analog input *MB96F345Dyy or MB96F345Fyy: Only Automotive input and CMOS hysteresis input (0.7/0.3) are supported
N		■ CMOS level output (I_{OL} = 3mA, I_{OH} = -3mA) ■ 2 different CMOS hysteresis inputs with input shutdown function * ■ Automotive input with input shutdown function ■ TTL input with input shutdown function * ■ Programmable pull-up resistor: 50kΩ approx. *MB96F345Dyy or MB96F345Fyy: Only Automotive input and CMOS hysteresis input (0.7/0.3) are supported

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000067_H	RLT1 - Reload Register - for reading			R
000068_H	RLT2 - Timer Control Status Register Low	TMCSRL2	TMCSR2	R/W
000069_H	RLT2 - Timer Control Status Register High	TMCSRH2		R/W
$00006A_H$	RLT2 - Reload Register - for writing		TMRLR2	W
$00006A_H$	RLT2 - Reload Register - for reading		TMR2	R
$00006B_H$	RLT2 - Reload Register - for writing			W
$00006B_H$	RLT2 - Reload Register - for reading			R
$00006C_H$	RLT3 - Timer Control Status Register Low	TMCSRL3	TMCSR3	R/W
$00006D_H$	RLT3 - Timer Control Status Register High	TMCSRH3		R/W
$00006E_H$	RLT3 - Reload Register - for writing		TMRLR3	W
$00006E_H$	RLT3 - Reload Register - for reading		TMR3	R
$00006F_H$	RLT3 - Reload Register - for writing			W
$00006F_H$	RLT3 - Reload Register - for reading			R
000070_H	RLT6 - Timer Control Status Register Low (dedic. RLT for PPG)	TMCSRL6	TMCSR6	R/W
000071_H	RLT6 - Timer Control Status Register High (dedic. RLT for PPG)	TMCSRH6		R/W
000072_H	RLT6 - Reload Register (dedic. RLT for PPG) - for writing		TMRLR6	W
000072_H	RLT6 - Reload Register (dedic. RLT for PPG) - for reading		TMR6	R
000073_H	RLT6 - Reload Register (dedic. RLT for PPG) - for writing			W
000073_H	RLT6 - Reload Register (dedic. RLT for PPG) - for reading			R
000074_H	PPG3-PPG0 - General Control register 1 Low	GCN1L0	GCN10	R/W
000075_H	PPG3-PPG0 - General Control register 1 High	GCN1H0		R/W
000076_H	PPG3-PPG0 - General Control register 2 Low	GCN2L0	GCN20	R/W
000077_H	PPG3-PPG0 - General Control register 2 High	GCN2H0		R/W
000078_H	PPG0 - Timer register		PTMR0	R
000079_H	PPG0 - Timer register			R
$00007A_H$	PPG0 - Period setting register		PCSR0	W
$00007B_H$	PPG0 - Period setting register			W
$00007C_H$	PPG0 - Duty cycle register		PDUT0	W
$00007D_H$	PPG0 - Duty cycle register			W
$00007E_H$	PPG0 - Control status register Low	PCNL0	PCN0	R/W
$00007F_H$	PPG0 - Control status register High	PCNH0		R/W
000080_H	PPG1 - Timer register		PTMR1	R

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$0003D9_H$	Memory Patch function - Patch data 4 High	PFDH4		R/W
$0003DA_H$	Memory Patch function - Patch data 5 Low	PFDL5	PFD5	R/W
$0003DB_H$	Memory Patch function - Patch data 5 High	PFDH5		R/W
$0003DC_H$	Memory Patch function - Patch data 6 Low	PFDL6	PFD6	R/W
$0003DD_H$	Memory Patch function - Patch data 6 High	PFDH6		R/W
$0003DE_H$	Memory Patch function - Patch data 7 Low	PFDL7	PFD7	R/W
$0003DF_H$	Memory Patch function - Patch data 7 High	PFDH7		R/W
$0003E0_H$	Data Flash Control and Status register A	DFCSA		R/W
$0003E1_H$	Data Flash Write command sequencer Control register A	DFWCA		R/W
$0003E2_H$	Data Flash Write command sequencer Status register A	DFWSA		R/W
$0003E3_H$-$0003F0_H$	Reserved			-
$0003F1_H$	Memory Control Status Register A	MCSRA		R/W
$0003F2_H$	Memory Timing Configuration Register A Low	MTCRAL	MTCRA	R/W
$0003F3_H$	Memory Timing Configuration Register A High	MTCRAH		R/W
$0003F4_H$	Reserved			-
$0003F5_H$	Memory Control Status Register B	MCSRB		R/W
$0003F6_H$	Memory Timing Configuration Register B Low	MTCRBL	MTCRB	R/W
$0003F7_H$	Memory Timing Configuration Register B High	MTCRBH		R/W
$0003F8_H$	Flash Memory Write Control register 0	FMWC0		R/W
$0003F9_H$	Flash Memory Write Control register 1	FMWC1		R/W
$0003FA_H$	Flash Memory Write Control register 2	FMWC2		R/W
$0003FB_H$	Flash Memory Write Control register 3	FMWC3		R/W
$0003FC_H$	Flash Memory Write Control register 4	FMWC4		R/W
$0003FD_H$	Flash Memory Write Control register 5	FMWC5		R/W
$0003FE_H$-$0003FF_H$	Reserved			-
000400_H	Standby Mode control register	SMCR		R/W
000401_H	Clock select register	CKSR		R/W
000402_H	Clock Stabilization select register	CKSSR		R/W
000403_H	Clock monitor register	CKMR		R
000404_H	Clock Frequency control register Low	CKFCRL	CKFCR	R/W
000405_H	Clock Frequency control register High	CKFCRH		R/W
000406_H	PLL Control register Low	PLLCRL	PLLCR	R/W

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$00043B_H$-000443_H	Reserved			-
000444_H	I/O Port P00 - Port Input Enable Register	PIER00		R/W
000445_H	I/O Port P01 - Port Input Enable Register	PIER01		R/W
000446_H	I/O Port P02 - Port Input Enable Register	PIER02		R/W
000447_H	I/O Port P03 - Port Input Enable Register	PIER03		R/W
000448_H	I/O Port P04 - Port Input Enable Register	PIER04		R/W
000449_H	I/O Port P05 - Port Input Enable Register	PIER05		R/W
$00044A_H$	I/O Port P06 - Port Input Enable Register	PIER06		R/W
$00044B_H$	I/O Port P07 - Port Input Enable Register	PIER07		R/W
$00044C_H$	I/O Port P08 - Port Input Enable Register	PIER08		R/W
$00044D_H$	I/O Port P09 - Port Input Enable Register	PIER09		R/W
$00044E_H$	I/O Port P10 - Port Input Enable Register	PIER10		R/W
$00044F_H$-000457_H	Reserved			-
000458_H	I/O Port P00 - Port Input Level Register	PILR00		R/W
000459_H	I/O Port P01 - Port Input Level Register	PILR01		R/W
$00045A_H$	I/O Port P02 - Port Input Level Register	PILR02		R/W
$00045B_H$	I/O Port P03 - Port Input Level Register	PILR03		R/W
$00045C_H$	I/O Port P04 - Port Input Level Register	PILR04		R/W
$00045D_H$	I/O Port P05 - Port Input Level Register	PILR05		R/W
$00045E_H$	I/O Port P06 - Port Input Level Register	PILR06		R/W
$00045F_H$	I/O Port P07 - Port Input Level Register	PILR07		R/W
000460_H	I/O Port P08 - Port Input Level Register	PILR08		R/W
000461_H	I/O Port P09 - Port Input Level Register	PILR09		R/W
000462_H	I/O Port P10 - Port Input Level Register	PILR10		R/W
000463_H-$00046B_H$	Reserved			-
$00046C_H$	I/O Port P00 - Extended Port Input Level Register	EPILR00		R/W
$00046D_H$	I/O Port P01 - Extended Port Input Level Register	EPILR01		R/W
$00046E_H$	I/O Port P02 - Extended Port Input Level Register	EPILR02		R/W
$00046F_H$	I/O Port P03 - Extended Port Input Level Register	EPILR03		R/W
000470_H	I/O Port P04 - Extended Port Input Level Register	EPILR04		R/W
000471_H	I/O Port P05 - Extended Port Input Level Register	EPILR05		R/W
000472_H	I/O Port P06 - Extended Port Input Level Register	EPILR06		R/W

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$0004E3_H$	RTC - Second Register	WTSR		R/W
$0004E4_H$	RTC - Minutes	WTMR		R/W
$0004E5_H$	RTC - Hour	WTHR		R/W
$0004E6_H$	RTC - Timer Control Extended Register	WTCER		R/W
$0004E7_H$	RTC - Clock select register	WTCKSR		R/W
$0004E8_H$	RTC - Timer Control Register Low	WTCRL	WTCR	R/W
$0004E9_H$	RTC - Timer Control Register High	WTCRH		R/W
$0004EA_H$	CAL - Calibration unit Control register	CUCR		R/W
$0004EB_H$	Reserved			-
$0004EC_H$	CAL - Duration Timer Data Register Low	CUTDL	CUTD	R/W
$0004ED_H$	CAL - Duration Timer Data Register High	CUTDH		R/W
$0004EE_H$	CAL - Calibration Timer Register 2 Low	CUTR2L	CUTR2	R
$0004EF_H$	CAL - Calibration Timer Register 2 High	CUTR2H		R
$0004F0_H$	CAL - Calibration Timer Register 1 Low	CUTR1L	CUTR1	R
$0004F1_H$	CAL - Calibration Timer Register 1 High	CUTR1H		R
$0004F2_H$-$0004F9_H$	Reserved			-
$0004FA_H$	RLT - Timer input select (for Cascading)	TMISR		R/W
$0004FB_H$-$00053D_H$	Reserved			-
$00053E_H$	USART7 - Serial Mode Register	SMR7		R/W
$00053F_H$	USART7 - Serial Control Register	SCR7		R/W
000540_H	USART7 - Serial TX Register	TDR7		W
000540_H	USART7 - Serial RX Register	RDR7		R
000541_H	USART7 - Serial Status Register	SSR7		R/W
000542_H	USART7 - Ext. Control/Com. Register	ECCR7		R/W
000543_H	USART7 - Ext. Status Com. Register	ESCR7		R/W
000544_H	USART7 - Baud Rate Generator Register Low	BGRL7	BGR7	R/W
000545_H	USART7 - Baud Rate Generator Register High	BGRH7		R/W
000546_H	USART7 - Extended Serial Interrupt Register	ESIR7		R/W
000547_H	Reserved			-
000548_H	USART8 - Serial Mode Register	SMR8		R/W
000549_H	USART8 - Serial Control Register	SCR8		R/W
$00054A_H$	USART8 - Serial TX Register	TDR8		W

Table 5: Interrupt vector table MB96(F)34x

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
30	384_H	EXTINT13	Yes	30	External Interrupt 13
31	380_H	EXTINT14	Yes	31	External Interrupt 14
32	$37C_H$	EXTINT15	Yes	32	External Interrupt 15
33	378_H	CAN0	No	33	CAN Controller 0 (except MB96(F)34xAyy or MB96(F)34xCyy)
34	374_H	CAN1	No	34	CAN Controller 1 (except MB96(F)34xAyy, MB96(F)34xCyy, MB96F345Dyy or MB96F345Fyy)
35	370_H	PPG0	Yes	35	Programmable Pulse Generator 0
36	$36C_H$	PPG1	Yes	36	Programmable Pulse Generator 1
37	368_H	PPG2	Yes	37	Programmable Pulse Generator 2
38	364_H	PPG3	Yes	38	Programmable Pulse Generator 3
39	360_H	PPG4	Yes	39	Programmable Pulse Generator 4
40	$35C_H$	PPG5	Yes	40	Programmable Pulse Generator 5
41	358_H	PPG6	Yes	41	Programmable Pulse Generator 6
42	354_H	PPG7	Yes	42	Programmable Pulse Generator 7
43	350_H	PPG8	Yes	43	Programmable Pulse Generator 8
44	$34C_H$	PPG9	Yes	44	Programmable Pulse Generator 9
45	348_H	PPG10	Yes	45	Programmable Pulse Generator 10
46	344_H	PPG11	Yes	46	Programmable Pulse Generator 11
47	340_H	PPG12	Yes	47	Programmable Pulse Generator 12
48	$33C_H$	PPG13	Yes	48	Programmable Pulse Generator 13
49	338_H	PPG14	Yes	49	Programmable Pulse Generator 14
50	334_H	PPG15	Yes	50	Programmable Pulse Generator 15
51	330_H	RLT0	Yes	51	Reload Timer 0
52	$32C_H$	RLT1	Yes	52	Reload Timer 1
53	328_H	RLT2	Yes	53	Reload Timer 2
54	324_H	RLT3	Yes	54	Reload Timer 3
55	320_H	PPGRLT	Yes	55	Reload Timer 6 - dedicated for PPG
56	$31C_H$	ICU0	Yes	56	Input Capture Unit 0
57	318_H	ICU1	Yes	57	Input Capture Unit 1
58	314_H	ICU2	Yes	58	Input Capture Unit 2
59	310_H	ICU3	Yes	59	Input Capture Unit 3

[4]: The maximum permitted power dissipation depends on the ambient temperature, the air flow velocity and the thermal conductance of the package on the PCB.The actual power dissipation depends on the customer application and can be calculated as follows:
$P_D = P_{IO} + P_{INT}$
$P_{IO} = \Sigma (V_{OL} * I_{OL} + V_{OH} * I_{OH})$ (IO load power dissipation, sum is performed on all IO ports)
$P_{INT} = V_{CC} * (I_{CC} + I_A)$ (internal power dissipation)
I_{CC} is the total core current consumption into V_{CC} as described in the “DC characteristics” and depends on the selected operation mode and clock frequency and the usage of functions like Flash programming or the clock modulator.I_A is the analog current consumption into AV_{CC}.

[5]: Worst case value for a package mounted on single layer PCB at specified T_A without air flow.

[6]: Please contact Cypress for reliability limitations when using under these conditions.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed any of these ratings.

14.2 Recommended Operating Conditions

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}	3.0	-	5.5	V	
Smoothing capacitor at C pin	C_S	3.5	4.7 - 10	15	µF	Use a low inductance capacitor (for example X7R ceramic capacitor)

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Sleep modes[1]	I_{CCSRCH}	RC Sleep mode with CLKS1/2 = CLKP1/2 = 2MHz (CLKMC, CLKPLL and CLKSC stopped)	+25°C	0.9	1.4	mA	Flash devices
			+125°C	1.5	4.1		
			+25°C	0.9	1.4	mA	MB96345/346
			+125°C	1.5	3.1		
	I_{CCSRCL}	RC Sleep mode with CLKS1/2 = CLKP1/2 = 100kHz, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)	+25°C	0.3	0.5	mA	MB96F346/F347/F348
			+125°C	0.8	3.4		
			+25°C	0.09	0.2	mA	MB96F345
			+125°C	0.59	3.1		
			+25°C	0.3	0.5	mA	MB96345/346
			+125°C	0.8	2.3		
		RC Sleep mode with CLKS1/2 = CLKP1/2 = 100kHz, SMCR:LPMSS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode)	+25°C	0.06	0.15	mA	Flash devices
			+125°C	0.56	3		
			+25°C	0.06	0.15	mA	MB96345/346
			+125°C	0.56	1.9		
	I_{CCSSUB}	Sub Sleep mode with CLKS1/2 = CLKP1/2 = 32kHz (CLKMC, CLKPLL and CLKRC stopped)	+25°C	0.04	0.12	mA	Flash devices
			+125°C	0.54	2.9		
			+25°C	0.04	0.12	mA	MB96345/346
			+125°C	0.54	1.85		

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

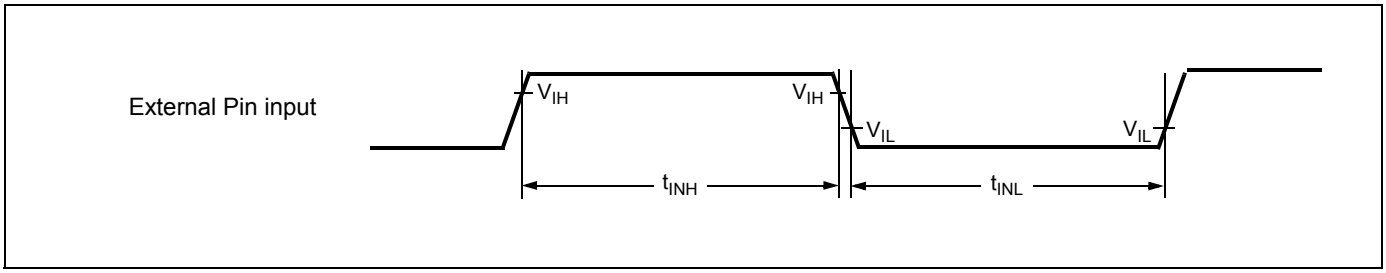
Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current for active Clock modulator	$I_{CCCLOMO}$	Clock modulator enabled (CMCR:PDX = 1)	-	3	4.5	mA	Must be added to all current above
Flash Write/Erase current	$I_{CCFLASH}$	Current for one Flash module	-	15	40	mA	Must be added to all current above
	$I_{CCDFLASH}$	Current for one Data Flash module		10	20	mA	Must be added to all current above
Input capacitance	C_{IN}	-	-	5	15	pF	Other than C, AV_{CC}, AV_{SS}, AVRH, AVRL, V_{CC}, V_{SS}
[1]: The power supply current is measured with a 4MHz external clock connected to the Main oscillator and a 32kHz external clock connected to the Sub oscillator. See chapter “Standby mode and voltage regulator control circuit” of the Hardware Manual for further details about voltage regulator control.							

14.4.5 External Input timing

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

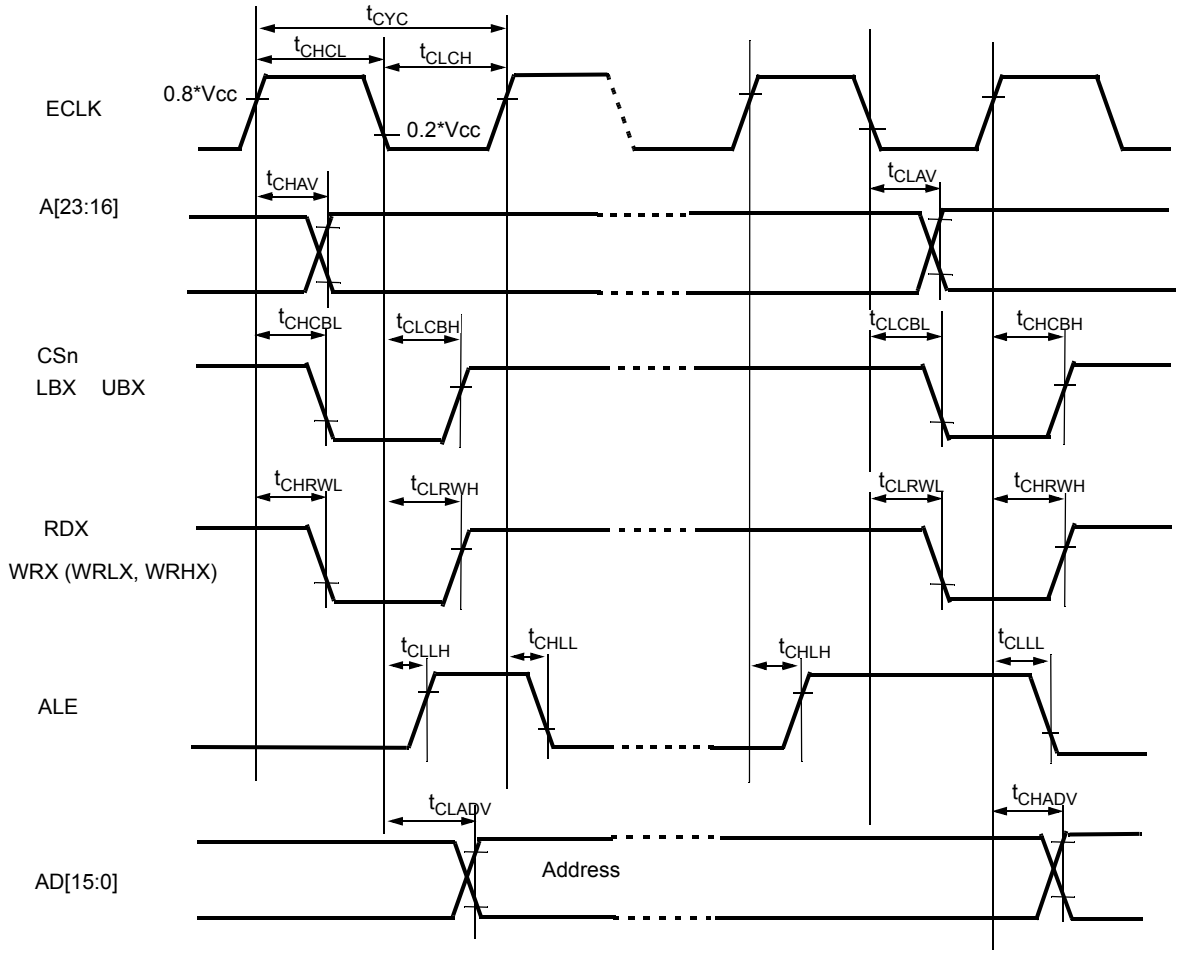
Parameter	Symbol	Pin	Condition	Value		Unit	Used Pin input function
				Min	Max		
Input pulse width	t_{INH} t_{INL}	INTn(_R)	-	200	-	ns	External Interrupt
		NMI(_R)					NMI
		Pnn_m		$2*t_{CLKP1}$ + 200 ($t_{CLKP1}=1/f_{CLKP1}$)	-	ns	General Purpose IO
		TINn(_R)					Reload Timer
		TTGn(_R)					PPG Trigger input
		ADTG(_R)					AD Converter Trigger
		FRCKn(_R)					Free Running Timer external clock
		INn(_R)					Input Capture

Note : Relocated Resource Inputs have same characteristics



14.4.6 External Bus timing

Note: The values given below are for an I/O driving strength IO_{drive} = 5mA. If IO_{drive} is 2mA, all the maximum output timing described in the different tables must then be increased by 10ns.



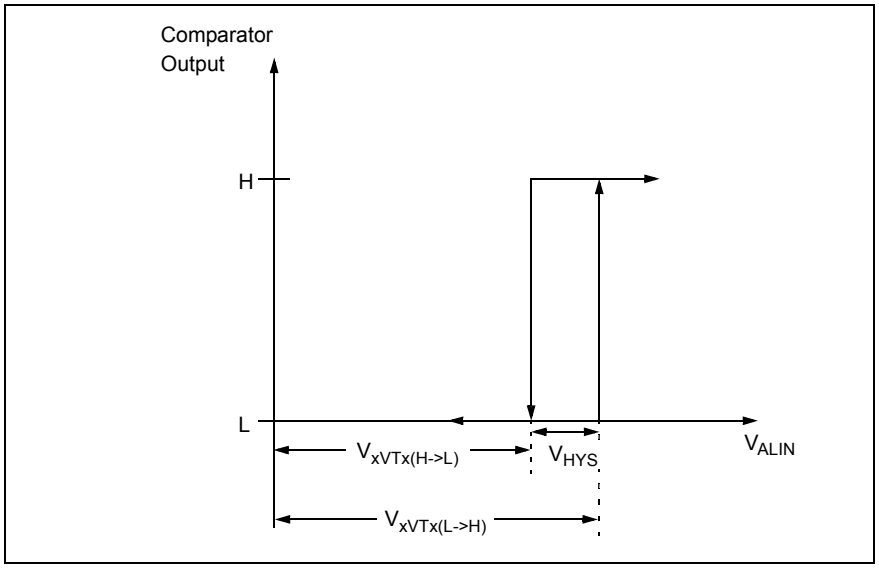
Refer to the Hardware Manual for detailed Timing Charts

(T_A = –40°C to +125°C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
RDX ↑ ⇒ ALE ↑ time	t_{RHLH}	RDX, ALE	EACL:STS=1 and EACL:ACE=1	$3t_{CYC}/2 - 10$	-	ns	
			other ECL:STS, EACL:ACE setting	$t_{CYC}/2 - 10$	-		
Valid address ⇒ ECLK ↑ time	t_{AVCH}	A[23:16], ECLK	-	$t_{CYC} - 15$	-	ns	
	t_{ADVCH}	AD[15:0], ECLK		$t_{CYC}/2 - 15$	-		
RDX ↓ ⇒ ECLK ↑ time	t_{RLCH}	RDX, ECLK	-	$t_{CYC}/2 - 10$	-	ns	
ALE ↓ ⇒ RDX ↓ time	t_{LLRL}	ALE, RDX	EACL:STS=0	$t_{CYC}/2 - 10$	-	ns	
			EACL:STS=1	– 10	-		
ECLK↑ ⇒ Valid data input	t_{CHDV}	AD[15:0], ECLK	-	-	$t_{CYC} - 50$	ns	

(T_A = –40°C to +125°C, V_{CC} = 3.0 to 4.5V, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
ALE pulse width	t_{LHLL}	ALE	EACL:STS=0 and EACL:ACE=0	$t_{CYC}/2 - 8$	-	ns	
			EACL:STS=1	$t_{CYC} - 8$	-		
			EACL:STS=0 and EACL:ACE=1	$3t_{CYC}/2 - 8$	-		
Valid address ⇒ ALE ↓ time	t_{AVLL}	ALE, A[23:16],	EACL:STS=0 and EACL:ACE=0	$t_{CYC} - 20$	-	ns	
			EACL:STS=1 and EACL:ACE=0	$3t_{CYC}/2 - 20$	-		
			EACL:STS=0 and EACL:ACE=1	$2t_{CYC} - 20$	-		
			EACL:STS=1 and EACL:ACE=1	$5t_{CYC}/2 - 20$	-		
	t_{ADVLL}	ALE, AD[15:0]	EACL:STS=0 and EACL:ACE=0	$t_{CYC}/2 - 20$	-	ns	
			EACL:STS=1 and EACL:ACE=0	$t_{CYC} - 20$	-		
			EACL:STS=0 and EACL:ACE=1	$3t_{CYC}/2 - 20$	-		
			EACL:STS=1 and EACL:ACE=1	$2t_{CYC} - 20$	-		
ALE ↓ ⇒ Address valid time	t_{LLAX}	ALE, AD[15:0]	EACL:STS=0	$t_{CYC}/2 - 20$	-	ns	
			EACL:STS=1	-20	-		
Valid address ⇒ RDX ↓ time	t_{AVRL}	RDX, A[23:16]	EACL:ACE=0	$3t_{CYC}/2 - 20$	-	ns	
			EACL:ACE=1	$5t_{CYC}/2 - 20$	-		
	t_{ADVRL}	RDX, AD[15:0]	EACL:ACE=0	$t_{CYC} - 20$	-	ns	
			EACL:ACE=1	$2t_{CYC} - 20$	-		


Comparator
Output
H
L
$V_{xVTx(H->L)}$
V_{HYS}
V_{ALIN}
$V_{xVTx(L->H)}$

14.7 Low Voltage Detector Characteristics

(T_A = -40 °C to +125 °C, V_{cc} = AV_{cc} = 3.0V - 5.5V, V_{ss} = AV_{ss} = 0V)

Parameter	Symbol	Value [1]		Value [2]		Unit	Remarks
		Min	Max	Min	Max		
Stabilization time	$T_{LVDSTAB}$	-	75	-	110	µs	After power-up or change of detection level
Level 0	V_{DL0}	2.7	2.9	2.65	2.95	V	CILCR:LVL[3:0]="0000"
Level 1	V_{DL1}	2.9	3.1	2.85	3.2	V	CILCR:LVL[3:0]="0001"
Level 2	V_{DL2}	3.1	3.3	3.05	3.4	V	CILCR:LVL[3:0]="0010"
Level 3	V_{DL3}	3.5	3.75	3.45	3.85	V	CILCR:LVL[3:0]="0011"
Level 4	V_{DL4}	3.6	3.85	3.55	3.95	V	CILCR:LVL[3:0]="0100"
Level 5	V_{DL5}	3.7	3.95	3.65	4.1	V	CILCR:LVL[3:0]="0101"
Level 6	V_{DL6}	3.8	4.05	3.75	4.2	V	CILCR:LVL[3:0]="0110"
Level 7	V_{DL7}	3.9	4.15	3.85	4.3	V	CILCR:LVL[3:0]="0111"
Level 8	V_{DL8}	4.0	4.25	3.95	4.4	V	CILCR:LVL[3:0]="1000"
Level 9	V_{DL9}	4.1	4.35	4.05	4.5	V	CILCR:LVL[3:0]="1001"
Level 10	V_{DL10}	not used		not used			
Level 11	V_{DL11}	not used		not used			
Level 12	V_{DL12}	not used		not used			
Level 13	V_{DL13}	not used		not used			
Level 14	V_{DL14}	not used		not used			
Level 15	V_{DL15}	not used		not used			

[1]: valid for all devices except devices listed under "[2]"

[2]: valid for: MB96F345

CILCR:LVL[3:0] are the low voltage detector level select bits of the CILCR register.

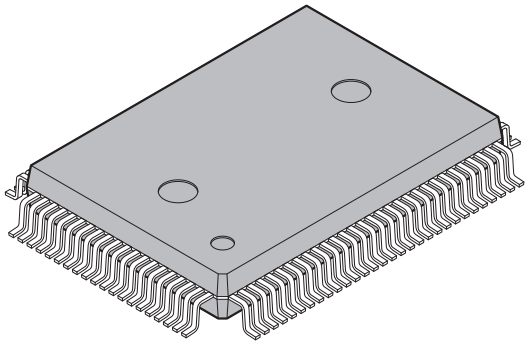
Levels 10 to 15 are not used in this device.

For correct detection, the slope of the voltage level must satisfy $\left|\frac{dV}{dt}\right| \leq 0.004\frac{V}{\mu s}$.

Faster variations are regarded as noise and may not be detected.

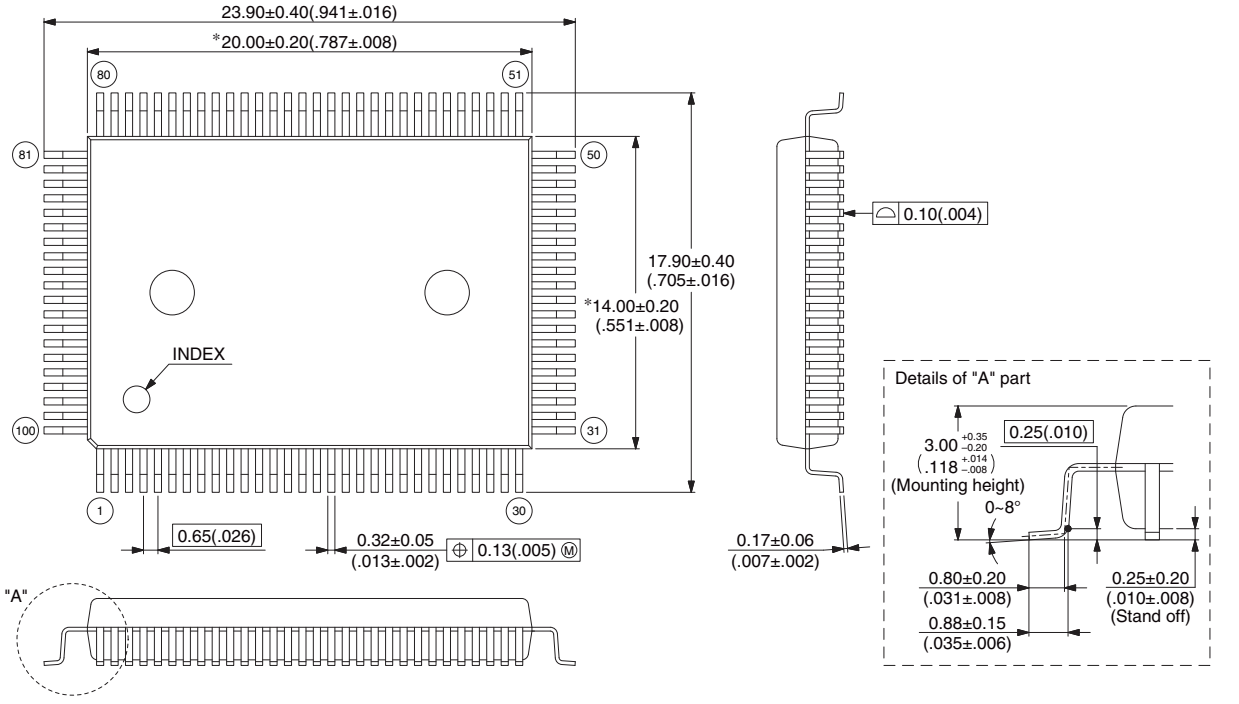
The functional operation of the MCU is guaranteed down to the minimum low voltage detection level of Vcc = 2.7V. The electrical characteristics however are only valid in the specified range (usually down to 3.0V).

17. Package Dimension MB96(F)34x QFP 100P

100-pin plastic QFP		
	Lead pitch	0.65 mm
	Package width × package length	14.00 mm × 20.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	3.35 mm MAX
	Code (Reference)	P-QFP100-14×20-0.65
(FPT-100P-M22)		

100-pin plastic QFP
(FPT-100P-M22)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.