Infineon Technologies - MB96F347RSAPQCR-GS-ERE2 Datasheet

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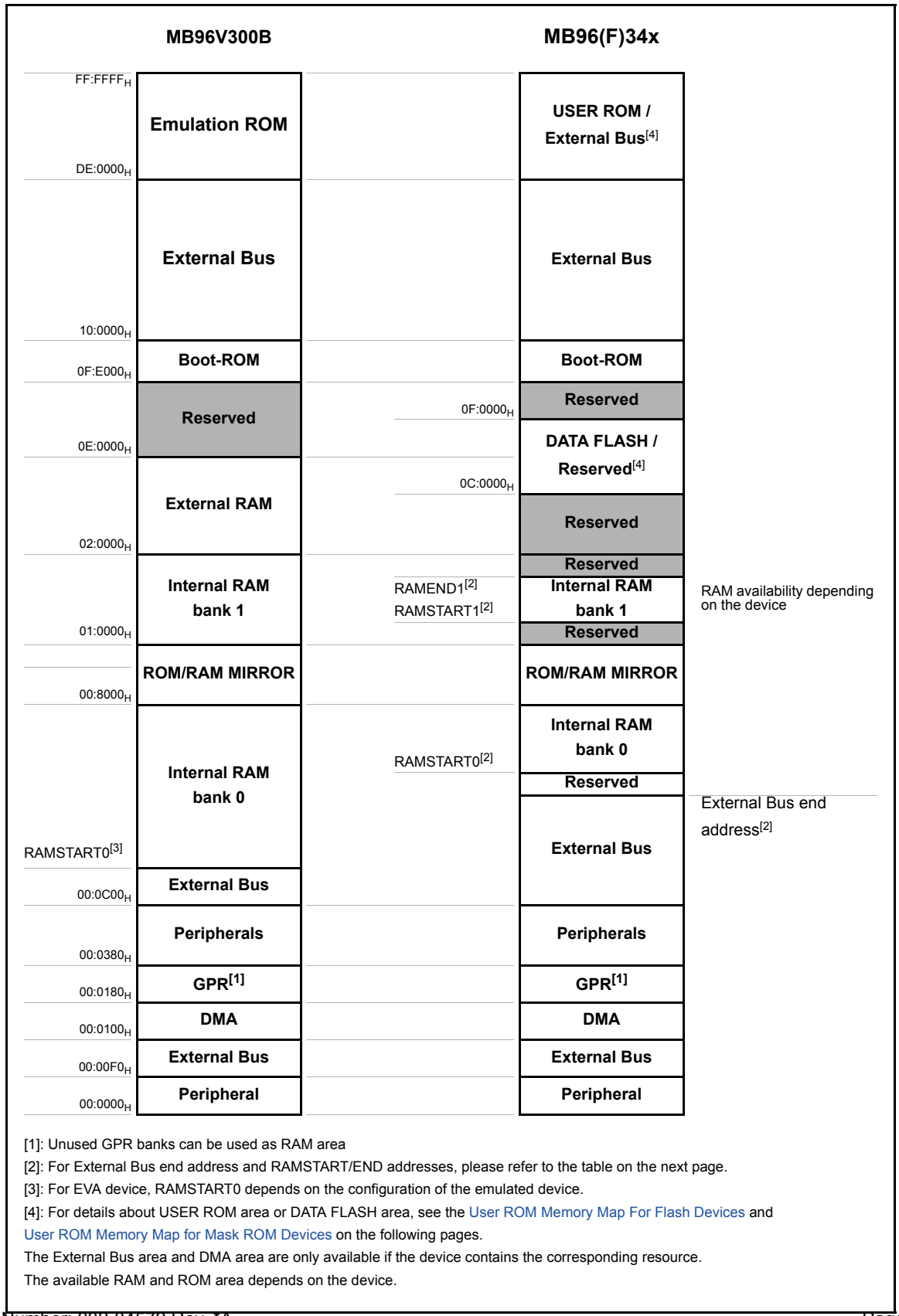
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	56MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, LVR, POR, PWM, WDT
Number of I/O	82
Program Memory Size	416KB (416K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-PQFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f347rsapqcr-gs-ere2

7. Memory Map



[1]: Unused GPR banks can be used as RAM area

[2]: For External Bus end address and RAMSTART/END addresses, please refer to the table on the next page.

[3]: For EVA device, RAMSTART0 depends on the configuration of the emulated device.

[4]: For details about USER ROM area or DATA FLASH area, see the User ROM Memory Map For Flash Devices and User ROM Memory Map for Mask ROM Devices on the following pages.

The External Bus area and DMA area are only available if the device contains the corresponding resource.

The available RAM and ROM area depends on the device.

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$00002B_H$	OCU0 - Compare Register			R/W
$00002C_H$	OCU1 - Compare Register		OCCP1	R/W
$00002D_H$	OCU1 - Compare Register			R/W
$00002E_H$	OCU2 - Output Compare Control Status	OCS2		R/W
$00002F_H$	OCU3 - Output Compare Control Status	OCS3		R/W
000030_H	OCU2 - Compare Register		OCCP2	R/W
000031_H	OCU2 - Compare Register			R/W
000032_H	OCU3 - Compare Register		OCCP3	R/W
000033_H	OCU3 - Compare Register			R/W
000034_H	OCU4 - Output Compare Control Status	OCS4		R/W
000035_H	OCU5 - Output Compare Control Status	OCS5		R/W
000036_H	OCU4 - Compare Register		OCCP4	R/W
000037_H	OCU4 - Compare Register			R/W
000038_H	OCU5 - Compare Register		OCCP5	R/W
000039_H	OCU5 - Compare Register			R/W
$00003A_H$	OCU6 - Output Compare Control Status	OCS6		R/W
$00003B_H$	OCU7 - Output Compare Control Status	OCS7		R/W
$00003C_H$	OCU6 - Compare Register		OCCP6	R/W
$00003D_H$	OCU6 - Compare Register			R/W
$00003E_H$	OCU7 - Compare Register		OCCP7	R/W
$00003F_H$	OCU7 - Compare Register			R/W
000040_H	ICU0/ICU1 - Control Status Register	ICS01		R/W
000041_H	ICU0/ICU1 - Edge register	ICE01		R/W
000042_H	ICU0 - Capture Register Low	IPCPL0	IPCP0	R
000043_H	ICU0 - Capture Register High	IPCPH0		R
000044_H	ICU1 - Capture Register Low	IPCPL1	IPCP1	R
000045_H	ICU1 - Capture Register High	IPCPH1		R
000046_H	ICU2/ICU3 - Control Status Register	ICS23		R/W
000047_H	ICU2/ICU3 - Edge register	ICE23		R/W
000048_H	ICU2 - Capture Register Low	IPCPL2	IPCP2	R
000049_H	ICU2 - Capture Register High	IPCPH2		R
$00004A_H$	ICU3 - Capture Register Low	IPCPL3	IPCP3	R

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000081_H	PPG1 - Timer register			R
000082_H	PPG1 - Period setting register		PCSR1	W
000083_H	PPG1 - Period setting register			W
000084_H	PPG1 - Duty cycle register		PDUT1	W
000085_H	PPG1 - Duty cycle register			W
000086_H	PPG1 - Control status register Low	PCNL1	PCN1	R/W
000087_H	PPG1 - Control status register High	PCNH1		R/W
000088_H	PPG2 - Timer register		PTMR2	R
000089_H	PPG2 - Timer register			R
$00008A_H$	PPG2 - Period setting register		PCSR2	W
$00008B_H$	PPG2 - Period setting register			W
$00008C_H$	PPG2 - Duty cycle register		PDUT2	W
$00008D_H$	PPG2 - Duty cycle register			W
$00008E_H$	PPG2 - Control status register Low	PCNL2	PCN2	R/W
$00008F_H$	PPG2 - Control status register High	PCNH2		R/W
000090_H	PPG3 - Timer register		PTMR3	R
000091_H	PPG3 - Timer register			R
000092_H	PPG3 - Period setting register		PCSR3	W
000093_H	PPG3 - Period setting register			W
000094_H	PPG3 - Duty cycle register		PDUT3	W
000095_H	PPG3 - Duty cycle register			W
000096_H	PPG3 - Control status register Low	PCNL3	PCN3	R/W
000097_H	PPG3 - Control status register High	PCNH3		R/W
000098_H	PPG7-PPG4 - General Control register 1 Low	GCN1L1	GCN11	R/W
000099_H	PPG7-PPG4 - General Control register 1 High	GCN1H1		R/W
$00009A_H$	PPG7-PPG4 - General Control register 2 Low	GCN2L1	GCN21	R/W
$00009B_H$	PPG7-PPG4 - General Control register 2 High	GCN2H1		R/W
$00009C_H$	PPG4 - Timer register		PTMR4	R
$00009D_H$	PPG4 - Timer register			R
$00009E_H$	PPG4 - Period setting register		PCSR4	W
$00009F_H$	PPG4 - Period setting register			W
$0000A0_H$	PPG4 - Duty cycle register		PDUT4	W

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$0000C1_H$	USART0 - Serial Control Register	SCR0		R/W
$0000C2_H$	USART0 - TX Register	TDR0		W
$0000C2_H$	USART0 - RX Register	RDR0		R
$0000C3_H$	USART0 - Serial Status	SSR0		R/W
$0000C4_H$	USART0 - Control/Com. Register	ECCR0		R/W
$0000C5_H$	USART0 - Ext. Status Register	ESCR0		R/W
$0000C6_H$	USART0 - Baud Rate Generator Register Low	BGRL0	BGR0	R/W
$0000C7_H$	USART0 - Baud Rate Generator Register High	BGRH0		R/W
$0000C8_H$	USART0 - Extended Serial Interrupt Register	ESIR0		R/W
$0000C9_H$	Reserved			-
$0000CA_H$	USART1 - Serial Mode Register	SMR1		R/W
$0000CB_H$	USART1 - Serial Control Register	SCR1		R/W
$0000CC_H$	USART1 - TX Register	TDR1		W
$0000CC_H$	USART1 - RX Register	RDR1		R
$0000CD_H$	USART1 - Serial Status	SSR1		R/W
$0000CE_H$	USART1 - Control/Com. Register	ECCR1		R/W
$0000CF_H$	USART1 - Ext. Status Register	ESCR1		R/W
$0000D0_H$	USART1 - Baud Rate Generator Register Low	BGRL1	BGR1	R/W
$0000D1_H$	USART1 - Baud Rate Generator Register High	BGRH1		R/W
$0000D2_H$	USART1 - Extended Serial Interrupt Register	ESIR1		R/W
$0000D3_H$	Reserved			-
$0000D4_H$	USART2 - Serial Mode Register	SMR2		R/W
$0000D5_H$	USART2 - Serial Control Register	SCR2		R/W
$0000D6_H$	USART2 - TX Register	TDR2		W
$0000D6_H$	USART2 - RX Register	RDR2		R
$0000D7_H$	USART2 - Serial Status	SSR2		R/W
$0000D8_H$	USART2 - Control/Com. Register	ECCR2		R/W
$0000D9_H$	USART2 - Ext. Status Register	ESCR2		R/W
$0000DA_H$	USART2 - Baud Rate Generator Register Low	BGRL2	BGR2	R/W
$0000DB_H$	USART2 - Baud Rate Generator Register High	BGRH2		R/W
$0000DC_H$	USART2 - Extended Serial Interrupt Register	ESIR2		R/W
$0000DD_H$	Reserved			-

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$00043B_H$-000443_H	Reserved			-
000444_H	I/O Port P00 - Port Input Enable Register	PIER00		R/W
000445_H	I/O Port P01 - Port Input Enable Register	PIER01		R/W
000446_H	I/O Port P02 - Port Input Enable Register	PIER02		R/W
000447_H	I/O Port P03 - Port Input Enable Register	PIER03		R/W
000448_H	I/O Port P04 - Port Input Enable Register	PIER04		R/W
000449_H	I/O Port P05 - Port Input Enable Register	PIER05		R/W
$00044A_H$	I/O Port P06 - Port Input Enable Register	PIER06		R/W
$00044B_H$	I/O Port P07 - Port Input Enable Register	PIER07		R/W
$00044C_H$	I/O Port P08 - Port Input Enable Register	PIER08		R/W
$00044D_H$	I/O Port P09 - Port Input Enable Register	PIER09		R/W
$00044E_H$	I/O Port P10 - Port Input Enable Register	PIER10		R/W
$00044F_H$-000457_H	Reserved			-
000458_H	I/O Port P00 - Port Input Level Register	PILR00		R/W
000459_H	I/O Port P01 - Port Input Level Register	PILR01		R/W
$00045A_H$	I/O Port P02 - Port Input Level Register	PILR02		R/W
$00045B_H$	I/O Port P03 - Port Input Level Register	PILR03		R/W
$00045C_H$	I/O Port P04 - Port Input Level Register	PILR04		R/W
$00045D_H$	I/O Port P05 - Port Input Level Register	PILR05		R/W
$00045E_H$	I/O Port P06 - Port Input Level Register	PILR06		R/W
$00045F_H$	I/O Port P07 - Port Input Level Register	PILR07		R/W
000460_H	I/O Port P08 - Port Input Level Register	PILR08		R/W
000461_H	I/O Port P09 - Port Input Level Register	PILR09		R/W
000462_H	I/O Port P10 - Port Input Level Register	PILR10		R/W
000463_H-$00046B_H$	Reserved			-
$00046C_H$	I/O Port P00 - Extended Port Input Level Register	EPILR00		R/W
$00046D_H$	I/O Port P01 - Extended Port Input Level Register	EPILR01		R/W
$00046E_H$	I/O Port P02 - Extended Port Input Level Register	EPILR02		R/W
$00046F_H$	I/O Port P03 - Extended Port Input Level Register	EPILR03		R/W
000470_H	I/O Port P04 - Extended Port Input Level Register	EPILR04		R/W
000471_H	I/O Port P05 - Extended Port Input Level Register	EPILR05		R/W
000472_H	I/O Port P06 - Extended Port Input Level Register	EPILR06		R/W

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$0005AD_H$	PPG14 - Timer register			R
$0005AE_H$	PPG14 - Period setting register		PCSR14	W
$0005AF_H$	PPG14 - Period setting register			W
$0005B0_H$	PPG14 - Duty cycle register		PDUT14	W
$0005B1_H$	PPG14 - Duty cycle register			W
$0005B2_H$	PPG14 - Control status register Low	PCNL14	PCN14	R/W
$0005B3_H$	PPG14 - Control status register High	PCNH14		R/W
$0005B4_H$	PPG15 - Timer register		PTMR15	R
$0005B5_H$	PPG15 - Timer register			R
$0005B6_H$	PPG15 - Period setting register		PCSR15	W
$0005B7_H$	PPG15 - Period setting register			W
$0005B8_H$	PPG15 - Duty cycle register		PDUT15	W
$0005B9_H$	PPG15 - Duty cycle register			W
$0005BA_H$	PPG15 - Control status register Low	PCNL15	PCN15	R/W
$0005BB_H$	PPG15 - Control status register High	PCNH15		R/W
$0005BC_H$-$00065F_H$	Reserved			-
000660_H	Peripheral Resource Relocation Register 10	PRRR10		R/W
000661_H	Peripheral Resource Relocation Register 11	PRRR11		R/W
000662_H	Peripheral Resource Relocation Register 12	PRRR12		R/W
000663_H	Peripheral Resource Relocation Register 13	PRRR13		W
000664_H-$0006DF_H$	Reserved			-
$0006E0_H$	External Bus - Area configuration register 0 Low	EACL0	EAC0	R/W
$0006E1_H$	External Bus - Area configuration register 0 High	EACH0		R/W
$0006E2_H$	External Bus - Area configuration register 1 Low	EACL1	EAC1	R/W
$0006E3_H$	External Bus - Area configuration register 1 High	EACH1		R/W
$0006E4_H$	External Bus - Area configuration register 2 Low	EACL2	EAC2	R/W
$0006E5_H$	External Bus - Area configuration register 2 High	EACH2		R/W
$0006E6_H$	External Bus - Area configuration register 3 Low	EACL3	EAC3	R/W
$0006E7_H$	External Bus - Area configuration register 3 High	EACH3		R/W
$0006E8_H$	External Bus - Area configuration register 4 Low	EACL4	EAC4	R/W
$0006E9_H$	External Bus - Area configuration register 4 High	EACH4		R/W
$0006EA_H$	External Bus - Area configuration register 5 Low	EACL5	EAC5	R/W

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000801_H	CAN1 - Control register High (reserved)	CTRLRH1		R
000802_H	CAN1 - Status register Low	STATRL1	STATR1	R/W
000803_H	CAN1 - Status register High (reserved)	STATRH1		R
000804_H	CAN1 - Error Counter Low (Transmit)	ERRCNTL1	ERRCNT1	R
000805_H	CAN1 - Error Counter High (Receive)	ERRCNTH1		R
000806_H	CAN1 - Bit Timing Register Low	BTRL1	BTR1	R/W
000807_H	CAN1 - Bit Timing Register High	BTRH1		R/W
000808_H	CAN1 - Interrupt Register Low	INTRL1	INTR1	R
000809_H	CAN1 - Interrupt Register High	INTRH1		R
$00080A_H$	CAN1 - Test Register Low	TESTRL1	TESTR1	R/W
$00080B_H$	CAN1 - Test Register High (reserved)	TESTRH1		R
$00080C_H$	CAN1 - BRP Extension register Low	BRPERL1	BRPER1	R/W
$00080D_H$	CAN1 - BRP Extension register High (reserved)	BRPERH1		R
$00080E_H$-$00080F_H$	Reserved			-
000810_H	CAN1 - IF1 Command request register Low	IF1CREQL1	IF1CREQ1	R/W
000811_H	CAN1 - IF1 Command request register High	IF1CREQH1		R/W
000812_H	CAN1 - IF1 Command Mask register Low	IF1CMSKL1	IF1CMSK1	R/W
000813_H	CAN1 - IF1 Command Mask register High (reserved)	IF1CMSKH1		R
000814_H	CAN1 - IF1 Mask 1 Register Low	IF1MSK1L1	IF1MSK11	R/W
000815_H	CAN1 - IF1 Mask 1 Register High	IF1MSK1H1		R/W
000816_H	CAN1 - IF1 Mask 2 Register Low	IF1MSK2L1	IF1MSK21	R/W
000817_H	CAN1 - IF1 Mask 2 Register High	IF1MSK2H1		R/W
000818_H	CAN1 - IF1 Arbitration 1 Register Low	IF1ARB1L1	IF1ARB11	R/W
000819_H	CAN1 - IF1 Arbitration 1 Register High	IF1ARB1H1		R/W
$00081A_H$	CAN1 - IF1 Arbitration 2 Register Low	IF1ARB2L1	IF1ARB21	R/W
$00081B_H$	CAN1 - IF1 Arbitration 2 Register High	IF1ARB2H1		R/W
$00081C_H$	CAN1 - IF1 Message Control Register Low	IF1MCTRL1	IF1MCTR1	R/W
$00081D_H$	CAN1 - IF1 Message Control Register High	IF1MCTRH1		R/W
$00081E_H$	CAN1 - IF1 Data A1 Low	IF1DTA1L1	IF1DTA11	R/W
$00081F_H$	CAN1 - IF1 Data A1 High	IF1DTA1H1		R/W
000820_H	CAN1 - IF1 Data A2 Low	IF1DTA2L1	IF1DTA21	R/W
000821_H	CAN1 - IF1 Data A2 High	IF1DTA2H1		R/W

Table 5: Interrupt vector table MB96(F)34x

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
60	$30C_H$	ICU4	Yes	60	Input Capture Unit 4
61	308_H	ICU5	Yes	61	Input Capture Unit 5
62	304_H	ICU6	Yes	62	Input Capture Unit 6
63	300_H	ICU7	Yes	63	Input Capture Unit 7
64	$2FC_H$	OCU0	Yes	64	Output Compare Unit 0
65	$2F8_H$	OCU1	Yes	65	Output Compare Unit 1
66	$2F4_H$	OCU2	Yes	66	Output Compare Unit 2
67	$2F0_H$	OCU3	Yes	67	Output Compare Unit 3
68	$2EC_H$	OCU4	Yes	68	Output Compare Unit 4
69	$2E8_H$	OCU5	Yes	69	Output Compare Unit 5
70	$2E4_H$	OCU6	Yes	70	Output Compare Unit 6
71	$2E0_H$	OCU7	Yes	71	Output Compare Unit 7
72	$2DC_H$	FRT0	Yes	72	Free Running Timer 0
73	$2D8_H$	FRT1	Yes	73	Free Running Timer 1
74	$2D4_H$	IIC0	Yes	74	I2C interface
75	$2D0_H$	IIC1	Yes	75	I2C interface
76	$2CC_H$	ADC0	Yes	76	A/D Converter
77	$2C8_H$	ALARM0	No	77	Alarm Comparator 0 (except MB96F345Dyy or MB96F345Fyy)
78	$2C4_H$	ALARM1	No	78	Alarm Comparator 1 (except MB96F345Dyy or MB96F345Fyy)
79	$2C0_H$	LINR0	Yes	79	LIN USART 0 RX
80	$2BC_H$	LINT0	Yes	80	LIN USART 0 TX
81	$2B8_H$	LINR1	Yes	81	LIN USART 1 RX
82	$2B4_H$	LINT1	Yes	82	LIN USART 1 TX
83	$2B0_H$	LINR2	Yes	83	LIN USART 2 RX
84	$2AC_H$	LINT2	Yes	84	LIN USART 2 TX
85	$2A8_H$	LINR3	Yes	85	LIN USART 3 RX
86	$2A4_H$	LINT3	Yes	86	LIN USART 3 TX
87	$2A0_H$	FLASH_A	No	87	Flash memory A (only Flash devices)
88	$29C_H$	FLASH_B	No	88	Flash memory B (only MB96F348T/H/C)
89	298_H	LINR7	Yes	89	LIN USART 7 RX

13. Handling Devices

Special care is required for the following when handling the device:

- Latch-up prevention
- Unused pins handling
- External clock usage
- Unused sub clock signal
- Notes on PLL clock mode operation
- Power supply pins (V_{CC}/V_{SS})
- Crystal oscillator circuit
- Turn on sequence of power supply to A/D converter and analog inputs
- Pin handling when not using the A/D converter
- Notes on energization
- Stabilization of power supply voltage
- Serial communication
- Handling of Data Flash

13.1 Latch-up prevention

CMOS IC chips may suffer latch-up under the following conditions:

- A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V_{CC} pins and V_{SS} pins.
- The AV_{CC} power supply is applied before the V_{CC} voltage.

Latch-up may increase the power supply current dramatically, causing thermal damages to the device.

For the same reason, extra care is required to not let the analog power-supply voltage (AV_{CC}, AVRH) exceed the digital power-supply voltage.

13.2 Unused pins handling

Unused input pins can be left open when the input is disabled (corresponding bit of Port Input Enable register PIER = 0).

Leaving unused input pins open when the input is enabled may result in misbehavior and possible permanent damage of the device. They must therefore be pulled up or pulled down through resistors. To prevent latch-up, those resistors should be more than 2 kΩ.

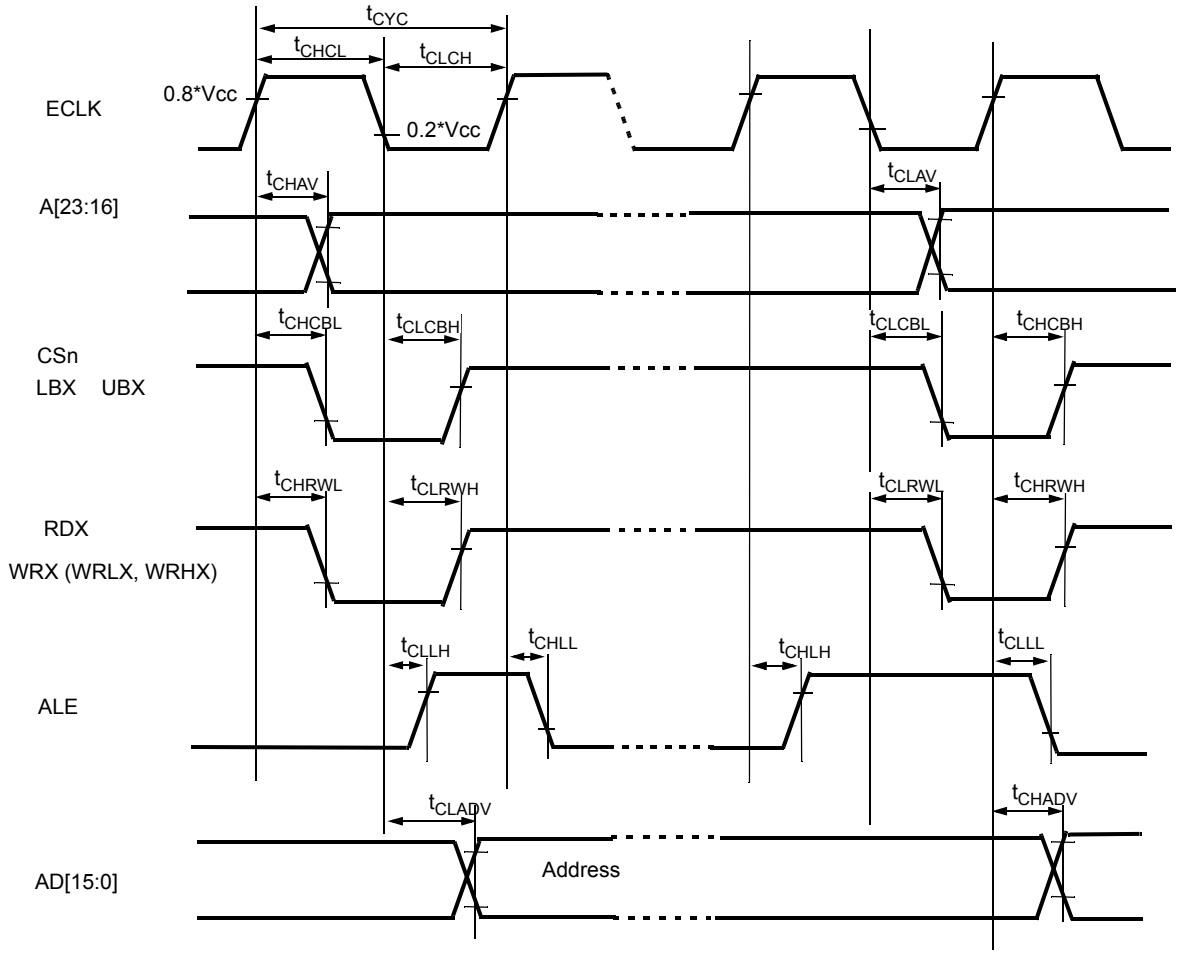
Unused bidirectional pins can be set either to the output state and be then left open, or to the input state with either input disabled or external pull-up/pull-down resistor as described above.

13.3 External clock usage

The permitted frequency range of an external clock depends on the oscillator type and configuration. See AC Characteristics for detailed modes and frequency limits. Single and opposite phase external clocks must be connected as follows:

(T_A = –40°C to +125°C, V_{CC} = 3.0 to 4.5V, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
ECLK	t_{CYC}	ECLK	-	30	-	ns	
	t_{CHCL}			t_{CYC}/2-8	t_{CYC}/2+8		
	t_{CLCH}			t_{CYC}/2-8	t_{CYC}/2+8		
ECLK → UBX/ LBX / CSn time	t_{CHCBH}	CSn, UBX, LBX, ECLK	-	-25	25	ns	
	t_{CHCBL}			-25	25		
	t_{CLCBH}			-25	25		
	t_{CLCBL}			-25	25		
ECLK → ALE time	t_{CHLH}	ALE, ECLK	-	-15	15	ns	
	t_{CHLL}			-15	15		
	t_{CLLH}			-15	15		
	t_{CLLL}			-15	15		
ECLK → address valid time	t_{CHAV}	A[23:16], ECLK	-	-20	20	ns	
	t_{CLAV}			-20	20		
	t_{CLADV}	AD[15:0], ECLK	-	-20	20	ns	
	t_{CHADV}			-20	20		
ECLK → RDX /WRX time	t_{CHRWH}	RDX, WRX, WRLX, WRHX, ECLK	-	-15	15	ns	
	t_{CHRWL}			-15	15		
	t_{CLRWH}			-15	15		
	t_{CLRWL}			-15	15		

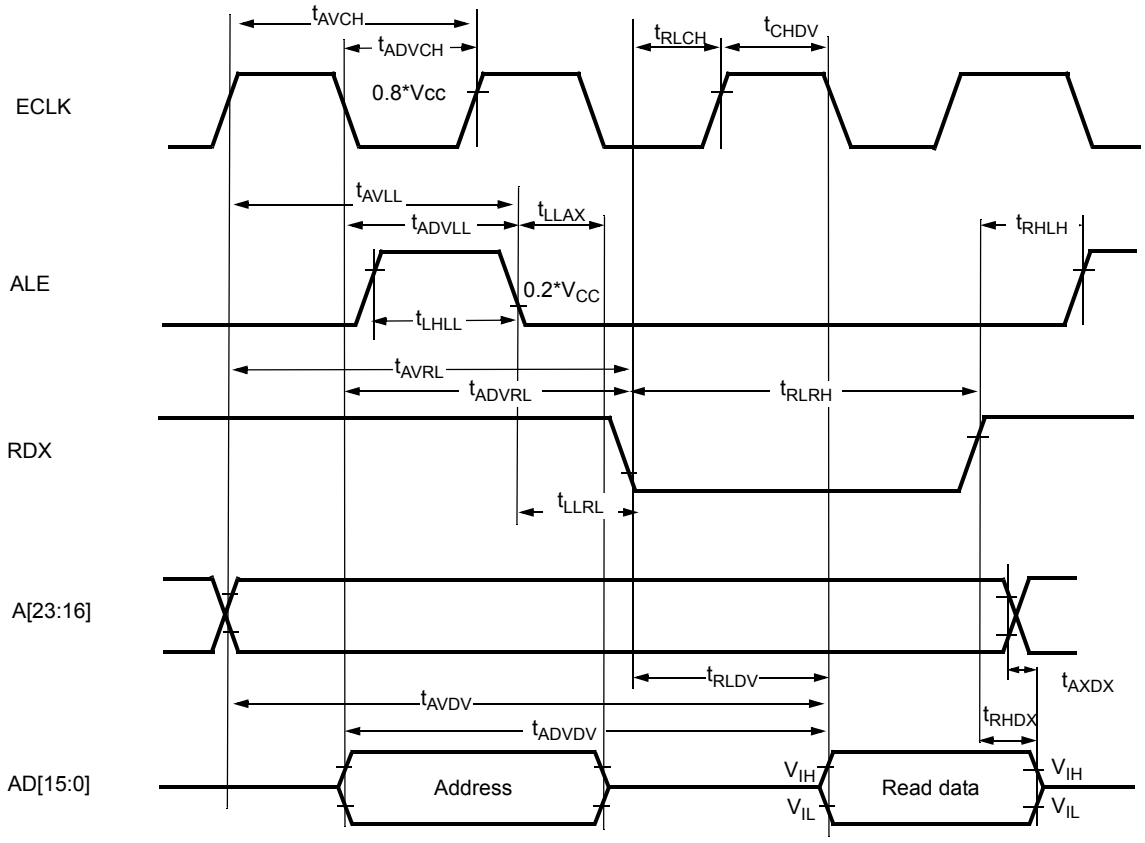


Refer to the Hardware Manual for detailed Timing Charts

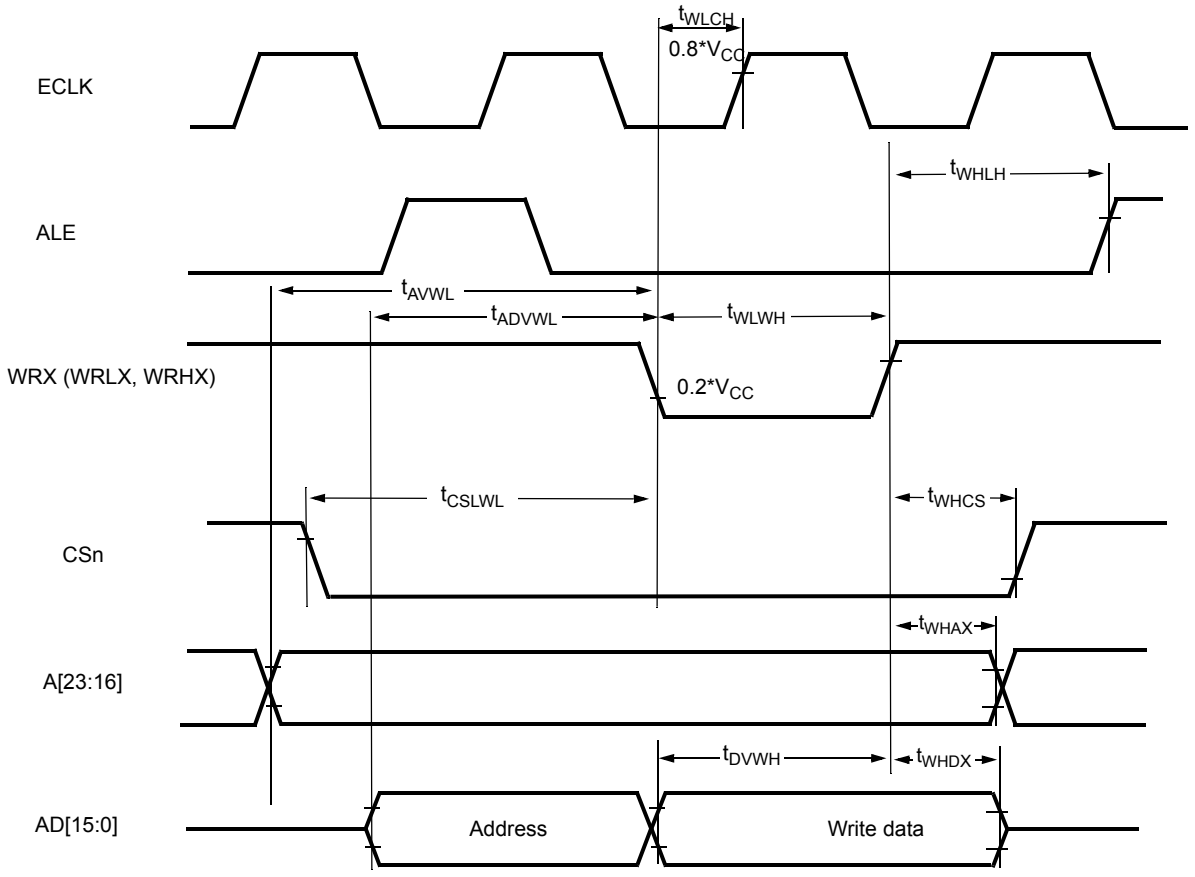
14.4.8 Bus Timing (Read)

(T_A = –40°C to +125°C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
ALE pulse width	t_{LHLL}	ALE	EACL:STS=0 and EACL:ACE=0	$t_{CYC}/2 - 5$	-	ns	
			EACL:STS=1	$t_{CYC} - 5$	-		
			EACL:STS=0 and EACL:ACE=1	$3t_{CYC}/2 - 5$	-		
Valid address ⇒ ALE ↓ time	t_{AVLL}	ALE, A[23:16],	EACL:STS=0 and EACL:ACE=0	$t_{CYC} - 15$	-	ns	
			EACL:STS=1 and EACL:ACE=0	$3t_{CYC}/2 - 15$	-		
			EACL:STS=0 and EACL:ACE=1	$2t_{CYC} - 15$	-		
			EACL:STS=1 and EACL:ACE=1	$5t_{CYC}/2 - 15$	-		
	t_{ADVLL}	ALE,AD[15:0]	EACL:STS=0 and EACL:ACE=0	$t_{CYC}/2 - 15$	-	ns	
			EACL:STS=1 and EACL:ACE=0	$t_{CYC} - 15$	-		
			EACL:STS=0 and EACL:ACE=1	$3t_{CYC}/2 - 15$	-		
			EACL:STS=1 and EACL:ACE=1	$2t_{CYC} - 15$	-		
ALE ↓ ⇒ Address valid time	t_{LLAX}	ALE, AD[15:0]	EACL:STS=0	$t_{CYC}/2 - 15$	-	ns	
			EACL:STS=1	-15	-		
Valid address ⇒ RDX ↓ time	t_{AVRL}	RDX, A[23:16]	EACL:ACE=0	$3t_{CYC}/2 - 15$	-	ns	
			EACL:ACE=1	$5t_{CYC}/2 - 15$	-		
	t_{ADVRL}	RDX, AD[15:0]	EACL:ACE=0	$t_{CYC} - 15$	-	ns	
			EACL:ACE=1	$2t_{CYC} - 15$	-		
Valid address ⇒ Valid data input	t_{AVDV}	A[23:16], AD[15:0]	EACL:ACE=0	-	$3t_{CYC} - 55$	ns	w/o cycle extension
			EACL:ACE=1	-	$4t_{CYC} - 55$		
	t_{ADVDV}	AD[15:0]	EACL:ACE=0	-	$5t_{CYC}/2 - 55$	ns	w/o cycle extension
			EACL:ACE=1	-	$7t_{CYC}/2 - 55$		
RDX pulse width	t_{RLRH}	RDX	-	$3\ t_{CYC}/2 - 5$	-	ns	w/o cycle extension
RDX ↓ ⇒ Valid data input	t_{RLDV}	RDX, AD[15:0]	-	-	$3\ t_{CYC}/2 - 50$	ns	w/o cycle extension
RDX ↑ ⇒ Data hold time	t_{RHDX}	RDX, AD[15:0]	-	0	-	ns	
Address valid ⇒ Data hold time	t_{AXDX}	A[23:16], AD[15:0]	-	0	-	ns	



Refer to the Hardware Manual for detailed Timing Charts



Refer to the Hardware Manual for detailed Timing Charts

14.4.10 Ready Input Timing

(T_A = –40°C to +125°C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Test Condition	Rated Value		Units	Remarks
				Min	Max		
RDY setup time	t_{RYHS}	RDY	-	35	-	ns	
RDY hold time	t_{RYHH}	RDY		0	-	ns	

(T_A = –40°C to +125°C, V_{CC} = 3.0 to 4.5V, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Test Condition	Rated Value		Units	Remarks
				Min	Max		
RDY setup time	t_{RYHS}	RDY	-	45	-	ns	
RDY hold time	t_{RYHH}	RDY		0	-	ns	

Note: If the RDY setup time is insufficient, use the auto-ready function.

14.4.12 USART timing

WARNING: The values given below are for an I/O driving strength IO_{drive} = 5mA. If IO_{drive} is 2mA, all the maximum output timing described in the different tables must then be increased by 10ns.

(T_A = -40°C to 125°C, V_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Condition	V_{CC} = AV_{CC}= 4.5V to 5.5V		V_{CC} = AV_{CC}= 3.0V to 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYCI}	SCKn	Internal Shift Clock Mode	4 t_{CLKP1}	-	4 t_{CLKP1}	-	ns
SCK ↓→ SOT delay time	t_{SLOVI}	SCKn, SOTn		-20	+20	-30	+30	ns
SOT → SCK ↑ delay time	t_{OVSHI}	SCKn, SOTn		N*t_{CLKP1} - 20 [1]	-	N*t_{CLKP1} - 30 [1]	-	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCKn, SINn		t_{CLKP1} + 45	-	t_{CLKP1} + 55	-	ns
SCK ↑→ Valid SIN hold time	t_{SHIXI}	SCKn, SINn		0	-	0	-	ns
Serial clock “L” pulse width	t_{SLSHE}	SCKn	External Shift Clock Mode	t_{CLKP1} + 10	-	t_{CLKP1} + 10	-	ns
Serial clock “H” pulse width	t_{SHSLE}	SCKn		t_{CLKP1} + 10	-	t_{CLKP1} + 10	-	ns
SCK ↓→ SOT delay time	t_{SLOVE}	SCKn, SOTn		-	2 t_{CLKP1} + 45	-	2 t_{CLKP1} + 55	ns
Valid SIN → SCK ↑	t_{IVSHE}	SCKn, SINn		t_{CLKP1}/2 + 10	-	t_{CLKP1}/2 + 10	-	ns
SCK ↑→ Valid SIN hold time	t_{SHIXE}	SCKn, SINn		t_{CLKP1} + 10	-	t_{CLKP1} + 10	-	ns
SCK fall time	t_{FE}	SCKn		-	20	-	20	ns
SCK rise time	t_{RE}	SCKn		-	20	-	20	ns

Notes:

- AC characteristic in CLK synchronized mode.
- C_L is the load capacity value of pins when testing.
- Depending on the used machine clock frequency, the maximum possible baud rate can be limited by some parameters. These parameters are shown in “MB96300 Super series HARDWARE MANUAL”.
- t_{CLKP1} is the cycle time of the peripheral clock 1 (CLKP1), Unit : ns

[1]: Parameter N depends on t_{SCYCI} and can be calculated as follows:

- if t_{SCYCI} = 2*k*t_{CLKP1}, then N = k, where k is an integer > 2
- if t_{SCYCI} = (2*k+1)*t_{CLKP1}, then N = k+1, where k is an integer > 1

Examples:

t_{SCYCI}	N
4*t_{CLKP1}	2
5*t_{CLKP1},	3
7*t_{CLKP1},	4
...	...

14.4.13 I²C Timing

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V,V_{SS} = AV_{SS} =0V)

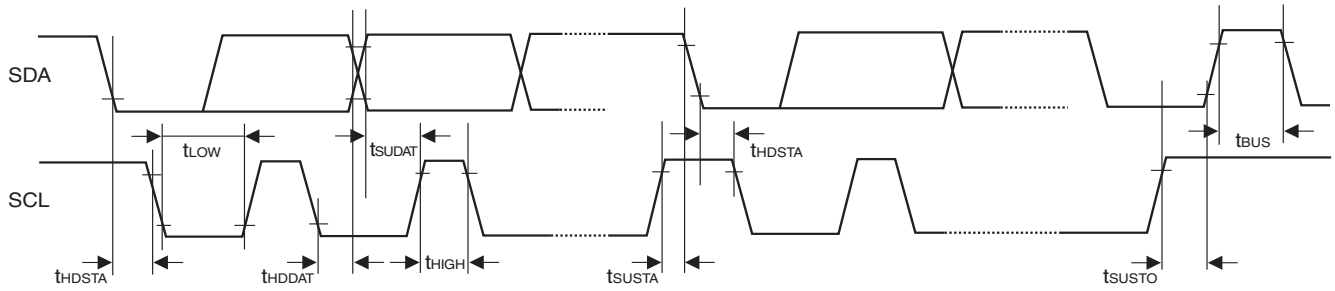
Parameter	Symbol	Condition	Standard-mode		Fast-mode[4]		Unit
			Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	R = 1.7 kΩ, C = 50 pF[1]	0	100	0	400	kHz
Hold time (repeated) START condition SDA↓→SCL¬	t_{HDSTA}		4.0	-	0.6	-	µs
"L" width of the SCL clock	t_{LOW}		4.7	-	1.3	-	µs
"H" width of the SCL clock	t_{HIGH}		4.0	-	0.6	-	µs
Set-up time for a repeated START condition SCL↓→SDA↑	t_{SUSTA}		4.7	-	0.6	-	µs
Data hold timeSCL↑→SDA↑↓	t_{HDDAT}		0	3.45[2]	0	0.9[3]	µs
Data set-up timeSDA↑↓→SCL↑	t_{SUDAT}		250	-	100	-	ns
Set-up time for STOP conditionSCL↑→SDA↑	t_{SUSTO}		4.0	-	0.6	-	µs
Bus free time between a STOP and START condition	t_{BUS}		4.7	-	1.3	-	µs

[1] : R,C: Pull-up resistor and load capacitor of the SCL and SDA lines.

[2]: The maximum t_{HDDAT} have only to be met if the device does not stretch the "L" width (t_{LOW}) of the SCL signal.

[3] : A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement t_{SUDAT}≥ 250 ns must then be met.

[4] : For use at over 100 kHz, set the peripheral clock 1 to at least 6 MHz.



14.5 Analog Digital Converter

(T_A = -40 °C to +125 °C, 3.0 V ≤ AVRH - AVRL, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	10	bit	
Total error	-	-	-3	-	+3	LSB	
Nonlinearity error	-	-	-2.5	-	+2.5	LSB	
Differential nonlinearity error	-	-	-1.9	-	+1.9	LSB	
Zero reading voltage	V_{OT}	ANn	AVRL - 1.5 LSB	AVRL+ 0.5 LSB	AVRL + 2.5 LSB	V	
Full scale reading voltage	V_{FST}	ANn	AVRH - 3.5 LSB	AVRH - 1.5 LSB	AVRH + 0.5 LSB	V	
Compare time	-	-	1.0	-	16,500	µs	4.5V ≤ AV_{CC} ≤ 5.5V
			2.0	-	-	µs	3.0V ≤ AV_{CC} < 4.5V
Sampling time	-	-	0.5	-	-	µs	4.5V ≤ AV_{CC} ≤ 5.5V
			1.2	-	-	µs	3.0V ≤ AV_{CC} < 4.5V
Analog port input curren	I_{AIN}	ANn	-3	-	+3	µA	AV_{SS}, AVRL < V_I < AV_{CC}, AVRH
Analog port input curren	I_{AIN}	ANn	-1	-	+1	µA	T_A = 25 °C, AV_{SS}, AVRL < V_I < AV_{CC}, AVRH
			-3	-	+3	µA	T_A = 125 °C,AV_{SS}, AVRL < V_I < AV_{CC}, AVRH
Analog input voltage range	V_{AIN}	ANn	AVRL	-	AVRH	V	
Reference voltage range	AVRH	AVRH/ AVRH 2	0.75 AVcc	-	AVcc	V	
	AVRL	AVRL	AV_{SS}	-	0.25 AV_{CC}	V	
Power supply current	I_A	AVcc	-	2.5	5	mA	A/D Converter active
	I_{AH}	AVcc	-	-	5	µA	A/D Converter not operated
Reference voltage current	I_R	AVRH/ AVRL	-	0.7	1	mA	A/D Converter active
	I_{RH}	AVRH/ AVRL	-	-	5	µA	A/D Converter not operated
Offset between input channels	-	ANn	-	-	4	LSB	

Note: The accuracy gets worse as |AVRH - AVRL| becomes smaller.

Table 6: Used settings

Mode	Selected Source Clock	Clock/Regulator Settings
Run mode	PLL	CLKS1 = CLKS2 = CLKB = CLKP1 = 56 MHz CLKP2 = 28 MHz Regulator in High Power Mode Core Voltage = 1.9 V
	Main osc.	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 4 MHz Regulator in High Power Mode Core Voltage = 1.8 V
	RC clock fast	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 2 MHz Regulator in High Power Mode Core Voltage = 1.8 V
	RC clock slow	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 100 kHz Regulator in High Power Mode Core Voltage = 1.8 V
	Sub osc.	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 32 kHz Regulator in Low Power Mode A Core Voltage = 1.8 V
Sleep mode	PLL	CLKS1 = CLKS2 = CLKP1 = 56 MHz CLKP2 = 28 MHz (CLKB is stopped in this mode) Regulator in High Power Mode Core Voltage = 1.9 V
	Main osc.	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 4 MHz (CLKB is stopped in this mode) Regulator in High Power Mode Core Voltage = 1.8 V
	RC clock fast	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 2 MHz (CLKB is stopped in this mode) Regulator in High Power Mode Core Voltage = 1.8 V
	RC clock slow	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 100 kHz (CLKB is stopped in this mode) Regulator in High Power Mode Core Voltage = 1.8 V
	Sub osc.	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 32 kHz (CLKB is stopped in this mode) Regulator in Low Power Mode A Core Voltage = 1.8 V

19. Revision History

Revision	Date	Modification
Prelim 1	2007-05-07	Creation
Prelim 2	2007-05-10	External bus hold timing update
Prelim 3	2007-05-23	Electrical characteristics updates
Prelim 4	2007-08-02	Electrical characteristics updates, Product lineup, changes and ordering information
Prelim 5	2007-09-12	Addition of the electrical characteristic examples and the LVD characteristics specifications, updates of the DC characteristics. Pin circuit type drawing modifications.
Prelim 6	2007-11-21	LVD typo correction. Update of the DC characteristics. Typos corrections.
Prelim 7	2007-12-04	Absolute maximum rating asterisks numbering corrected. Typos page 59: Hardware -> Hardware. IO map table regenerated. Typos corrections. IO circuit drawings modified. Renaming of the Main/Satellite Flash into Flash memory A/B. Memory map reworked.
Prelim 8	2008-02-04	■ Satellite Flash -> 32kB Data Flash ■ MB96345 added (under development) ■ MB96F348 TSA/HSA/TWA/HWA removed (outdated devices) ■ Block diagram and pin assignment corrected (existing resource pins) ■ Pin function table corrected ■ I/O circuit type diagrams corrected ■ Memory map cleaned up ■ "Flash sector configuration" replaced by corrected "User ROM Memory map for Flash devices", “ROM configuration” replaced by “User ROM Memory map for Mask ROM devices” ■ Parallel Flash programming pinning removed ■ IO map table regenerated: ❒ Port register: Naming style corrected ❒ Memory control registers renamed (Main/Sat -> A/B) ❒ addresses after 000BFFh removed ■ Absolute maximum ratings: Pd and Ta specified more precisely ■ oscillator input levels in oscillation mode with external clock added ■ Run and Sleep mode currents: 96/48MHz and 72/36MHz settings added ■ Run mode current spec in 48/24MHz mode corrected ■ Maximum CLKS1/2 frequency for all devices correctly specified ■ Maximum CLKP2 for MB96F34xY/R/Axx corrected ■ External bus timings: missing conditions added and readability improved ■ Alarm comparator spec updated (transition voltages defined) ■ MB96V300A removed ■ Ordering information updated ■ Typos and formatting corrected

Revision	Date	Modification
9	2009-01-09	■ Format adjusted to official Cypress datasheet standard (mainly style changes and official notes and disclaimer added) ■ Numbering of Electrical Characteristics subchapters automated ■ Note about devices under development modified ■ I/O map: Note added about reserved addresses ■ ICCSPLL for CLKS1=96MHz mode: increased by 1mA ■ Serial programming interface: Note about handshaking pins improved ■ specified AD converter channel offset to 4LSB ■ package code of MB96V300 corrected in ordering information ■ Added voltage condition to pull-up resistance spec ■ Lineup: Term “Data Flash” replaced by “independent 32KB Flash” ■ Ordering information: column “Independent 32KB Data Flash” replaced by new column “Flash/ROM”, column “Remarks” removed ■ Official package dimension drawing with additional notes added ■ Empty pages removed ■ Alarm comparator: Power supply current max values increased, comparison time reduced, mode transition time and power-up stabilization time newly added ■ Handling devices: Notes added about Serial communication and about using ceramic resonators. ■ Feature list and AC Characteristics: 16MHz maximum frequency is valid for crystal oscillators. For resonators, maximum frequency depends on Q-factor ■ AC characteristics: PLL phase skew spec added, CLKVCO min=64MHz ■ VOL3 spec improved: spec valid for 3mA load for full Vcc range ■ MB96F345 added ■ Preliminary DC spec of MB96345/346 added ■ Permitted power dissipation of Flash devices in QFP package improved ■ C-Pin cap spec updated: 4.7uF-10uF capacitor with tolerance permitted ■ “Preliminary” watermark removed
10	To be released	■ I/O map: IOABK0-5 added at address 000A00H-000A05H ■ Ordering Information: Suffix “A” added to all MB96F345 device versions ■ AD converter I_{AIN} spec improved: 1uA valid up to 105deg, 1.2uA above 105deg