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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

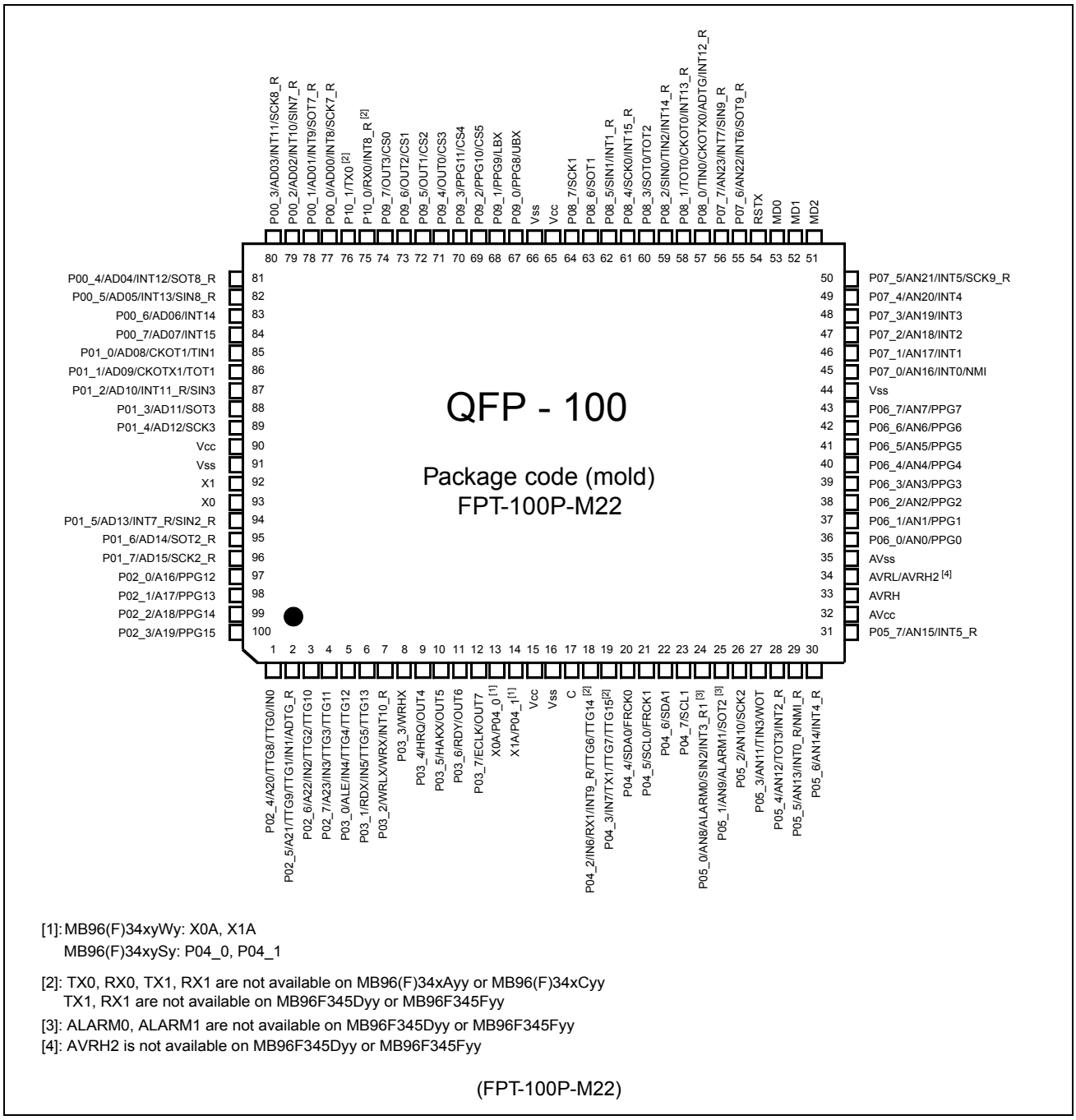
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	56MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, LVR, POR, PWM, WDT
Number of I/O	82
Program Memory Size	416KB (416K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-PQFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f347rsbpqc-gs-ere2

Contents

3. Pin Assignments

Figure 2. Pin assignment of MB96(F)34x (FPT-100P-M22)



[1]: MB96(F)34xyWy: X0A, X1A
MB96(F)34xySy: P04_0, P04_1

[2]: TX0, RX0, TX1, RX1 are not available on MB96(F)34xAyy or MB96(F)34xCyy
TX1, RX1 are not available on MB96F345Dyy or MB96F345Fyy

[3]: ALARM0, ALARM1 are not available on MB96F345Dyy or MB96F345Fyy

[4]: AVRH2 is not available on MB96F345Dyy or MB96F345Fyy

(FPT-100P-M22)

Remark:

MB96(F)34x products are pin-compatible to F^{2}MC-16LX family MB90340 series.

Table 1: Pin Function description

Pin name	Feature	Description
RDY	External bus	External bus interface external wait state request input
RSTX	Core	Reset input
RXn	CAN	CAN interface n RX input
SCKn	USART	USART n serial clock input/output
SCKn_R	USART	Relocated USART n serial clock input/output
SCLn	I2C	I^2C interface n clock I/O input/output
SDAn	I2C	I^2C interface n serial data I/O input/output
SINn	USART	USART n serial data input
SINn_R	USART	Relocated USART n serial data input
SOTn	USART	USART n serial data output
SOTn_R	USART	Relocated USART n serial data output
TINn	Reload Timer	Reload Timer n event input
TOTn	Reload Timer	Reload Timer n output
TTGn	PPG	Programmable Pulse Generator n trigger input
TXn	CAN	CAN interface n TX output
UBX	External bus	External Bus Interface Upper Byte select strobe output
V_{CC}	Supply	Power supply
V_{SS}	Supply	Power supply
WOT	RTC	Real Timer clock output
WRHX	External bus	External bus High byte write strobe output
WRLX/WRX	External bus	External bus Low byte / Word write strobe output
X0	Clock	Oscillator input
X0A	Clock	Subclock Oscillator input (only for devices with suffix "W")
X1	Clock	Oscillator output
X1A	Clock	Subclock Oscillator output (only for devices with suffix "W")

8. User ROM Memory Map For Flash Devices

MB96F345D
MB96F345F

Alternative mode CPU address	Flash memory mode address	Flash size 160kByte +64KByte Data Flash	
$FF:FFFF_H$ $FF:0000_H$	$3F:FFFF_H$ $3F:0000_H$	S39 - 64K	Flash A
$FE:FFFF_H$ $FE:0000_H$	$3E:FFFF_H$ $3E:0000_H$	S38 - 64K	
$FD:FFFF_H$ $FD:0000_H$	$3D:FFFF_H$ $3D:0000_H$	External bus	
$FC:FFFF_H$ $FC:0000_H$	$3C:FFFF_H$ $3C:0000_H$		
$FB:FFFF_H$ $FB:0000_H$	$3B:FFFF_H$ $3B:0000_H$		
$FA:FFFF_H$ $FA:0000_H$	$3A:FFFF_H$ $3A:0000_H$		
$F9:FFFF_H$ $F9:0000_H$	$39:FFFF_H$ $39:0000_H$		
$F8:FFFF_H$ $F8:0000_H$	$38:FFFF_H$ $38:0000_H$		
$F7:FFFF_H$ $F7:0000_H$	$37:FFFF_H$ $37:0000_H$		
$F6:FFFF_H$ $F6:0000_H$	$36:FFFF_H$ $36:0000_H$		
$F5:FFFF_H$ $F5:0000_H$	$35:FFFF_H$ $35:0000_H$		
$F4:FFFF_H$ $F4:0000_H$	$34:FFFF_H$ $34:0000_H$		
$F3:FFFF_H$ $F3:0000_H$	$33:FFFF_H$ $33:0000_H$		
$F2:FFFF_H$ $F2:0000_H$	$32:FFFF_H$ $32:0000_H$		
$F1:FFFF_H$ $F1:0000_H$	$31:FFFF_H$ $31:0000_H$		
$F0:FFFF_H$ $F0:0000_H$	$30:FFFF_H$ $30:0000_H$		
$E0:FFFF_H$ $E0:0000_H$			
$DF:FFFF_H$ $DF:8000_H$		Reserved	
$DF:7FFF_H$ $DF:6000_H$	$1F:7FFF_H$ $1F:6000_H$	SA3 - 8K	Flash A
$DF:5FFF_H$ $DF:4000_H$	$1F:5FFF_H$ $1F:4000_H$	SA2 - 8K	
$DF:3FFF_H$ $DF:2000_H$	$1F:3FFF_H$ $1F:2000_H$	SA1 - 8K	
$DF:1FFF_H$ $DF:0000_H$	$1F:1FFF_H$ $1F:0000_H$	SA0 - 8K [1]	
$DE:FFFF_H$ $DE:0000_H$		Reserved	
$0E:FFFF_H$ $0E:FF00_H$	$(0E:FFFF_H)$ $(0E:FF00_H)$	SDA0-256 [2]	Data Flash A
$0E:FEFF_H$ $0E:0000_H$		Reserved	
$0D:FFFF_H$ $0D:C000_H$	$(0F:FFFF_H)$ $(0F:C000_H)$	SDA4-16K	Data Flash A
$0D:BFFF_H$ $0D:8000_H$	$(0F:BFFF_H)$ $(0F:8000_H)$	SDA3-16K	
$0D:7FFF_H$ $0D:4000_H$	$(0F:7FFF_H)$ $(0F:4000_H)$	SDA2-16K	
$0D:3FFF_H$ $0D:0000_H$	$(0F:3FFF_H)$ $(0F:0000_H)$	SDA1-16K	
$0C:FFFF_H$ $0C:0000_H$		Reserved	

[1]: Sector SA0 contains the ROM Configuration Block RCBA at CPU address $DF:0000_H$ - $DF:007F_H$

[2]: Sector SDA0 contains the ROM Configuration Block RCBDA at CPU address $DE:FF00_H$ - $DE:FF2F_H$

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$0000C1_H$	USART0 - Serial Control Register	SCR0		R/W
$0000C2_H$	USART0 - TX Register	TDR0		W
$0000C2_H$	USART0 - RX Register	RDR0		R
$0000C3_H$	USART0 - Serial Status	SSR0		R/W
$0000C4_H$	USART0 - Control/Com. Register	ECCR0		R/W
$0000C5_H$	USART0 - Ext. Status Register	ESCR0		R/W
$0000C6_H$	USART0 - Baud Rate Generator Register Low	BGRL0	BGR0	R/W
$0000C7_H$	USART0 - Baud Rate Generator Register High	BGRH0		R/W
$0000C8_H$	USART0 - Extended Serial Interrupt Register	ESIR0		R/W
$0000C9_H$	Reserved			-
$0000CA_H$	USART1 - Serial Mode Register	SMR1		R/W
$0000CB_H$	USART1 - Serial Control Register	SCR1		R/W
$0000CC_H$	USART1 - TX Register	TDR1		W
$0000CC_H$	USART1 - RX Register	RDR1		R
$0000CD_H$	USART1 - Serial Status	SSR1		R/W
$0000CE_H$	USART1 - Control/Com. Register	ECCR1		R/W
$0000CF_H$	USART1 - Ext. Status Register	ESCR1		R/W
$0000D0_H$	USART1 - Baud Rate Generator Register Low	BGRL1	BGR1	R/W
$0000D1_H$	USART1 - Baud Rate Generator Register High	BGRH1		R/W
$0000D2_H$	USART1 - Extended Serial Interrupt Register	ESIR1		R/W
$0000D3_H$	Reserved			-
$0000D4_H$	USART2 - Serial Mode Register	SMR2		R/W
$0000D5_H$	USART2 - Serial Control Register	SCR2		R/W
$0000D6_H$	USART2 - TX Register	TDR2		W
$0000D6_H$	USART2 - RX Register	RDR2		R
$0000D7_H$	USART2 - Serial Status	SSR2		R/W
$0000D8_H$	USART2 - Control/Com. Register	ECCR2		R/W
$0000D9_H$	USART2 - Ext. Status Register	ESCR2		R/W
$0000DA_H$	USART2 - Baud Rate Generator Register Low	BGRL2	BGR2	R/W
$0000DB_H$	USART2 - Baud Rate Generator Register High	BGRH2		R/W
$0000DC_H$	USART2 - Extended Serial Interrupt Register	ESIR2		R/W
$0000DD_H$	Reserved			-

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$0003B9_H$	Memory Patch function - Patch address 0 middle	PFAM0		R/W
$0003BA_H$	Memory Patch function - Patch address 0 high	PFAH0		R/W
$0003BB_H$	Memory Patch function - Patch address 1 low	PFAL1		R/W
$0003BC_H$	Memory Patch function - Patch address 1 middle	PFAM1		R/W
$0003BD_H$	Memory Patch function - Patch address 1 high	PFAH1		R/W
$0003BE_H$	Memory Patch function - Patch address 2 low	PFAL2		R/W
$0003BF_H$	Memory Patch function - Patch address 2 middle	PFAM2		R/W
$0003C0_H$	Memory Patch function - Patch address 2 high	PFAH2		R/W
$0003C1_H$	Memory Patch function - Patch address 3 low	PFAL3		R/W
$0003C2_H$	Memory Patch function - Patch address 3 middle	PFAM3		R/W
$0003C3_H$	Memory Patch function - Patch address 3 high	PFAH3		R/W
$0003C4_H$	Memory Patch function - Patch address 4 low	PFAL4		R/W
$0003C5_H$	Memory Patch function - Patch address 4 middle	PFAM4		R/W
$0003C6_H$	Memory Patch function - Patch address 4 high	PFAH4		R/W
$0003C7_H$	Memory Patch function - Patch address 5 low	PFAL5		R/W
$0003C8_H$	Memory Patch function - Patch address 5 middle	PFAM5		R/W
$0003C9_H$	Memory Patch function - Patch address 5 high	PFAH5		R/W
$0003CA_H$	Memory Patch function - Patch address 6 low	PFAL6		R/W
$0003CB_H$	Memory Patch function - Patch address 6 middle	PFAM6		R/W
$0003CC_H$	Memory Patch function - Patch address 6 high	PFAH6		R/W
$0003CD_H$	Memory Patch function - Patch address 7 low	PFAL7		R/W
$0003CE_H$	Memory Patch function - Patch address 7 middle	PFAM7		R/W
$0003CF_H$	Memory Patch function - Patch address 7 high	PFAH7		R/W
$0003D0_H$	Memory Patch function - Patch data 0 Low	PFDL0	PFD0	R/W
$0003D1_H$	Memory Patch function - Patch data 0 High	PFDH0		R/W
$0003D2_H$	Memory Patch function - Patch data 1 Low	PFDL1	PFD1	R/W
$0003D3_H$	Memory Patch function - Patch data 1 High	PFDH1		R/W
$0003D4_H$	Memory Patch function - Patch data 2 Low	PFDL2	PFD2	R/W
$0003D5_H$	Memory Patch function - Patch data 2 High	PFDH2		R/W
$0003D6_H$	Memory Patch function - Patch data 3 Low	PFDL3	PFD3	R/W
$0003D7_H$	Memory Patch function - Patch data 3 High	PFDH3		R/W
$0003D8_H$	Memory Patch function - Patch data 4 Low	PFDL4	PFD4	R/W

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$0004B3_H$-$0004BB_H$	Reserved			-
$0004BC_H$	I/O Port P00 - External Pin State Register	EPSR00		R
$0004BD_H$	I/O Port P01 - External Pin State Register	EPSR01		R
$0004BE_H$	I/O Port P02 - External Pin State Register	EPSR02		R
$0004BF_H$	I/O Port P03 - External Pin State Register	EPSR03		R
$0004C0_H$	I/O Port P04 - External Pin State Register	EPSR04		R
$0004C1_H$	I/O Port P05 - External Pin State Register	EPSR05		R
$0004C2_H$	I/O Port P06 - External Pin State Register	EPSR06		R
$0004C3_H$	I/O Port P07 - External Pin State Register	EPSR07		R
$0004C4_H$	I/O Port P08 - External Pin State Register	EPSR08		R
$0004C5_H$	I/O Port P09 - External Pin State Register	EPSR09		R
$0004C6_H$	I/O Port P10 - External Pin State Register	EPSR10		R
$0004C7_H$-$0004CF_H$	Reserved			-
$0004D0_H$	ADC analog input enable register 0	ADER0		R/W
$0004D1_H$	ADC analog input enable register 1	ADER1		R/W
$0004D2_H$	ADC analog input enable register 2	ADER2		R/W
$0004D3_H$	ADC analog input enable register 3	ADER3		R/W
$0004D4_H$	ADC analog input enable register 4	ADER4		R/W
$0004D5_H$	Reserved			-
$0004D6_H$	Peripheral Resource Relocation Register 0	PRRR0		R/W
$0004D7_H$	Peripheral Resource Relocation Register 1	PRRR1		R/W
$0004D8_H$	Peripheral Resource Relocation Register 2	PRRR2		R/W
$0004D9_H$	Peripheral Resource Relocation Register 3	PRRR3		R/W
$0004DA_H$	Peripheral Resource Relocation Register 4	PRRR4		R/W
$0004DB_H$	Peripheral Resource Relocation Register 5	PRRR5		R/W
$0004DC_H$	Peripheral Resource Relocation Register 6	PRRR6		R/W
$0004DD_H$	Peripheral Resource Relocation Register 7	PRRR7		R/W
$0004DE_H$	Peripheral Resource Relocation Register 8	PRRR8		R/W
$0004DF_H$	Peripheral Resource Relocation Register 9	PRRR9		R/W
$0004E0_H$	RTC - Sub Second Register L	WTBRL0	WTBR0	R/W
$0004E1_H$	RTC - Sub Second Register M	WTBRH0		R/W
$0004E2_H$	RTC - Sub-Second Register H	WTBR1		R/W

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$00056D_H$	PPG7 - Timer register			R
$00056E_H$	PPG7 - Period setting register		PCSR7	W
$00056F_H$	PPG7 - Period setting register			W
000570_H	PPG7 - Duty cycle register		PDUT7	W
000571_H	PPG7 - Duty cycle register			W
000572_H	PPG7 - Control status register Low	PCNL7	PCN7	R/W
000573_H	PPG7 - Control status register High	PCNH7		R/W
000574_H	PPG11-PPG8 - General Control register 1 Low	GCN1L2	GCN12	R/W
000575_H	PPG11-PPG8 - General Control register 1 High	GCN1H2		R/W
000576_H	PPG11-PPG8 - General Control register 2 Low	GCN2L2	GCN22	R/W
000577_H	PPG11-PPG8 - General Control register 2 High	GCN2H2		R/W
000578_H	PPG8 - Timer register		PTMR8	R
000579_H	PPG8 - Timer register			R
$00057A_H$	PPG8 - Period setting register		PCSR8	W
$00057B_H$	PPG8 - Period setting register			W
$00057C_H$	PPG8 - Duty cycle register		PDUT8	W
$00057D_H$	PPG8 - Duty cycle register			W
$00057E_H$	PPG8 - Control status register Low	PCNL8	PCN8	R/W
$00057F_H$	PPG8 - Control status register High	PCNH8		R/W
000580_H	PPG9 - Timer register		PTMR9	R
000581_H	PPG9 - Timer register			R
000582_H	PPG9 - Period setting register		PCSR9	W
000583_H	PPG9 - Period setting register			W
000584_H	PPG9 - Duty cycle register		PDUT9	W
000585_H	PPG9 - Duty cycle register			W
000586_H	PPG9 - Control status register Low	PCNL9	PCN9	R/W
000587_H	PPG9 - Control status register High	PCNH9		R/W
000588_H	PPG10 - Timer register		PTMR10	R
000589_H	PPG10 - Timer register			R
$00058A_H$	PPG10 - Period setting register		PCSR10	W
$00058B_H$	PPG10 - Period setting register			W
$00058C_H$	PPG10 - Duty cycle register		PDUT10	W

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$0005AD_H$	PPG14 - Timer register			R
$0005AE_H$	PPG14 - Period setting register		PCSR14	W
$0005AF_H$	PPG14 - Period setting register			W
$0005B0_H$	PPG14 - Duty cycle register		PDUT14	W
$0005B1_H$	PPG14 - Duty cycle register			W
$0005B2_H$	PPG14 - Control status register Low	PCNL14	PCN14	R/W
$0005B3_H$	PPG14 - Control status register High	PCNH14		R/W
$0005B4_H$	PPG15 - Timer register		PTMR15	R
$0005B5_H$	PPG15 - Timer register			R
$0005B6_H$	PPG15 - Period setting register		PCSR15	W
$0005B7_H$	PPG15 - Period setting register			W
$0005B8_H$	PPG15 - Duty cycle register		PDUT15	W
$0005B9_H$	PPG15 - Duty cycle register			W
$0005BA_H$	PPG15 - Control status register Low	PCNL15	PCN15	R/W
$0005BB_H$	PPG15 - Control status register High	PCNH15		R/W
$0005BC_H$-$00065F_H$	Reserved			-
000660_H	Peripheral Resource Relocation Register 10	PRRR10		R/W
000661_H	Peripheral Resource Relocation Register 11	PRRR11		R/W
000662_H	Peripheral Resource Relocation Register 12	PRRR12		R/W
000663_H	Peripheral Resource Relocation Register 13	PRRR13		W
000664_H-$0006DF_H$	Reserved			-
$0006E0_H$	External Bus - Area configuration register 0 Low	EACL0	EAC0	R/W
$0006E1_H$	External Bus - Area configuration register 0 High	EACH0		R/W
$0006E2_H$	External Bus - Area configuration register 1 Low	EACL1	EAC1	R/W
$0006E3_H$	External Bus - Area configuration register 1 High	EACH1		R/W
$0006E4_H$	External Bus - Area configuration register 2 Low	EACL2	EAC2	R/W
$0006E5_H$	External Bus - Area configuration register 2 High	EACH2		R/W
$0006E6_H$	External Bus - Area configuration register 3 Low	EACL3	EAC3	R/W
$0006E7_H$	External Bus - Area configuration register 3 High	EACH3		R/W
$0006E8_H$	External Bus - Area configuration register 4 Low	EACL4	EAC4	R/W
$0006E9_H$	External Bus - Area configuration register 4 High	EACH4		R/W
$0006EA_H$	External Bus - Area configuration register 5 Low	EACL5	EAC5	R/W

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000801_H	CAN1 - Control register High (reserved)	CTRLRH1		R
000802_H	CAN1 - Status register Low	STATRL1	STATR1	R/W
000803_H	CAN1 - Status register High (reserved)	STATRH1		R
000804_H	CAN1 - Error Counter Low (Transmit)	ERRCNTL1	ERRCNT1	R
000805_H	CAN1 - Error Counter High (Receive)	ERRCNTH1		R
000806_H	CAN1 - Bit Timing Register Low	BTRL1	BTR1	R/W
000807_H	CAN1 - Bit Timing Register High	BTRH1		R/W
000808_H	CAN1 - Interrupt Register Low	INTRL1	INTR1	R
000809_H	CAN1 - Interrupt Register High	INTRH1		R
$00080A_H$	CAN1 - Test Register Low	TESTRL1	TESTR1	R/W
$00080B_H$	CAN1 - Test Register High (reserved)	TESTRH1		R
$00080C_H$	CAN1 - BRP Extension register Low	BRPERL1	BRPER1	R/W
$00080D_H$	CAN1 - BRP Extension register High (reserved)	BRPERH1		R
$00080E_H$-$00080F_H$	Reserved			-
000810_H	CAN1 - IF1 Command request register Low	IF1CREQL1	IF1CREQ1	R/W
000811_H	CAN1 - IF1 Command request register High	IF1CREQH1		R/W
000812_H	CAN1 - IF1 Command Mask register Low	IF1CMSKL1	IF1CMSK1	R/W
000813_H	CAN1 - IF1 Command Mask register High (reserved)	IF1CMSKH1		R
000814_H	CAN1 - IF1 Mask 1 Register Low	IF1MSK1L1	IF1MSK11	R/W
000815_H	CAN1 - IF1 Mask 1 Register High	IF1MSK1H1		R/W
000816_H	CAN1 - IF1 Mask 2 Register Low	IF1MSK2L1	IF1MSK21	R/W
000817_H	CAN1 - IF1 Mask 2 Register High	IF1MSK2H1		R/W
000818_H	CAN1 - IF1 Arbitration 1 Register Low	IF1ARB1L1	IF1ARB11	R/W
000819_H	CAN1 - IF1 Arbitration 1 Register High	IF1ARB1H1		R/W
$00081A_H$	CAN1 - IF1 Arbitration 2 Register Low	IF1ARB2L1	IF1ARB21	R/W
$00081B_H$	CAN1 - IF1 Arbitration 2 Register High	IF1ARB2H1		R/W
$00081C_H$	CAN1 - IF1 Message Control Register Low	IF1MCTRL1	IF1MCTR1	R/W
$00081D_H$	CAN1 - IF1 Message Control Register High	IF1MCTRH1		R/W
$00081E_H$	CAN1 - IF1 Data A1 Low	IF1DTA1L1	IF1DTA11	R/W
$00081F_H$	CAN1 - IF1 Data A1 High	IF1DTA1H1		R/W
000820_H	CAN1 - IF1 Data A2 Low	IF1DTA2L1	IF1DTA21	R/W
000821_H	CAN1 - IF1 Data A2 High	IF1DTA2H1		R/W

Table 5: Interrupt vector table MB96(F)34x

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
60	$30C_H$	ICU4	Yes	60	Input Capture Unit 4
61	308_H	ICU5	Yes	61	Input Capture Unit 5
62	304_H	ICU6	Yes	62	Input Capture Unit 6
63	300_H	ICU7	Yes	63	Input Capture Unit 7
64	$2FC_H$	OCU0	Yes	64	Output Compare Unit 0
65	$2F8_H$	OCU1	Yes	65	Output Compare Unit 1
66	$2F4_H$	OCU2	Yes	66	Output Compare Unit 2
67	$2F0_H$	OCU3	Yes	67	Output Compare Unit 3
68	$2EC_H$	OCU4	Yes	68	Output Compare Unit 4
69	$2E8_H$	OCU5	Yes	69	Output Compare Unit 5
70	$2E4_H$	OCU6	Yes	70	Output Compare Unit 6
71	$2E0_H$	OCU7	Yes	71	Output Compare Unit 7
72	$2DC_H$	FRT0	Yes	72	Free Running Timer 0
73	$2D8_H$	FRT1	Yes	73	Free Running Timer 1
74	$2D4_H$	IIC0	Yes	74	I2C interface
75	$2D0_H$	IIC1	Yes	75	I2C interface
76	$2CC_H$	ADC0	Yes	76	A/D Converter
77	$2C8_H$	ALARM0	No	77	Alarm Comparator 0 (except MB96F345Dyy or MB96F345Fyy)
78	$2C4_H$	ALARM1	No	78	Alarm Comparator 1 (except MB96F345Dyy or MB96F345Fyy)
79	$2C0_H$	LINR0	Yes	79	LIN USART 0 RX
80	$2BC_H$	LINT0	Yes	80	LIN USART 0 TX
81	$2B8_H$	LINR1	Yes	81	LIN USART 1 RX
82	$2B4_H$	LINT1	Yes	82	LIN USART 1 TX
83	$2B0_H$	LINR2	Yes	83	LIN USART 2 RX
84	$2AC_H$	LINT2	Yes	84	LIN USART 2 TX
85	$2A8_H$	LINR3	Yes	85	LIN USART 3 RX
86	$2A4_H$	LINT3	Yes	86	LIN USART 3 TX
87	$2A0_H$	FLASH_A	No	87	Flash memory A (only Flash devices)
88	$29C_H$	FLASH_B	No	88	Flash memory B (only MB96F348T/H/C)
89	298_H	LINR7	Yes	89	LIN USART 7 RX

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Permitted Power dissipation (Mask ROM devices) [4]	P_D	-	350	mW	T_A=105°C
		-	360	mW	T_A=125°C [6]
Operating ambient temperature	T_A	0	+70	°C	MB96V300B
		-40	+105		
		-40	+125		[6]
Storage temperature	T_{STG}	-55	+150	°C	

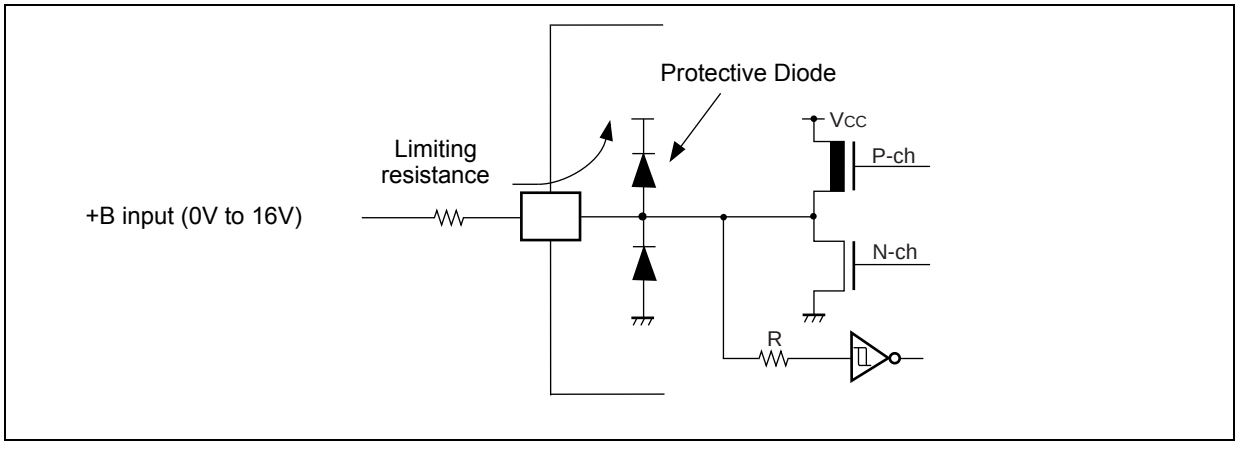
[1]: AV_{CC} and V_{CC} must be set to the same voltage. It is required that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} neither when the power is switched on.

[2]: V_I and V_O should not exceed V_{CC} + 0.3 V. V_I should also not exceed the specified ratings. However if the maximum current to/from a input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating. Input/output voltages of standard ports depend on V_{CC}.

[3]:

- Applicable to all general purpose I/O pins (Pnn_m)
- Use within recommended operating conditions.
- Use at DC voltage (current)
- The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the Power reset (except devices with persistent low voltage reset in internal vector mode).

Sample recommended circuits:



(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Sleep modes[1]	I_{CCSPLL}	PLL Sleep mode with CLKS1/2 = 48MHz, CLKP1/2 = 24MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	9	10.5	mA	Flash devices
			+125°C	9.7	13		
			+25°C	8	9.5	mA	MB96345/346
			+125°C	8.7	11.5		
		PLL Sleep mode with CLKS1/2 = CLKP1= 56MHz, CLKP2 = 28MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	14	15.5	mA	MB96F346/F347/F348
			+125°C	14.8	18		
			+25°C	13.5	15	mA	MB96345/346
			+125°C	14.3	17		
		PLL Sleep mode with CLKS1/2 = 72MHz, CLKP1 = 36MHz, CLKP2 = 18MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	10.5	12	mA	MB96F346/F347/F348Y/R/Ayy
			+125°C	11.3	14.5		
		PLL Sleep mode with CLKS1/2 = 80MHz, CLKP1 = 40MHz, CLKP2 = 20MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	TBD	TBD	mA	MB96F345
			+125°C	TBD	TBD		
		PLL Sleep mode with CLKS1/2 = 96MHz, CLKP1= 48MHz, CLKP2 = 24MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	15	16.5	mA	MB96F348T/H/CyB/C
			+125°C	15.8	19		
			+25°C	14	15.5	mA	MB96345/346
			+125°C	14.8	17.5		
	$I_{CCSMAIN}$	Main Sleep mode with CLKS1/2 = CLKP1/2 = 4MHz (CLKPLL, CLKSC and CLKRC stopped)	+25°C	1.5	1.8	mA	Flash devices
			+125°C	2	4.5		
			+25°C	1.5	1.8	mA	MB96345/346
			+125°C	2	3.8		

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Timer modes[1]	I_{CCTPLL}	PLL Timer mode with CLKMC = 4MHz, CLKPLL = 48MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	1.6	2	mA	Flash devices
			+125°C	2.1	5		
			+25°C	1.6	2	mA	MB96345/346
			+125°C	2.1	4		
	$I_{CCTMAIN}$	Main Timer mode with CLKMC = 4MHz, SMCR:LPMSS = 0 (CLKPLL, CLKRC and CLKSC stopped. Voltage regulator in high power mode)	+25°C	0.35	0.5	mA	MB96F346/F347/F348
			+125°C	0.85	3.3		
			+25°C	0.13	0.2	mA	MB96F345
			+125°C	0.63	3		
			+25°C	0.35	0.5	mA	MB96345/346
			+125°C	0.85	2.3		
		Main Timer mode with CLKMC = 4MHz, SMCR:LPMSS = 1 (CLKPLL, CLKRC and CLKSC stopped. Voltage regulator in low power mode)	+25°C	0.1	0.15	mA	Flash devices
			+125°C	0.6	2.9		
			+25°C	0.1	0.15		MB96345/346
			+125°C	0.6	1.9		
	I_{CCTRCH}	RC Timer mode with CLKRC = 2MHz, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)	+25°C	0.35	0.5	mA	MB96F346/F347/F348
			+125°C	0.85	3.3		
			+25°C	0.13	0.2	mA	MB96F345
			+125°C	0.63	3		
			+25°C	0.35	0.5	mA	MB96345/346
			+125°C	0.85	2.3		
		RC Timer mode with CLKRC = 2MHz, SMCR:LPMSS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode)	+25°C	0.1	0.15	mA	Flash devices
			+125°C	0.6	2.9		
			+25°C	0.1	0.15	mA	MB96345/346
			+125°C	0.6	1.9		

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Timer modes[1]	I_{CCTRCL}	RC Timer mode with CLKRC = 100kHz, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)	+25°C	0.3	0.45	mA	MB96F346/F347/F348
			+125°C	0.8	3.2		
			+25°C	0.08	0.15	mA	MB96F345
			+125°C	0.58	2.95		
			+25°C	0.3	0.45	mA	MB96345/346
			+125°C	0.8	2.2		
		RC Timer mode with CLKRC = 100kHz, SMCR:LPMSS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode)	+25°C	0.05	0.1	mA	Flash devices
			+125°C	0.55	2.85		
			+25°C	0.05	0.1	mA	MB96345/346
			+125°C	0.55	1.85		
	I_{CCTSUB}	Sub Timer mode with CLKSC = 32kHz (CLKMC, CLKPLL and CLKRC stopped)	+25°C	0.03	0.1	mA	Flash devices
			+125°C	0.53	2.85		
			+25°C	0.03	0.1	mA	MB96345/346
			+125°C	0.53	1.85		
Power supply current in Stop Mode	I_{CCH}	VRCR:LPMB[2:0] = 110_B (Core voltage at 1.8V)	+25°C	0.02	0.08	mA	Flash devices
			+125°C	0.52	2.8		
			+25°C	0.02	0.08	mA	MB96345/346
			+125°C	0.52	1.8		
		VRCR:LPMB[2:0] = 000_B (Core voltage at 1.2V)	+25°C	0.015	0.06	mA	Flash devices
			+125°C	0.4	2.3		
			+25°C	0.015	0.06	mA	MB96345/346
			+125°C	0.4	1.4		
Power supply current for active Low Voltage detector	I_{CCLVD}	Low voltage detector enabled (RCR:LVDE = 1)	-	5	10	µA	MB96F345 Must be added to all current above
			+25°C	90	140	µA	Other devices Must be added to all current above
			+125°C	100	150		

(T_A = –40°C to +125°C, V_{CC} = 3.0 to 4.5V, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

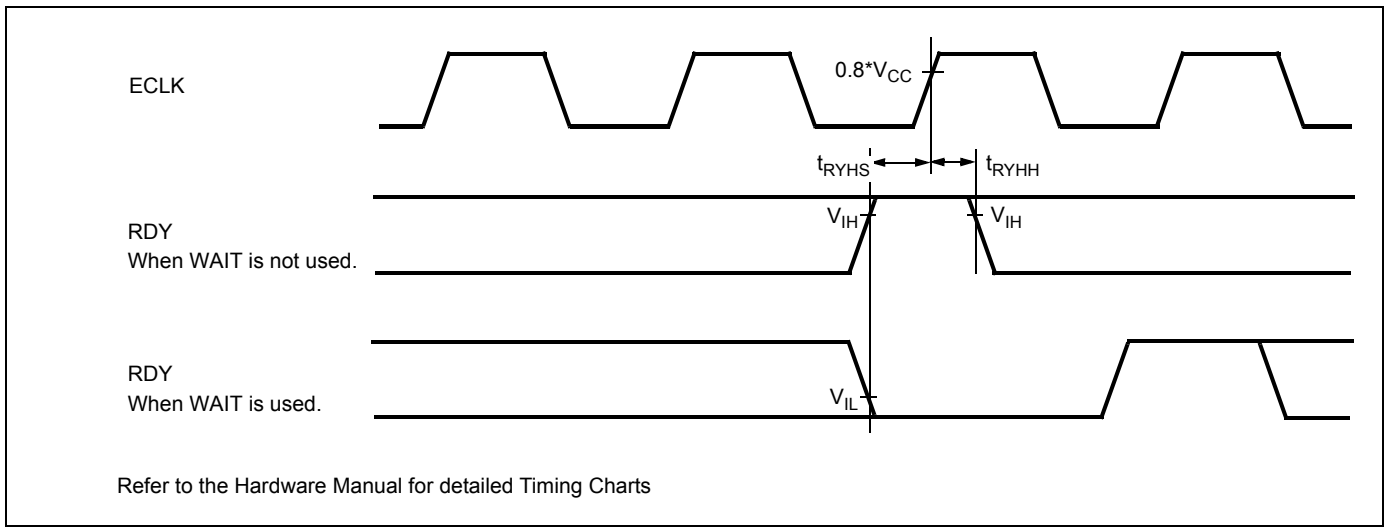
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
ECLK	t_{CYC}	ECLK	-	30	-	ns	
	t_{CHCL}			t_{CYC}/2-8	t_{CYC}/2+8		
	t_{CLCH}			t_{CYC}/2-8	t_{CYC}/2+8		
ECLK → UBX/ LBX / CSn time	t_{CHCBH}	CSn, UBX, LBX, ECLK	-	-25	25	ns	
	t_{CHCBL}			-25	25		
	t_{CLCBH}			-25	25		
	t_{CLCBL}			-25	25		
ECLK → ALE time	t_{CHLH}	ALE, ECLK	-	-15	15	ns	
	t_{CHLL}			-15	15		
	t_{CLLH}			-15	15		
	t_{CLLL}			-15	15		
ECLK → address valid time	t_{CHAV}	A[23:16], ECLK	-	-20	20	ns	
	t_{CLAV}			-20	20		
	t_{CLADV}	AD[15:0], ECLK	-	-20	20	ns	
	t_{CHADV}			-20	20		
ECLK → RDX /WRX time	t_{CHRWH}	RDX, WRX, WRLX, WRHX, ECLK	-	-15	15	ns	
	t_{CHRWL}			-15	15		
	t_{CLRWH}			-15	15		
	t_{CLRWL}			-15	15		

(T_A = –40°C to +125°C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
RDX ↑ ⇒ ALE ↑ time	t_{RHLH}	RDX, ALE	EACL:STS=1 and EACL:ACE=1	$3t_{CYC}/2 - 10$	-	ns	
			other ECL:STS, EACL:ACE setting	$t_{CYC}/2 - 10$	-		
Valid address ⇒ ECLK ↑ time	t_{AVCH}	A[23:16], ECLK	-	$t_{CYC} - 15$	-	ns	
	t_{ADVCH}	AD[15:0], ECLK		$t_{CYC}/2 - 15$	-		
RDX ↓ ⇒ ECLK ↑ time	t_{RLCH}	RDX, ECLK	-	$t_{CYC}/2 - 10$	-	ns	
ALE ↓ ⇒ RDX ↓ time	t_{LLRL}	ALE, RDX	EACL:STS=0	$t_{CYC}/2 - 10$	-	ns	
			EACL:STS=1	– 10	-		
ECLK↑ ⇒ Valid data input	t_{CHDV}	AD[15:0], ECLK	-	-	$t_{CYC} - 50$	ns	

(T_A = –40°C to +125°C, V_{CC} = 3.0 to 4.5V, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
ALE pulse width	t_{LHLL}	ALE	EACL:STS=0 and EACL:ACE=0	$t_{CYC}/2 - 8$	-	ns	
			EACL:STS=1	$t_{CYC} - 8$	-		
			EACL:STS=0 and EACL:ACE=1	$3t_{CYC}/2 - 8$	-		
Valid address ⇒ ALE ↓ time	t_{AVLL}	ALE, A[23:16],	EACL:STS=0 and EACL:ACE=0	$t_{CYC} - 20$	-	ns	
			EACL:STS=1 and EACL:ACE=0	$3t_{CYC}/2 - 20$	-		
			EACL:STS=0 and EACL:ACE=1	$2t_{CYC} - 20$	-		
			EACL:STS=1 and EACL:ACE=1	$5t_{CYC}/2 - 20$	-		
	t_{ADVLL}	ALE, AD[15:0]	EACL:STS=0 and EACL:ACE=0	$t_{CYC}/2 - 20$	-	ns	
			EACL:STS=1 and EACL:ACE=0	$t_{CYC} - 20$	-		
			EACL:STS=0 and EACL:ACE=1	$3t_{CYC}/2 - 20$	-		
			EACL:STS=1 and EACL:ACE=1	$2t_{CYC} - 20$	-		
ALE ↓ ⇒ Address valid time	t_{LLAX}	ALE, AD[15:0]	EACL:STS=0	$t_{CYC}/2 - 20$	-	ns	
			EACL:STS=1	-20	-		
Valid address ⇒ RDX ↓ time	t_{AVRL}	RDX, A[23:16]	EACL:ACE=0	$3t_{CYC}/2 - 20$	-	ns	
			EACL:ACE=1	$5t_{CYC}/2 - 20$	-		
	t_{ADVRL}	RDX, AD[15:0]	EACL:ACE=0	$t_{CYC} - 20$	-	ns	
			EACL:ACE=1	$2t_{CYC} - 20$	-		



Refer to the Hardware Manual for detailed Timing Charts

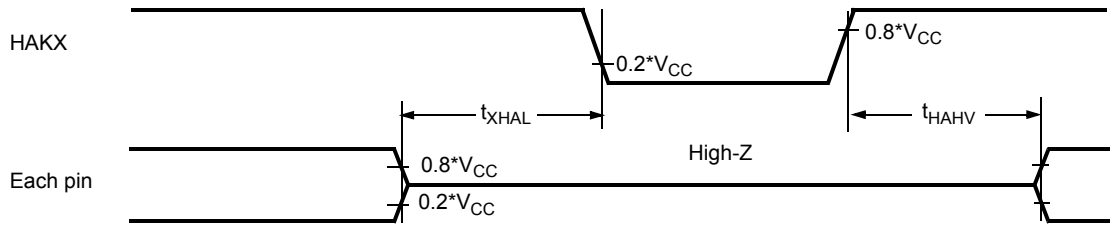
14.4.11 Hold Timing

(T_A = –40°C to +125°C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min	Max		
Pin floating ⇒ HAKX ↓ time	t_{XHAL}	HAKX	-	t_{CYC} – 20	t_{CYC} + 20	ns	
HAKX ↑ time ⇒ Pin valid time	t_{HAHV}	HAKX		t_{CYC} – 20	t_{CYC} + 20	ns	

(T_A = –40°C to +125°C, V_{CC} = 3.0 to 4.5V, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min	Max		
Pin floating ⇒ HAKX ↓ time	t_{XHAL}	HAKX	-	t_{CYC} – 25	t_{CYC} + 25	ns	
HAKX ↑ time ⇒ Pin valid time	t_{HAHV}	HAKX		t_{CYC} – 25	t_{CYC} + 25	ns	



Refer to the Hardware Manual for detailed Timing Charts

14.6 Alarm Comparator

(T_A = -40 °C to +125 °C, V_{CC} = AV_{CC} = 3.0V - 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Power supply current	I_{A5ALMF}	AV_{CC}	-	25	45	µA	Alarm comparator enabled in fast mode (one channel)
	I_{A5ALMS}		-	7	13	µA	Alarm comparator enabled in slow mode (one channel)
	I_{A5ALMH}		-	-	5	µA	Alarm comparator disabled
ALARM pin input current	I_{ALIN}	ALARM0, ALARM1	-1	-	+1	µA	T_A = 25 °C
			-3	-	+3	µA	T_A = 125 °C
ALARM pin input voltage range	V_{ALIN}		0	-	AV_{CC}	V	
External low threshold high->low transition	$V_{EVTL(H->L)}$		0.36 * AV_{CC} -0.25	0.36 * AV_{CC} -0.1	-	V	INTREF = 0
External low threshold low->high transition	$V_{EVTL(L->H)}$		-	0.36 * AV_{CC} +0.1	0.36 * AV_{CC} +0.25	V	
External high threshold high->low transition	$V_{EVTH(H->L)}$		0.78 * AV_{CC} -0.25	0.78 * AV_{CC} -0.1	-	V	
External high threshold low->high transition	$V_{EVTH(L->H)}$			0.78 * AV_{CC} +0.1	0.78 * AV_{CC} +0.25	V	
Internal low threshold high->low transition	$V_{IVTL(H->L)}$		0.9	1.1	-	V	INTREF = 1
Internal low threshold low->high transition	$V_{IVTL(L->H)}$		-	1.3	1.55	V	
Internal high threshold high->low transition	$V_{IVTH(H->L)}$		2.2	2.4	-	V	
Internal high threshold low->high transition	$V_{IVTH(L->H)}$		-	2.6	2.85	V	
Switching hysteresis	V_{HYS}		50	-	300	mV	
Comparison time	t_{COMPF}		-	0.1	1	µs	CMD = 1 (fast)
	t_{COMPS}		-	1	10	µs	CMD = 0 (slow)
Power-up stabilization time after enabling alarm comparator	t_{PD}		-	1	5	ms	Threshold levels specified above are not guaranteed within this time
Slow/Fast mode transition time	t_{CMD}		-	100	500	µs	

18.1 MCU with CAN Controller

Part number	Flash/ROM	Subclock	Persistent Low Voltage Reset	Package
MB96F347YSB PQC-GSE2	Flash A (416KB)	No	Yes	100 pin Plastic QFP (FPT-100P-M22)
MB96F347RSB PQC-GSE2			No	
MB96F347YWB PQC-GSE2		Yes	Yes	
MB96F347RWB PQC-GSE2			No	
MB96F347YSB PMC-GSE2		No	Yes	100 pin Plastic LQFP (FPT-100P-M20)
MB96F347RSB PMC-GSE2			No	
MB96F347YWB PMC-GSE2		Yes	Yes	
MB96F347RWB PMC-GSE2			No	
MB96F348YSB PQC-GSE2	Flash A (544KB)	No	Yes	100 pin Plastic QFP (FPT-100P-M22)
MB96F348RSB PQC-GSE2			No	
MB96F348YWB PQC-GSE2		Yes	Yes	
MB96F348RWB PQC-GSE2			No	
MB96F348YSB PMC-GSE2		No	Yes	100 pin Plastic LQFP (FPT-100P-M20)
MB96F348RSB PMC-GSE2			No	
MB96F348YWB PMC-GSE2		Yes	Yes	
MB96F348RWB PMC-GSE2			No	
MB96F348TSC PQC-GSE2	Flash A (544KB) Flash B (32KB)	No	Yes	100 pin Plastic QFP (FPT-100P-M22)
MB96F348HSC PQC-GSE2			No	
MB96F348TWC PQC-GSE2		Yes	Yes	
MB96F348HWC PQC-GSE2			No	
MB96F348TSC PMC-GSE2		No	Yes	100 pin Plastic LQFP (FPT-100P-M20)
MB96F348HSC PMC-GSE2			No	
MB96F348TWC PMC-GSE2		Yes	Yes	
MB96F348HWC PMC-GSE2			No	
MB96V300BRB-ES(for evaluation)	Emulated by ext. RAM	Yes	No	416 pin Plastic BGA (BGA-416P-M02)