Infineon Technologies - MB96F348ASBPMC-GS-N2E2 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

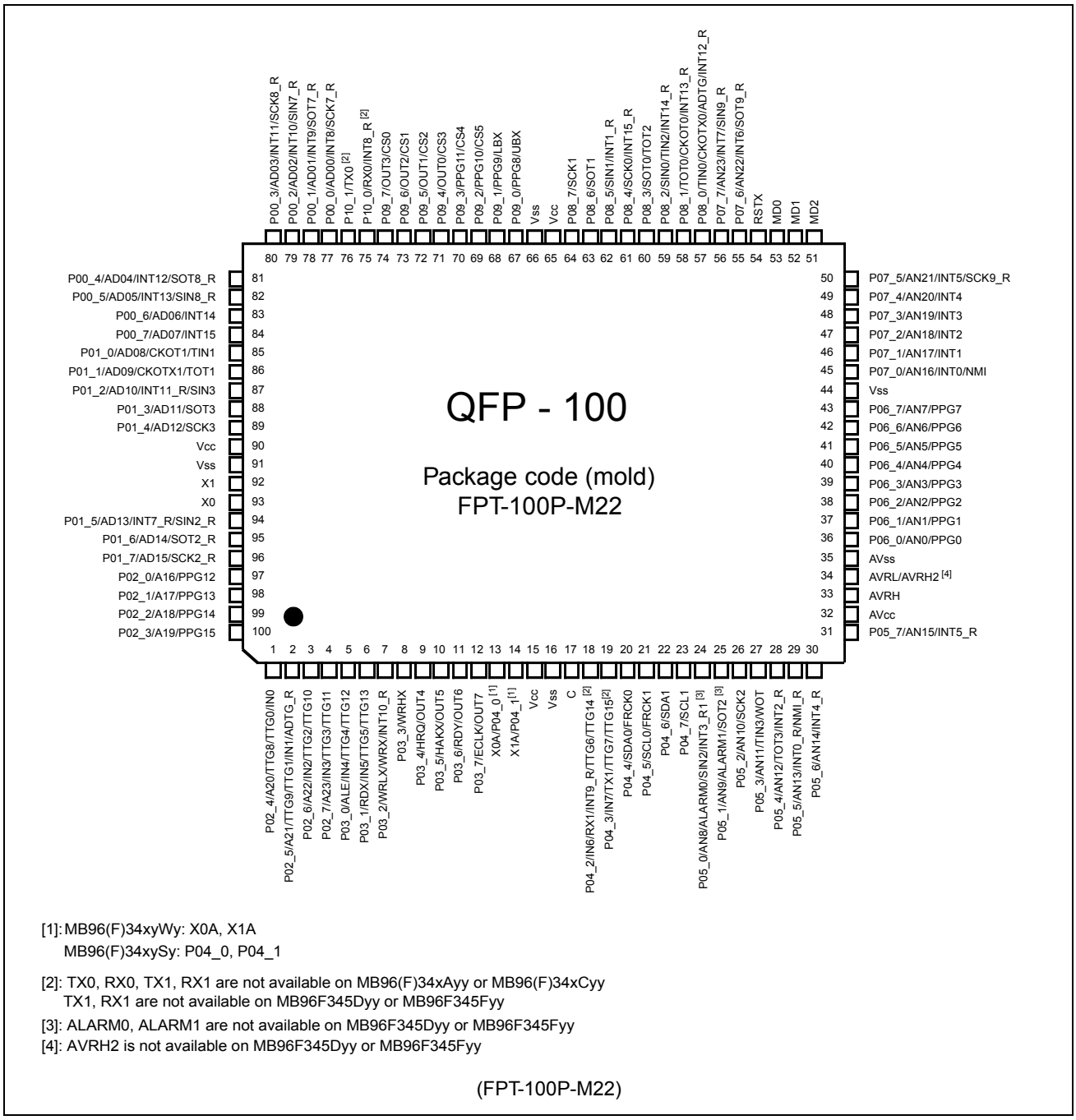
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	56MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, LVR, POR, PWM, WDT
Number of I/O	82
Program Memory Size	544KB (544K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f348asbpmc-gs-n2e2

Feature	Description
Alarm comparator	■ Monitors an external voltage and generates an interrupt in case of a voltage lower or higher than the defined thresholds ■ Threshold voltages defined externally or generated internally ■ Status is readable, interrupts can be masked separately
I/O Ports	■ Virtually all external pins can be used as general purpose I/O ■ All push-pull outputs (except when used as I2C SDA/SCL line) ■ Bit-wise programmable as input/output or peripheral signal ■ Bit-wise programmable input enable ■ Bit-wise programmable input levels: Automotive / CMOS-Schmitt trigger / TTL (TTL levels not supported by all devices) ■ Bit-wise programmable pull-up resistor ■ Bit-wise programmable output driving strength for EMI optimization
Packages	■ 100-pin plastic QFP and LQFP
Flash Memory	■ Supports automatic programming, Embedded Algorithm ■ Write/Erase/Erase-Suspend/Resume commands ■ A flag indicating completion of the algorithm ■ Number of erase cycles: 10,000 times ■ Data retention time: 20 years ■ Erase can be performed on each sector individually ■ Sector protection ■ Flash Security feature to protect the content of the Flash ■ Low voltage detection during Flash erase

3. Pin Assignments

Figure 2. Pin assignment of MB96(F)34x (FPT-100P-M22)



[1]: MB96(F)34xyWy: X0A, X1A
MB96(F)34xySy: P04_0, P04_1

[2]: TX0, RX0, TX1, RX1 are not available on MB96(F)34xAyy or MB96(F)34xCyy
TX1, RX1 are not available on MB96F345Dyy or MB96F345Fyy

[3]: ALARM0, ALARM1 are not available on MB96F345Dyy or MB96F345Fyy

[4]: AVRH2 is not available on MB96F345Dyy or MB96F345Fyy

(FPT-100P-M22)

Remark:

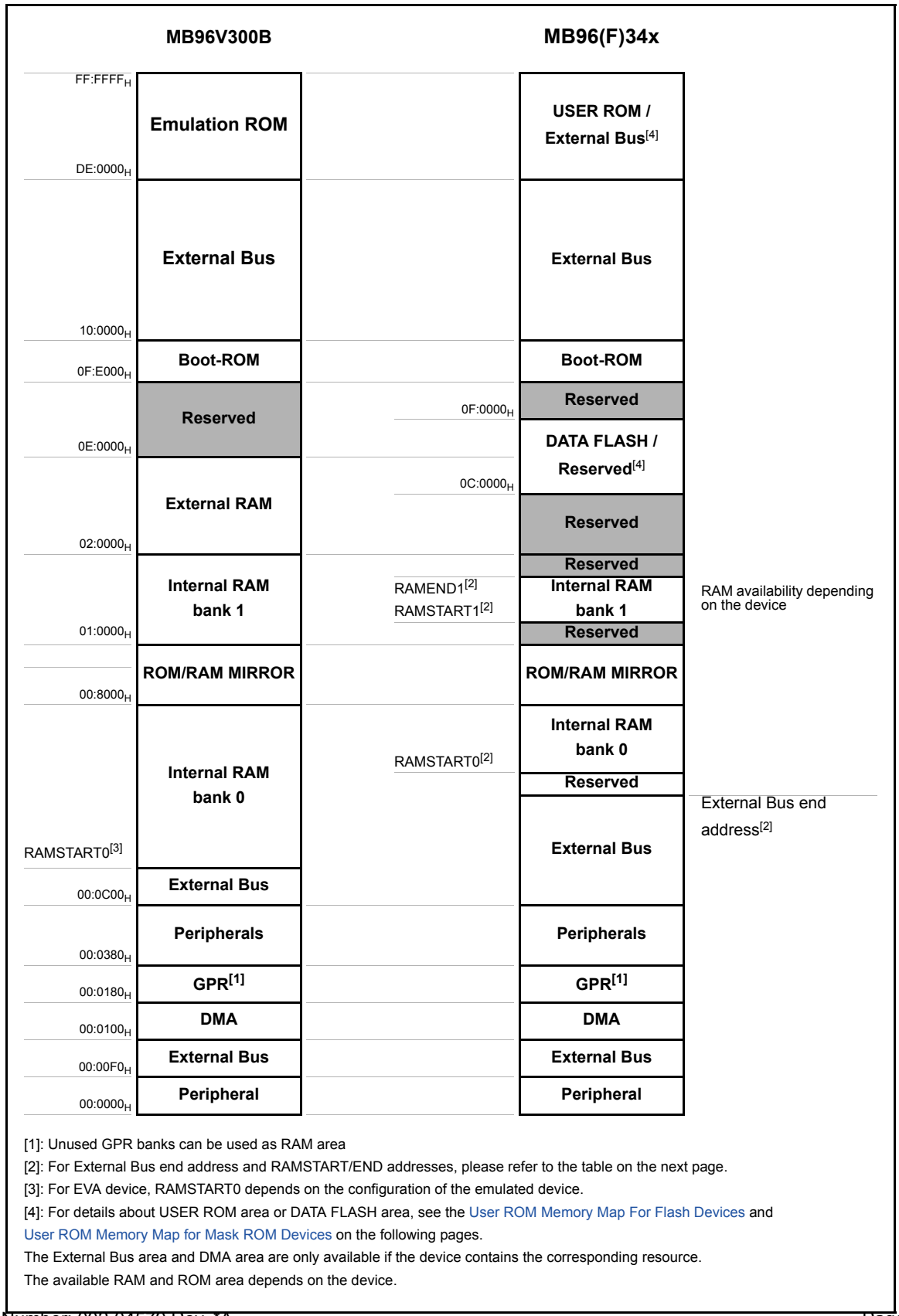
MB96(F)34x products are pin-compatible to F^{2}MC-16LX family MB90340 series.

4. Pin Function Description

Table 1: Pin Function description

Pin name	Feature	Description
ADn	External bus	External bus interface (multiplexed mode) address output and data input/output
ADTG	ADC	A/D converter trigger input
ADTG_R	ADC	Relocated A/D converter trigger input
ALARMn	Alarm comparator	Alarm Comparator n input
ALE	External bus	External bus Address Latch Enable output
An	External bus	External bus address output
ANn	ADC	A/D converter channel n input
AV_{CC}	Supply	Analog circuits power supply
AVRH	ADC	A/D converter high reference voltage input
AVRH2	ADC	Alternative A/D converter high reference voltage input
AVRL	ADC	A/D converter low reference voltage input
AV_{SS}	Supply	Analog circuits power supply
C	Voltage regulator	Internally regulated power supply stabilization capacitor pin
CKOTn	Clock output function	Clock Output function n output
CKOTXn	Clock output function	Clock Output function n inverted output
ECLK	External bus	External bus clock output
CSn	External bus	External bus chip select n output
FRCKn	Free Running Timer	Free Running Timer n input
HAKX	External bus	External bus Hold Acknowledge
HRQ	External bus	External bus Hold Request
INn	ICU	Input Capture Unit n input
INTn	External Interrupt	External Interrupt n input
INTn_R	External Interrupt	Relocated External Interrupt n input
LBX	External bus	External Bus Interface Lower Byte select strobe output
MDn	Core	Input pins for specifying the operating mode.
NMI	External Interrupt	Non-Maskable Interrupt input
NMI_R	External Interrupt	Relocated Non-Maskable Interrupt input
OUTn	OCU	Output Compare Unit n waveform output
Pxx_n	GPIO	General purpose IO
PPGn	PPG	Programmable Pulse Generator n output
RDX	External bus	External bus interface read strobe output

7. Memory Map



[1]: Unused GPR banks can be used as RAM area

[2]: For External Bus end address and RAMSTART/END addresses, please refer to the table on the next page.

[3]: For EVA device, RAMSTART0 depends on the configuration of the emulated device.

[4]: For details about USER ROM area or DATA FLASH area, see the User ROM Memory Map For Flash Devices and User ROM Memory Map for Mask ROM Devices on the following pages.

The External Bus area and DMA area are only available if the device contains the corresponding resource.

The available RAM and ROM area depends on the device.

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000114_H	DMA2 - I/O register address pointer low byte	IOAL2	IOA2	R/W
000115_H	DMA2 - I/O register address pointer high byte	IOAH2		R/W
000116_H	DMA2 - Data counter low byte	DCTL2	DCT2	R/W
000117_H	DMA2 - Data counter high byte	DCTH2		R/W
000118_H	DMA3 - Buffer address pointer low byte	BAPL3		R/W
000119_H	DMA3 - Buffer address pointer middle byte	BAPM3		R/W
$00011A_H$	DMA3 - Buffer address pointer high byte	BAPH3		R/W
$00011B_H$	DMA3 - DMA control register	DMACS3		R/W
$00011C_H$	DMA3 - I/O register address pointer low byte	IOAL3	IOA3	R/W
$00011D_H$	DMA3 - I/O register address pointer high byte	IOAH3		R/W
$00011E_H$	DMA3 - Data counter low byte	DCTL3	DCT3	R/W
$00011F_H$	DMA3 - Data counter high byte	DCTH3		R/W
000120_H	DMA4 - Buffer address pointer low byte	BAPL4		R/W
000121_H	DMA4 - Buffer address pointer middle byte	BAPM4		R/W
000122_H	DMA4 - Buffer address pointer high byte	BAPH4		R/W
000123_H	DMA4 - DMA control register	DMACS4		R/W
000124_H	DMA4 - I/O register address pointer low byte	IOAL4	IOA4	R/W
000125_H	DMA4 - I/O register address pointer high byte	IOAH4		R/W
000126_H	DMA4 - Data counter low byte	DCTL4	DCT4	R/W
000127_H	DMA4 - Data counter high byte	DCTH4		R/W
000128_H	DMA5 - Buffer address pointer low byte	BAPL5		R/W
000129_H	DMA5 - Buffer address pointer middle byte	BAPM5		R/W
$00012A_H$	DMA5 - Buffer address pointer high byte	BAPH5		R/W
$00012B_H$	DMA5 - DMA control register	DMACS5		R/W
$00012C_H$	DMA5 - I/O register address pointer low byte	IOAL5	IOA5	R/W
$00012D_H$	DMA5 - I/O register address pointer high byte	IOAH5		R/W
$00012E_H$	DMA5 - Data counter low byte	DCTL5	DCT5	R/W
$00012F_H$	DMA5 - Data counter high byte	DCTH5		R/W
000130_H-$00017F_H$	Reserved			-
000180_H-$00037F_H$	CPU - General Purpose registers (RAM access)	GPR_RAM		R/W
000380_H	DMA0 - Interrupt select	DISEL0		R/W
000381_H	DMA1 - Interrupt select	DISEL1		R/W

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000407_H	PLL Control register High	PLLCRH		R/W
000408_H	RC clock timer control register	RCTCR		R/W
000409_H	Main clock timer control register	MCTCR		R/W
$00040A_H$	Sub clock timer control register	SCTCR		R/W
$00040B_H$	Reset cause and clock status register with clear function	RCCSRC		R
$00040C_H$	Reset configuration register	RCR		R/W
$00040D_H$	Reset cause and clock status register	RCCSR		R
$00040E_H$	Watch dog timer configuration register	WDTC		R/W
$00040F_H$	Watch dog timer clear pattern register	WDTCP		W
000410_H-000414_H	Reserved			-
000415_H	Clock output activation register	COAR		R/W
000416_H	Clock output configuration register 0	COCR0		R/W
000417_H	Clock output configuration register 1	COCR1		R/W
000418_H	Clock Modulator control register	CMCR		R/W
000419_H	Reserved			-
$00041A_H$	Clock Modulator Parameter register Low	CMPRL	CMPR	R/W
$00041B_H$	Clock Modulator Parameter register High	CMPRH		R/W
$00041C_H$-$00042B_H$	Reserved			-
$00042C_H$	Voltage Regulator Control register	VRCR		R/W
$00042D_H$	Clock Input and LVD Control Register	CILCR		R/W
$00042E_H$-$00042F_H$	Reserved			-
000430_H	I/O Port P00 - Data Direction Register	DDR00		R/W
000431_H	I/O Port P01 - Data Direction Register	DDR01		R/W
000432_H	I/O Port P02 - Data Direction Register	DDR02		R/W
000433_H	I/O Port P03 - Data Direction Register	DDR03		R/W
000434_H	I/O Port P04 - Data Direction Register	DDR04		R/W
000435_H	I/O Port P05 - Data Direction Register	DDR05		R/W
000436_H	I/O Port P06 - Data Direction Register	DDR06		R/W
000437_H	I/O Port P07 - Data Direction Register	DDR07		R/W
000438_H	I/O Port P08 - Data Direction Register	DDR08		R/W
000439_H	I/O Port P09 - Data Direction Register	DDR09		R/W
$00043A_H$	I/O Port P10 - Data Direction Register	DDR10		R/W

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000473_H	I/O Port P07 - Extended Port Input Level Register	EPILR07		R/W
000474_H	I/O Port P08 - Extended Port Input Level Register	EPILR08		R/W
000475_H	I/O Port P09 - Extended Port Input Level Register	EPILR09		R/W
000476_H	I/O Port P10 - Extended Port Input Level Register	EPILR10		R/W
000477_H-$00047F_H$	Reserved			-
000480_H	I/O Port P00 - Port Output Drive Register	PODR00		R/W
000481_H	I/O Port P01 - Port Output Drive Register	PODR01		R/W
000482_H	I/O Port P02 - Port Output Drive Register	PODR02		R/W
000483_H	I/O Port P03 - Port Output Drive Register	PODR03		R/W
000484_H	I/O Port P04 - Port Output Drive Register	PODR04		R/W
000485_H	I/O Port P05 - Port Output Drive Register	PODR05		R/W
000486_H	I/O Port P06 - Port Output Drive Register	PODR06		R/W
000487_H	I/O Port P07 - Port Output Drive Register	PODR07		R/W
000488_H	I/O Port P08 - Port Output Drive Register	PODR08		R/W
000489_H	I/O Port P09 - Port Output Drive Register	PODR09		R/W
$00048A_H$	I/O Port P10 - Port Output Drive Register	PODR10		R/W
$00048B_H$-$00049B_H$	Reserved			-
$00049C_H$	I/O Port P08 - Port High Drive Register	PHDR08		R/W
$00049D_H$	I/O Port P09 - Port High Drive Register	PHDR09		R/W
$00049E_H$	I/O Port P10 - Port High Drive Register	PHDR10		R/W
$00049F_H$-$0004A7_H$	Reserved			-
$0004A8_H$	I/O Port P00 - Pull-Up resistor Control Register	PUCR00		R/W
$0004A9_H$	I/O Port P01 - Pull-Up resistor Control Register	PUCR01		R/W
$0004AA_H$	I/O Port P02 - Pull-Up resistor Control Register	PUCR02		R/W
$0004AB_H$	I/O Port P03 - Pull-Up resistor Control Register	PUCR03		R/W
$0004AC_H$	I/O Port P04 - Pull-Up resistor Control Register	PUCR04		R/W
$0004AD_H$	I/O Port P05 - Pull-Up resistor Control Register	PUCR05		R/W
$0004AE_H$	I/O Port P06 - Pull-Up resistor Control Register	PUCR06		R/W
$0004AF_H$	I/O Port P07 - Pull-Up resistor Control Register	PUCR07		R/W
$0004B0_H$	I/O Port P08 - Pull-Up resistor Control Register	PUCR08		R/W
$0004B1_H$	I/O Port P09 - Pull-Up resistor Control Register	PUCR09		R/W
$0004B2_H$	I/O Port P10 - Pull-Up resistor Control Register	PUCR10		R/W

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$00056D_H$	PPG7 - Timer register			R
$00056E_H$	PPG7 - Period setting register		PCSR7	W
$00056F_H$	PPG7 - Period setting register			W
000570_H	PPG7 - Duty cycle register		PDUT7	W
000571_H	PPG7 - Duty cycle register			W
000572_H	PPG7 - Control status register Low	PCNL7	PCN7	R/W
000573_H	PPG7 - Control status register High	PCNH7		R/W
000574_H	PPG11-PPG8 - General Control register 1 Low	GCN1L2	GCN12	R/W
000575_H	PPG11-PPG8 - General Control register 1 High	GCN1H2		R/W
000576_H	PPG11-PPG8 - General Control register 2 Low	GCN2L2	GCN22	R/W
000577_H	PPG11-PPG8 - General Control register 2 High	GCN2H2		R/W
000578_H	PPG8 - Timer register		PTMR8	R
000579_H	PPG8 - Timer register			R
$00057A_H$	PPG8 - Period setting register		PCSR8	W
$00057B_H$	PPG8 - Period setting register			W
$00057C_H$	PPG8 - Duty cycle register		PDUT8	W
$00057D_H$	PPG8 - Duty cycle register			W
$00057E_H$	PPG8 - Control status register Low	PCNL8	PCN8	R/W
$00057F_H$	PPG8 - Control status register High	PCNH8		R/W
000580_H	PPG9 - Timer register		PTMR9	R
000581_H	PPG9 - Timer register			R
000582_H	PPG9 - Period setting register		PCSR9	W
000583_H	PPG9 - Period setting register			W
000584_H	PPG9 - Duty cycle register		PDUT9	W
000585_H	PPG9 - Duty cycle register			W
000586_H	PPG9 - Control status register Low	PCNL9	PCN9	R/W
000587_H	PPG9 - Control status register High	PCNH9		R/W
000588_H	PPG10 - Timer register		PTMR10	R
000589_H	PPG10 - Timer register			R
$00058A_H$	PPG10 - Period setting register		PCSR10	W
$00058B_H$	PPG10 - Period setting register			W
$00058C_H$	PPG10 - Duty cycle register		PDUT10	W

Table 4: I/O map MB96(F)34x

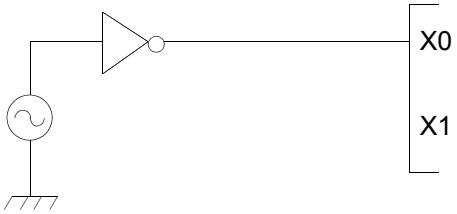
Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$0006EB_H$	External Bus - Area configuration register 5 High	EACH5		R/W
$0006EC_H$	External Bus - Area select register 2	EAS2		R/W
$0006ED_H$	External Bus - Area select register 3	EAS3		R/W
$0006EE_H$	External Bus - Area select register 4	EAS4		R/W
$0006EF_H$	External Bus - Area select register 5	EAS5		R/W
$0006F0_H$	External Bus - Mode register	EBM		R/W
$0006F1_H$	External Bus - Clock and Function register	EBCF		R/W
$0006F2_H$	External Bus - Address output enable register 0	EBAE0		R/W
$0006F3_H$	External Bus - Address output enable register 1	EBAE1		R/W
$0006F4_H$	External Bus - Address output enable register 2	EBAE2		R/W
$0006F5_H$	External Bus - Control signal register	EBCS		R/W
$0006F6_H$-$0006FF_H$	Reserved			-
000700_H	CAN0 - Control register Low	CTRLRL0	CTRLR0	R/W
000701_H	CAN0 - Control register High (reserved)	CTRLRH0		R
000702_H	CAN0 - Status register Low	STATRL0	STATR0	R/W
000703_H	CAN0 - Status register High (reserved)	STATRH0		R
000704_H	CAN0 - Error Counter Low (Transmit)	ERRCNTL0	ERRCNT0	R
000705_H	CAN0 - Error Counter High (Receive)	ERRCNTH0		R
000706_H	CAN0 - Bit Timing Register Low	BTRL0	BTR0	R/W
000707_H	CAN0 - Bit Timing Register High	BTRH0		R/W
000708_H	CAN0 - Interrupt Register Low	INTRL0	INTR0	R
000709_H	CAN0 - Interrupt Register High	INTRH0		R
$00070A_H$	CAN0 - Test Register Low	TESTRL0	TESTR0	R/W
$00070B_H$	CAN0 - Test Register High (reserved)	TESTRH0		R
$00070C_H$	CAN0 - BRP Extension register Low	BRPERL0	BRPER0	R/W
$00070D_H$	CAN0 - BRP Extension register High (reserved)	BRPERH0		R
$00070E_H$-$00070F_H$	Reserved			-
000710_H	CAN0 - IF1 Command request register Low	IF1CREQL0	IF1CREQ0	R/W
000711_H	CAN0 - IF1 Command request register High	IF1CREQH0		R/W
000712_H	CAN0 - IF1 Command Mask register Low	IF1CMSKL0	IF1CMSK0	R/W
000713_H	CAN0 - IF1 Command Mask register High (reserved)	IF1CMSKH0		R
000714_H	CAN0 - IF1 Mask 1 Register Low	IF1MSK1L0	IF1MSK10	R/W

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000822_H	CAN1 - IF1 Data B1 Low	IF1DTB1L1	IF1DTB11	R/W
000823_H	CAN1 - IF1 Data B1 High	IF1DTB1H1		R/W
000824_H	CAN1 - IF1 Data B2 Low	IF1DTB2L1	IF1DTB21	R/W
000825_H	CAN1 - IF1 Data B2 High	IF1DTB2H1		R/W
000826_H-$00083F_H$	Reserved			-
000840_H	CAN1 - IF2 Command request register Low	IF2CREQL1	IF2CREQ1	R/W
000841_H	CAN1 - IF2 Command request register High	IF2CREQH1		R/W
000842_H	CAN1 - IF2 Command Mask register Low	IF2CMSKL1	IF2CMSK1	R/W
000843_H	CAN1 - IF2 Command Mask register High (reserved)	IF2CMSKH1		R
000844_H	CAN1 - IF2 Mask 1 Register Low	IF2MSK1L1	IF2MSK11	R/W
000845_H	CAN1 - IF2 Mask 1 Register High	IF2MSK1H1		R/W
000846_H	CAN1 - IF2 Mask 2 Register Low	IF2MSK2L1	IF2MSK21	R/W
000847_H	CAN1 - IF2 Mask 2 Register High	IF2MSK2H1		R/W
000848_H	CAN1 - IF2 Arbitration 1 Register Low	IF2ARB1L1	IF2ARB11	R/W
000849_H	CAN1 - IF2 Arbitration 1 Register High	IF2ARB1H1		R/W
$00084A_H$	CAN1 - IF2 Arbitration 2 Register Low	IF2ARB2L1	IF2ARB21	R/W
$00084B_H$	CAN1 - IF2 Arbitration 2 Register High	IF2ARB2H1		R/W
$00084C_H$	CAN1 - IF2 Message Control Register Low	IF2MCTRL1	IF2MCTR1	R/W
$00084D_H$	CAN1 - IF2 Message Control Register High	IF2MCTRH1		R/W
$00084E_H$	CAN1 - IF2 Data A1 Low	IF2DTA1L1	IF2DTA11	R/W
$00084F_H$	CAN1 - IF2 Data A1 High	IF2DTA1H1		R/W
000850_H	CAN1 - IF2 Data A2 Low	IF2DTA2L1	IF2DTA21	R/W
000851_H	CAN1 - IF2 Data A2 High	IF2DTA2H1		R/W
000852_H	CAN1 - IF2 Data B1 Low	IF2DTB1L1	IF2DTB11	R/W
000853_H	CAN1 - IF2 Data B1 High	IF2DTB1H1		R/W
000854_H	CAN1 - IF2 Data B2 Low	IF2DTB2L1	IF2DTB21	R/W
000855_H	CAN1 - IF2 Data B2 High	IF2DTB2H1		R/W
000856_H-$00087F_H$	Reserved			-
000880_H	CAN1 - Transmission Request 1 Register Low	TREQR1L1	TREQR11	R
000881_H	CAN1 - Transmission Request 1 Register High	TREQR1H1		R
000882_H	CAN1 - Transmission Request 2 Register Low	TREQR2L1	TREQR21	R
000883_H	CAN1 - Transmission Request 2 Register High	TREQR2H1		R

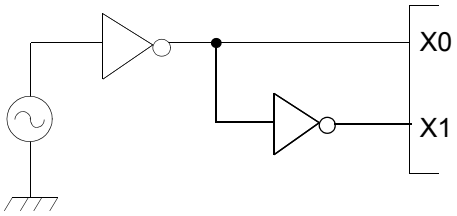
13.3.1 Single phase external clock

■ When using a single phase external clock, X0 pin must be driven and X1 pin left open.



13.3.2 Opposite phase external clock

■ When using an opposite phase external clock, X1 (X1A) must be supplied with a clock signal which has the opposite phase to the X0 (X0A) pins.



13.4 Unused sub clock signal

If the pins X0A and X1A are not connected to an oscillator, a pull-down resistor must be connected on the X0A pin and the X1A pin must be left open.

13.5 Notes on PLL clock mode operation

If the PLL clock mode is selected and no external oscillator is operating or no external clock is supplied, the microcontroller attempts to work with the free oscillating PLL. Performance of this operation, however, cannot be guaranteed.

13.6 Power supply pins (V_{CC}/v_{SS})

It is required that all V_{CC}-level as well as all V_{SS}-level power supply pins are at the same potential. If there is more than one V_{CC} or V_{SS} level, the device may operate incorrectly or be damaged even within the guaranteed operating range.

V_{CC} and V_{SS} must be connected to the device from the power supply with lowest possible impedance.

As a measure against power supply noise, it is required to connect a bypass capacitor of about 0.1 μF between V_{CC} and V_{SS} as close as possible to V_{CC} and V_{SS} pins.

14.3 DC characteristics

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input H voltage	V_{IH}	Port inputs Pnn_m	CMOS Hysteresis 0.8/0.2 input selected	0.8 V_{CC}	-	V_{CC} + 0.3	V	
			CMOS Hysteresis 0.7/0.3 input selected	0.7 V_{CC}	-	V_{CC} + 0.3	V	$V_{CC} \geq 4.5V$
				0.74 V_{CC}	-	V_{CC} + 0.3	V	$V_{CC} < 4.5V$
			AUTOMOTIVE Hysteresis input selected	0.8 V_{CC}	-	V_{CC} + 0.3	V	
			TTL input selected	2.0	-	V_{CC} + 0.3	V	
	V_{IHX0F}	X0	External clock in “Fast Clock Input mode”	0.8 V_{CC}	-	V_{CC} + 0.3	V	Not available in MB96F34xY/R/AxA
	V_{IHX0S}	X0,X1, X0A,X1A	External clock in “oscillation mode”	2.5	-	V_{CC} + 0.3	V	
	V_{IHR}	RSTX	-	0.8 V_{CC}	-	V_{CC} + 0.3	V	CMOS Hysteresis input
	V_{IHM}	MD2-MD0	-	V_{CC} - 0.3	-	V_{CC} + 0.3	V	
Input L voltage	V_{IL}	Port inputs Pnn_m	CMOS Hysteresis 0.8/0.2 input selected	V_{SS} - 0.3	-	0.2 V_{CC}	V	
			CMOS Hysteresis 0.7/0.3 input selected	V_{SS} - 0.3	-	0.3 V_{CC}	V	
			AUTOMOTIVE Hysteresis input selected	V_{SS} - 0.3	-	0.5 V_{CC}	V	$V_{CC} \geq 4.5V$
				V_{SS} - 0.3	-	0.46 V_{CC}		$V_{CC} < 4.5V$
			TTL input selected	V_{SS} - 0.3	-	0.8	V	
	V_{ILX0F}	X0	External clock in “Fast Clock Input mode”	V_{SS} - 0.3	-	0.2 V_{CC}	V	Not available in MB96F34xY/R/AxA
	V_{ILX0S}	X0,X1, X0A,X1A	External clock in “oscillation mode”	V_{SS} - 0.3	-	0.4	V	
	V_{ILR}	RSTX	-	V_{SS} - 0.3	-	0.2 V_{CC}	V	CMOS Hysteresis input
	V_{ILM}	MD2-MD0	-	V_{SS} - 0.3	-	V_{SS} + 0.3	V	
Output H voltage	V_{OH2}	Normal outputs	$4.5V \leq V_{CC} \leq 5.5V$, I_{OH} = -2mA / $3.0V \leq V_{CC} < 4.5V$, I_{OH} = -1.6mA	V_{CC} - 0.5	-	-	V	Driving strength set to 2mA
	V_{OH5}	Normal outputs	$4.5V \leq V_{CC} \leq 5.5V$, I_{OH} = -5mA / $3.0V \leq V_{CC} < 4.5V$, I_{OH} = -3mA	V_{CC} - 0.5	-	-	V	Driving strength set to 5mA
	V_{OH3}	3mA outputs	$4.5V \leq V_{CC} \leq 5.5V$, I_{OH} = -3mA / $3.0V \leq V_{CC} < 4.5V$, I_{OH} = -2mA	V_{CC} - 0.5	-	-	V	

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Sleep modes[1]	I_{CCSPLL}	PLL Sleep mode with CLKS1/2 = 48MHz, CLKP1/2 = 24MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	9	10.5	mA	Flash devices
			+125°C	9.7	13		
			+25°C	8	9.5	mA	MB96345/346
			+125°C	8.7	11.5		
		PLL Sleep mode with CLKS1/2 = CLKP1= 56MHz, CLKP2 = 28MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	14	15.5	mA	MB96F346/F347/F348
			+125°C	14.8	18		
			+25°C	13.5	15	mA	MB96345/346
			+125°C	14.3	17		
		PLL Sleep mode with CLKS1/2 = 72MHz, CLKP1 = 36MHz, CLKP2 = 18MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	10.5	12	mA	MB96F346/F347/F348Y/R/Ayy
			+125°C	11.3	14.5		
		PLL Sleep mode with CLKS1/2 = 80MHz, CLKP1 = 40MHz, CLKP2 = 20MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	TBD	TBD	mA	MB96F345
			+125°C	TBD	TBD		
		PLL Sleep mode with CLKS1/2 = 96MHz, CLKP1= 48MHz, CLKP2 = 24MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	15	16.5	mA	MB96F348T/H/CyB/C
			+125°C	15.8	19		
			+25°C	14	15.5	mA	MB96345/346
			+125°C	14.8	17.5		
	$I_{CCSMAIN}$	Main Sleep mode with CLKS1/2 = CLKP1/2 = 4MHz (CLKPLL, CLKSC and CLKRC stopped)	+25°C	1.5	1.8	mA	Flash devices
			+125°C	2	4.5		
			+25°C	1.5	1.8	mA	MB96345/346
			+125°C	2	3.8		

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Timer modes[1]	I_{CCTRCL}	RC Timer mode with CLKRC = 100kHz, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)	+25°C	0.3	0.45	mA	MB96F346/F347/F348
			+125°C	0.8	3.2		
			+25°C	0.08	0.15	mA	MB96F345
			+125°C	0.58	2.95		
			+25°C	0.3	0.45	mA	MB96345/346
			+125°C	0.8	2.2		
		RC Timer mode with CLKRC = 100kHz, SMCR:LPMSS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode)	+25°C	0.05	0.1	mA	Flash devices
			+125°C	0.55	2.85		
			+25°C	0.05	0.1	mA	MB96345/346
			+125°C	0.55	1.85		
	I_{CCTSUB}	Sub Timer mode with CLKSC = 32kHz (CLKMC, CLKPLL and CLKRC stopped)	+25°C	0.03	0.1	mA	Flash devices
			+125°C	0.53	2.85		
			+25°C	0.03	0.1	mA	MB96345/346
			+125°C	0.53	1.85		
Power supply current in Stop Mode	I_{CCH}	VRCR:LPMB[2:0] = 110_B (Core voltage at 1.8V)	+25°C	0.02	0.08	mA	Flash devices
			+125°C	0.52	2.8		
			+25°C	0.02	0.08	mA	MB96345/346
			+125°C	0.52	1.8		
		VRCR:LPMB[2:0] = 000_B (Core voltage at 1.2V)	+25°C	0.015	0.06	mA	Flash devices
			+125°C	0.4	2.3		
			+25°C	0.015	0.06	mA	MB96345/346
			+125°C	0.4	1.4		
Power supply current for active Low Voltage detector	I_{CCLVD}	Low voltage detector enabled (RCR:LVDE = 1)	-	5	10	µA	MB96F345 Must be added to all current above
			+25°C	90	140	µA	Other devices Must be added to all current above
			+125°C	100	150		

14.4.8 Bus Timing (Read)

(T_A = –40°C to +125°C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
ALE pulse width	t_{LHLL}	ALE	EACL:STS=0 and EACL:ACE=0	$t_{CYC}/2 - 5$	-	ns	
			EACL:STS=1	$t_{CYC} - 5$	-		
			EACL:STS=0 and EACL:ACE=1	$3t_{CYC}/2 - 5$	-		
Valid address ⇒ ALE ↓ time	t_{AVLL}	ALE, A[23:16],	EACL:STS=0 and EACL:ACE=0	$t_{CYC} - 15$	-	ns	
			EACL:STS=1 and EACL:ACE=0	$3t_{CYC}/2 - 15$	-		
			EACL:STS=0 and EACL:ACE=1	$2t_{CYC} - 15$	-		
			EACL:STS=1 and EACL:ACE=1	$5t_{CYC}/2 - 15$	-		
	t_{ADVLL}	ALE,AD[15:0]	EACL:STS=0 and EACL:ACE=0	$t_{CYC}/2 - 15$	-	ns	
			EACL:STS=1 and EACL:ACE=0	$t_{CYC} - 15$	-		
			EACL:STS=0 and EACL:ACE=1	$3t_{CYC}/2 - 15$	-		
			EACL:STS=1 and EACL:ACE=1	$2t_{CYC} - 15$	-		
ALE ↓ ⇒ Address valid time	t_{LLAX}	ALE, AD[15:0]	EACL:STS=0	$t_{CYC}/2 - 15$	-	ns	
			EACL:STS=1	-15	-		
Valid address ⇒ RDX ↓ time	t_{AVRL}	RDX, A[23:16]	EACL:ACE=0	$3t_{CYC}/2 - 15$	-	ns	
			EACL:ACE=1	$5t_{CYC}/2 - 15$	-		
	t_{ADVRL}	RDX, AD[15:0]	EACL:ACE=0	$t_{CYC} - 15$	-	ns	
			EACL:ACE=1	$2t_{CYC} - 15$	-		
Valid address ⇒ Valid data input	t_{AVDV}	A[23:16], AD[15:0]	EACL:ACE=0	-	$3t_{CYC} - 55$	ns	w/o cycle extension
			EACL:ACE=1	-	$4t_{CYC} - 55$		
	t_{ADVDV}	AD[15:0]	EACL:ACE=0	-	$5t_{CYC}/2 - 55$	ns	w/o cycle extension
			EACL:ACE=1	-	$7t_{CYC}/2 - 55$		
RDX pulse width	t_{RLRH}	RDX	-	$3\ t_{CYC}/2 - 5$	-	ns	w/o cycle extension
RDX ↓ ⇒ Valid data input	t_{RLDV}	RDX, AD[15:0]	-	-	$3\ t_{CYC}/2 - 50$	ns	w/o cycle extension
RDX ↑ ⇒ Data hold time	t_{RHDX}	RDX, AD[15:0]	-	0	-	ns	
Address valid ⇒ Data hold time	t_{AXDX}	A[23:16], AD[15:0]	-	0	-	ns	

14.4.12 USART timing

WARNING: The values given below are for an I/O driving strength IO_{drive} = 5mA. If IO_{drive} is 2mA, all the maximum output timing described in the different tables must then be increased by 10ns.

(T_A = -40°C to 125°C, V_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Condition	V_{CC} = AV_{CC}= 4.5V to 5.5V		V_{CC} = AV_{CC}= 3.0V to 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYCI}	SCKn	Internal Shift Clock Mode	4 t_{CLKP1}	-	4 t_{CLKP1}	-	ns
SCK ↓→ SOT delay time	t_{SLOVI}	SCKn, SOTn		-20	+20	-30	+30	ns
SOT → SCK ↑ delay time	t_{OVSHI}	SCKn, SOTn		N*t_{CLKP1} - 20 [1]	-	N*t_{CLKP1} - 30 [1]	-	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCKn, SINn		t_{CLKP1} + 45	-	t_{CLKP1} + 55	-	ns
SCK ↑→ Valid SIN hold time	t_{SHIXI}	SCKn, SINn		0	-	0	-	ns
Serial clock “L” pulse width	t_{SLSHE}	SCKn	External Shift Clock Mode	t_{CLKP1} + 10	-	t_{CLKP1} + 10	-	ns
Serial clock “H” pulse width	t_{SHSLE}	SCKn		t_{CLKP1} + 10	-	t_{CLKP1} + 10	-	ns
SCK ↓→ SOT delay time	t_{SLOVE}	SCKn, SOTn		-	2 t_{CLKP1} + 45	-	2 t_{CLKP1} + 55	ns
Valid SIN → SCK ↑	t_{IVSHE}	SCKn, SINn		t_{CLKP1}/2 + 10	-	t_{CLKP1}/2 + 10	-	ns
SCK ↑→ Valid SIN hold time	t_{SHIXE}	SCKn, SINn		t_{CLKP1} + 10	-	t_{CLKP1} + 10	-	ns
SCK fall time	t_{FE}	SCKn		-	20	-	20	ns
SCK rise time	t_{RE}	SCKn		-	20	-	20	ns

Notes:

- AC characteristic in CLK synchronized mode.
- C_L is the load capacity value of pins when testing.
- Depending on the used machine clock frequency, the maximum possible baud rate can be limited by some parameters. These parameters are shown in “MB96300 Super series HARDWARE MANUAL”.
- t_{CLKP1} is the cycle time of the peripheral clock 1 (CLKP1), Unit : ns

[1]: Parameter N depends on t_{SCYCI} and can be calculated as follows:

- if t_{SCYCI} = 2*k*t_{CLKP1}, then N = k, where k is an integer > 2
- if t_{SCYCI} = (2*k+1)*t_{CLKP1}, then N = k+1, where k is an integer > 1

Examples:

t_{SCYCI}	N
4*t_{CLKP1}	2
5*t_{CLKP1},	3
7*t_{CLKP1},	4
...	...

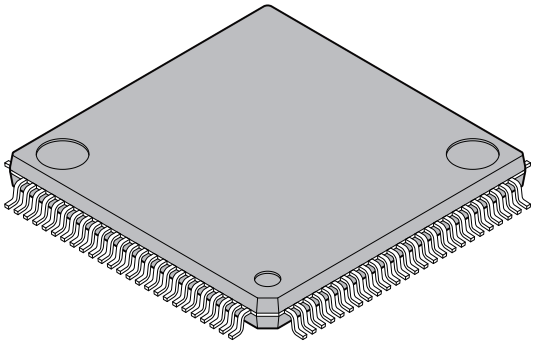
14.8 Flash Memory Program/erase Characteristics

(T_A = -40°C to 105°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time Program/Data Flash (Main Flash)	-	0.9	3.6	s	Without erasure pre-programming time
Sector erase time Data Flash	-	0.5	2	s	Without erasure pre-programming time
	-	0.8	3.6	s	Including erasure pre-programming time
Chip erase time Program/Data Flash (Main Flash)	-	n*0.9	n*3.6	s	Without erasure pre-programming time (n is the number of Flash sector of the device)
Chip erase time Data Flash	-	2.5	10	s	Without erasure pre-programming time
	-	3.7	16.4	s	Including erasure pre-programming time
Word (16-bit width) programming time Program/Data Flash (Main Flash)	-	23	370	us	Without overhead time for submitting write command
Byte (8-bit width) programming time Data Flash	-	15	100	us	Without overhead time for submitting write command
Program/Erase cycle	10000	-	-	cycle	100 000 Program/Erase cycles are under evaluation by Cypress
Flash data retention time	20	-	-	year	[1]

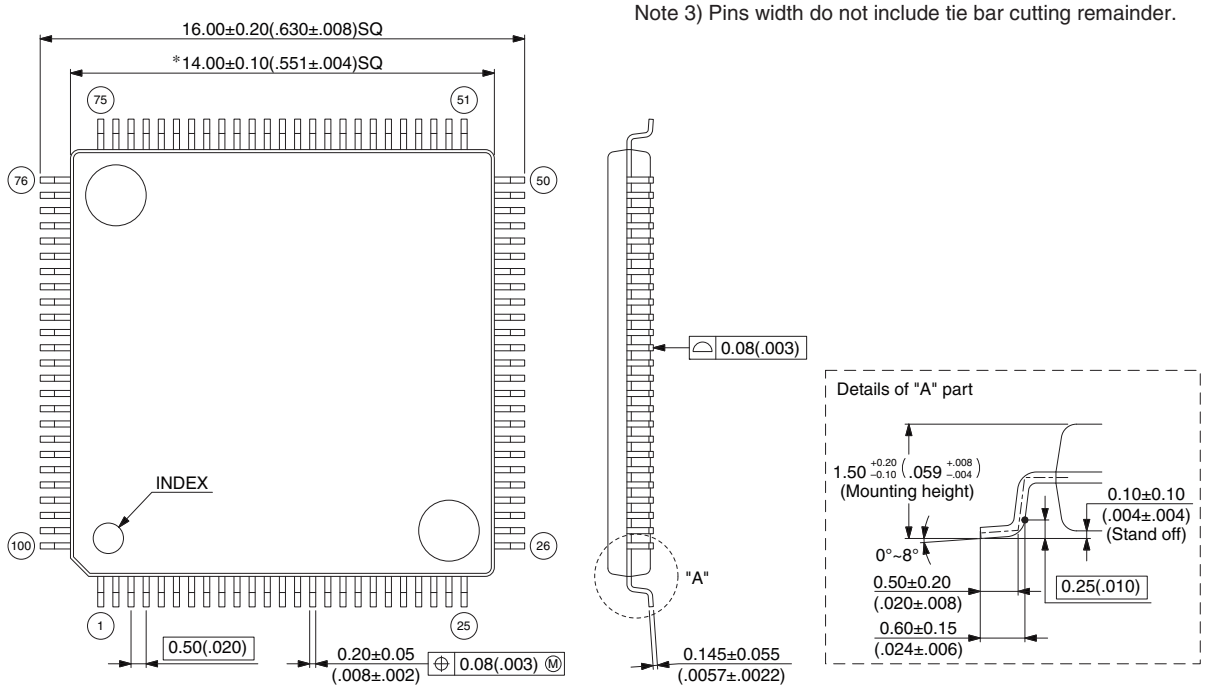
[1]: This value was converted from the results of evaluating the reliability of the technology (using Arrhenius equation to convert high temperature measurements into normalized value at 85^{o}C)

16. Package Dimension MB96(F)34x LQFP 100P

100-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	14.0 mm × 14.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm Max
	Weight	0.65 g
(FPT-100P-M20)	Code (Reference)	P-LFQFP100-14×14-0.50

100-pin plastic LQFP
(FPT-100P-M20)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values

18. Ordering Information

18.1 MCU with CAN Controller

Part number	Flash/ROM	Subclock	Persistent Low Voltage Reset	Package
MB96345YSA PQC-GSE2 [1]	ROM (160KB)	No	Yes	100 pin Plastic QFP (FPT-100P-M22)
MB96345RSA PQC-GSE2 [1]			No	
MB96345YWA PQC-GSE2 [1]		Yes	Yes	
MB96345RWA PQC-GSE2 [1]			No	
MB96345YSA PMC-GSE2[1]		No	Yes	100 pin Plastic LQFP (FPT-100P-M20)
MB96345RSA PMC-GSE2 [1]			No	
MB96345YWA PMC-GSE2 [1]		Yes	Yes	
MB96345RWA PMC-GSE2[1]			No	
MB96346YSA PQC-GSE2[1]	ROM (288KB)	No	Yes	100 pin Plastic QFP (FPT-100P-M22)
MB96346RSA PQC-GSE2[1]			No	
MB96346YWA PQC-GSE2 [1]		Yes	Yes	
MB96346RWA PQC-GSE2 [1]			No	
MB96346YSA PMC-GSE2 [1]		No	Yes	100 pin Plastic LQFP (FPT-100P-M20)
MB96346RSA PMC-GSE2[1]			No	
MB96346YWA PMC-GSE2 [1]		Yes	Yes	
MB96346RWA PMC-GSE2 [1]			No	
MB96F345FSA PQC-GSE2 [1]	Flash A (160KB) Data Flash A (64KB)	No	Yes	100 pin Plastic QFP (FPT-100P-M22)
MB96F345DSA PQC-GSE2 [1]			No	
MB96F345FWA PQC-GSE2 [1]		Yes	Yes	
MB96F345DWA PQC-GSE2 [1]			No	
MB96F345FSA PMC-GSE2 [1]		No	Yes	100 pin Plastic LQFP (FPT-100P-M20)
MB96F345DSA PMC-GSE2 [1]			No	
MB96F345FWA PMC-GSE2[1]		Yes	Yes	
MB96F345DWA PMC-GSE2 [1]			No	
MB96F346YSB PQC-GSE2	Flash A (288KB)	No	Yes	100 pin Plastic QFP (FPT-100P-M22)
MB96F346RSB PQC-GSE2			No	
MB96F346YWB PQC-GSE2		Yes	Yes	
MB96F346RWB PQC-GSE2			No	
MB96F346YSB PMC-GSE2		No	Yes	100 pin Plastic LQFP (FPT-100P-M20)
MB96F346RSB PMC-GSE2			No	
MB96F346YWB PMC-GSE2		Yes	Yes	
MB96F346RWB PMC-GSE2			No	

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