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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Discontinued at Digi-Key
Core Processor	F ² MC-16FX
Core Size	16-Bit
Speed	56MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, LVR, POR, PWM, WDT
Number of I/O	82
Program Memory Size	544KB (544K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f348asbpmc-gse2

1. Product Lineup

Features		MB96V300B	MB96(F)34x
Product type		Evaluation sample	Flash product: MB96F34x Mask ROM product: MB9634x
Product options			
YS		NA	Low voltage reset persistently on / Single clock
RS			Low voltage reset can be disabled / Single clock
YW			Low voltage reset persistently on / Dual clock
RW			Low voltage reset can be disabled / Dual clock
TS			indep. 32KB Flash / Low voltage reset persistently on / Single clock
HS			indep. 32KB Flash / Low voltage reset can be disabled / Single clock
TW			indep. 32KB Flash / Low voltage reset persistently on / Dual clock
HW			indep. 32KB Flash / Low voltage reset can be disabled / Dual clock
FS			64KB Data Flash / Low voltage reset persistently on / Single clock
DS			64KB Data Flash / Low voltage reset can be disabled / Single clock
FW			64KB Data Flash / Low voltage reset persistently on / Dual clock
DW			64KB Data Flash / Low voltage reset can be disabled / Dual clock
AS			No CAN / Low voltage reset can be disabled / Single clock devices
CS			No CAN / indep. 32KB Flash / Low voltage reset can be disabled / Single clock
AW			No CAN / Low voltage reset can be disabled / Dual clock
CW			No CAN / indep. 32KB Flash / Low voltage reset can be disabled / Dual clock
Flash/ROM	RAM		
160KB	8KB	ROM/Flash memory emulation by external RAM, 92KB internal RAM	MB96345Y ^[1] , MB96345R ^[1]
224KB [Flash A: 160KB, Data Flash A: 64KB]	8KB		MB96F345F ^[1] , MB96F345D ^[1]
288KB	16KB		MB96F346Y, MB96346Y ^[1] , MB96F346R, MB96346R ^[1] , MB96F346A
416KB	16KB		MB96F347Y, MB96F347R, MB96F347A
544KB	24KB		MB96F348Y, MB96F348R, MB96F348A
576KB [Flash A: 544KB, Flash B: 32KB]	24KB		MB96F348T, MB96F348H, MB96F348C
Package		BGA416	FPT-100P-M20 FPT-100P-M22
DMA		16 channels	6 channels
USART		10 channels	7 channels

2. Block Diagram

Figure 1. Block diagram of MB96(F)34x

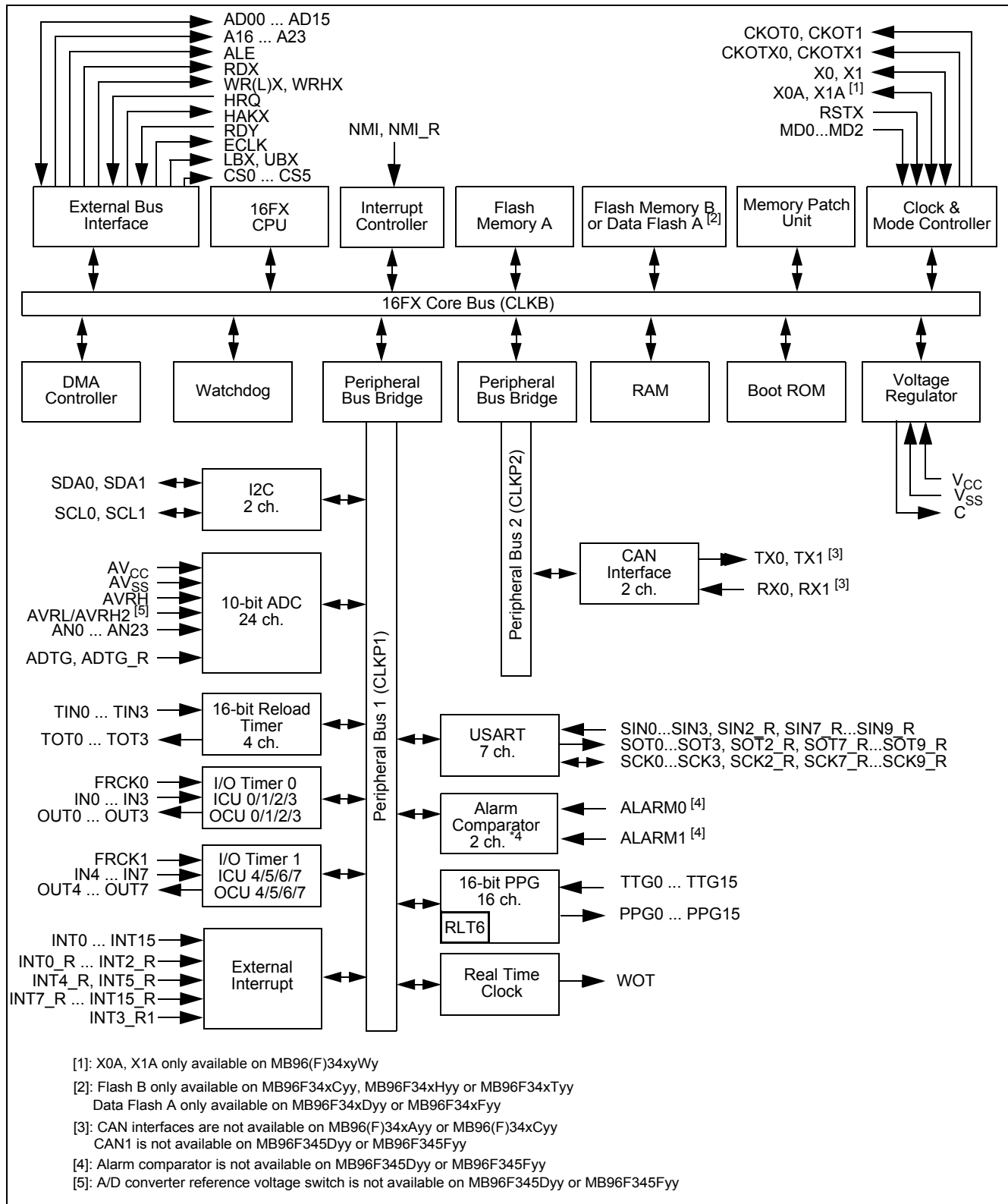
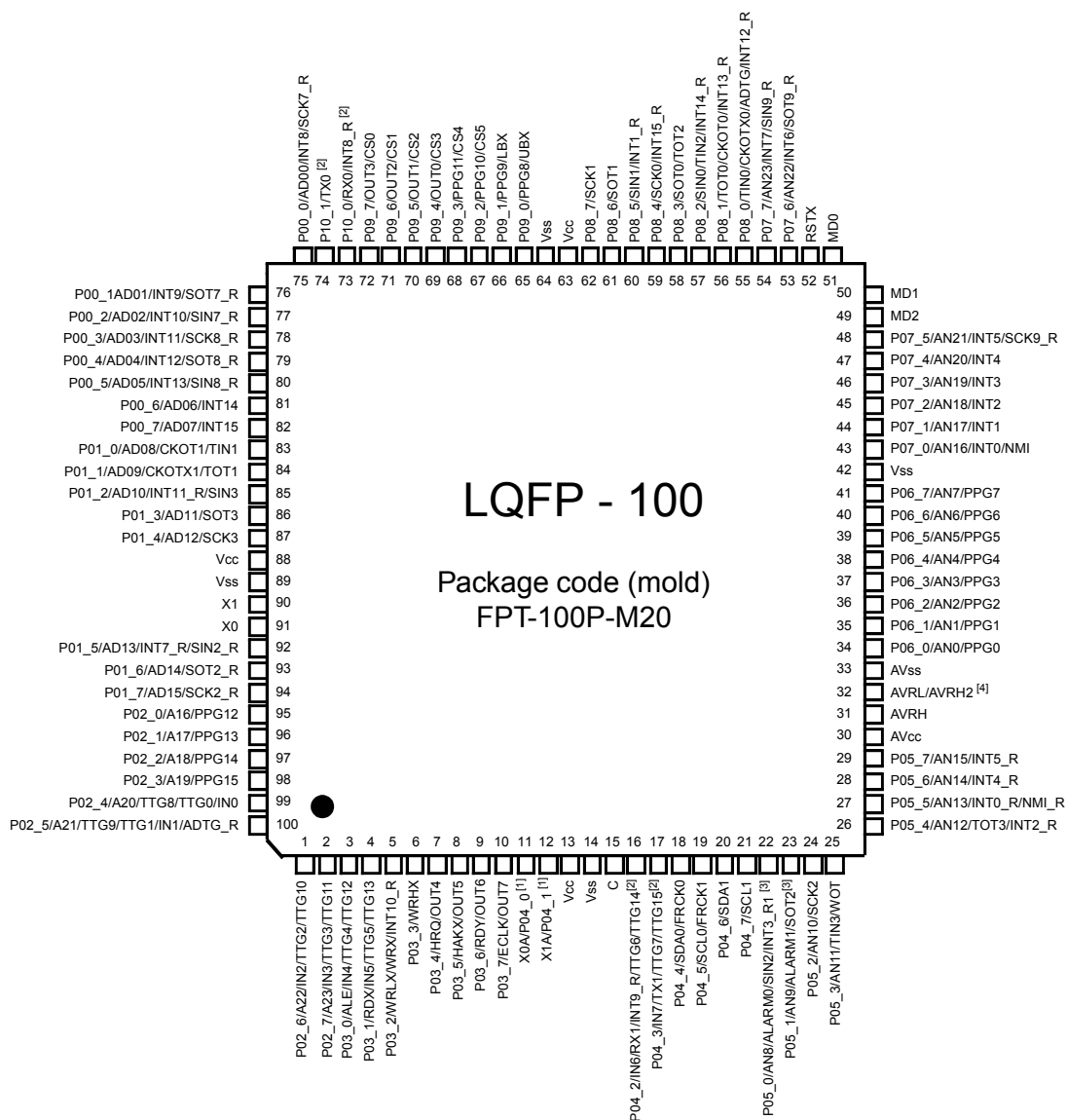
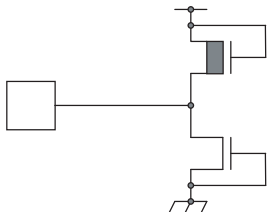
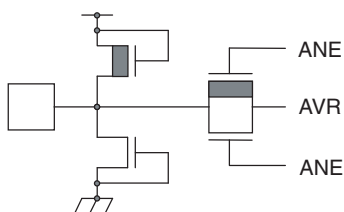
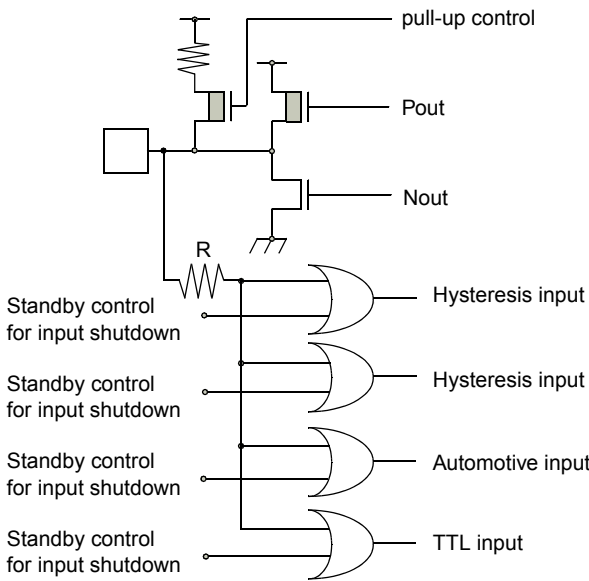


Figure 3. Pin assignment of MB96(F)34x (FPT-100P-M20)



Type	Circuit	Remarks
F		■ Power supply input protection circuit
G		■ A/D converter ref+ (AVRH/AVRH2) power supply input pin with protection circuit ■ Flash devices do not have a protection circuit against VCC for pins AVRH/AVRH2 ■ Devices without AVRH reference switch do not have an analog switch for the AVRL pin
H		■ CMOS level output (programmable $I_{OL} = 5\text{mA}$, $I_{OH} = -5\text{mA}$ and $I_{OL} = 2\text{mA}$, $I_{OH} = -2\text{mA}$) ■ 2 different CMOS hysteresis inputs with input shutdown function * ■ Automotive input with input shutdown function ■ TTL input with input shutdown function * ■ Programmable pull-up resistor: 50kΩ approx. *MB96F345Dyy or MB96F345Fyy: Only Automotive input and CMOS hysteresis input (0.7/0.3) are supported

7. Memory Map

MB96V300B			MB96(F)34x		
FF:FFFF _H	Emulation ROM		USER ROM / External Bus ^[4]		
DE:0000 _H					
	External Bus		External Bus		
10:0000 _H					
0F:E000 _H	Boot-ROM		Boot-ROM		
	Reserved	0F:0000 _H	Reserved		
0E:0000 _H			DATA FLASH / Reserved ^[4]		
	External RAM	0C:0000 _H	Reserved		
02:0000 _H			Reserved		
	Internal RAM bank 1	RAMEND1 ^[2] RAMSTART1 ^[2]	Internal RAM bank 1		RAM availability depending on the device
01:0000 _H			Reserved		
	ROM/RAM MIRROR		ROM/RAM MIRROR		
00:8000 _H			Internal RAM bank 0		
	Internal RAM bank 0	RAMSTART0 ^[2]	Reserved		
RAMSTART0 ^[3]			External Bus		External Bus end address ^[2]
00:0C00 _H	External Bus				
	Peripherals		Peripherals		
00:0380 _H					
00:0180 _H	GPR ^[1]		GPR ^[1]		
00:0100 _H	DMA		DMA		
00:00F0 _H	External Bus		External Bus		
00:0000 _H	Peripheral		Peripheral		

[1]: Unused GPR banks can be used as RAM area

[2]: For External Bus end address and RAMSTART/END addresses, please refer to the table on the next page.

[3]: For EVA device, RAMSTART0 depends on the configuration of the emulated device.

[4]: For details about USER ROM area or DATA FLASH area, see the [User ROM Memory Map For Flash Devices](#) and [User ROM Memory Map for Mask ROM Devices](#) on the following pages.

The External Bus area and DMA area are only available if the device contains the corresponding resource.

The available RAM and ROM area depends on the device.

11. I/O Map

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000000 _H	I/O Port P00 - Port Data Register	PDR00		R/W
000001 _H	I/O Port P01 - Port Data Register	PDR01		R/W
000002 _H	I/O Port P02 - Port Data Register	PDR02		R/W
000003 _H	I/O Port P03 - Port Data Register	PDR03		R/W
000004 _H	I/O Port P04 - Port Data Register	PDR04		R/W
000005 _H	I/O Port P05 - Port Data Register	PDR05		R/W
000006 _H	I/O Port P06 - Port Data Register	PDR06		R/W
000007 _H	I/O Port P07 - Port Data Register	PDR07		R/W
000008 _H	I/O Port P08 - Port Data Register	PDR08		R/W
000009 _H	I/O Port P09 - Port Data Register	PDR09		R/W
00000A _H	I/O Port P10 - Port Data Register	PDR10		R/W
00000B _H -000017 _H	Reserved			-
000018 _H	ADC0 - Control Status register Low	ADCSL	ADCS	R/W
000019 _H	ADC0 - Control Status register High	ADCSH		R/W
00001A _H	ADC0 - Data Register Low	ADCRL	ADCR	R
00001B _H	ADC0 - Data Register High	ADCRH		R
00001C _H	ADC0 - Setting Register		ADSR	R/W
00001D _H	ADC0 - Setting Register			R/W
00001E _H	ADC0 - Extended Configuration Register	ADECR		R/W
00001F _H	Reserved			-
000020 _H	FRT0 - Data register of free-running timer		TCDT0	R/W
000021 _H	FRT0 - Data register of free-running timer			R/W
000022 _H	FRT0 - Control status register of free-running timer Low	TCCSL0	TCCS0	R/W
000023 _H	FRT0 - Control status register of free-running timer High	TCCSH0		R/W
000024 _H	FRT1 - Data register of free-running timer		TCDT1	R/W
000025 _H	FRT1 - Data register of free-running timer			R/W
000026 _H	FRT1 - Control status register of free-running timer Low	TCCSL1	TCCS1	R/W
000027 _H	FRT1 - Control status register of free-running timer High	TCCSH1		R/W
000028 _H	OCU0 - Output Compare Control Status	OCS0		R/W
000029 _H	OCU1 - Output Compare Control Status	OCS1		R/W
00002A _H	OCU0 - Compare Register		OCCP0	R/W

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000715 _H	CAN0 - IF1 Mask 1 Register High	IF1MSK1H0		R/W
000716 _H	CAN0 - IF1 Mask 2 Register Low	IF1MSK2L0	IF1MSK20	R/W
000717 _H	CAN0 - IF1 Mask 2 Register High	IF1MSK2H0		R/W
000718 _H	CAN0 - IF1 Arbitration 1 Register Low	IF1ARB1L0	IF1ARB10	R/W
000719 _H	CAN0 - IF1 Arbitration 1 Register High	IF1ARB1H0		R/W
00071A _H	CAN0 - IF1 Arbitration 2 Register Low	IF1ARB2L0	IF1ARB20	R/W
00071B _H	CAN0 - IF1 Arbitration 2 Register High	IF1ARB2H0		R/W
00071C _H	CAN0 - IF1 Message Control Register Low	IF1MCTRL0	IF1MCTR0	R/W
00071D _H	CAN0 - IF1 Message Control Register High	IF1MCTRH0		R/W
00071E _H	CAN0 - IF1 Data A1 Low	IF1DTA1L0	IF1DTA10	R/W
00071F _H	CAN0 - IF1 Data A1 High	IF1DTA1H0		R/W
000720 _H	CAN0 - IF1 Data A2 Low	IF1DTA2L0	IF1DTA20	R/W
000721 _H	CAN0 - IF1 Data A2 High	IF1DTA2H0		R/W
000722 _H	CAN0 - IF1 Data B1 Low	IF1DTB1L0	IF1DTB10	R/W
000723 _H	CAN0 - IF1 Data B1 High	IF1DTB1H0		R/W
000724 _H	CAN0 - IF1 Data B2 Low	IF1DTB2L0	IF1DTB20	R/W
000725 _H	CAN0 - IF1 Data B2 High	IF1DTB2H0		R/W
000726 _H -00073F _H	Reserved			-
000740 _H	CAN0 - IF2 Command request register Low	IF2CREQL0	IF2CREQ0	R/W
000741 _H	CAN0 - IF2 Command request register High	IF2CREQH0		R/W
000742 _H	CAN0 - IF2 Command Mask register Low	IF2CMSKL0	IF2CMSK0	R/W
000743 _H	CAN0 - IF2 Command Mask register High (reserved)	IF2CMSKH0		R
000744 _H	CAN0 - IF2 Mask 1 Register Low	IF2MSK1L0	IF2MSK10	R/W
000745 _H	CAN0 - IF2 Mask 1 Register High	IF2MSK1H0		R/W
000746 _H	CAN0 - IF2 Mask 2 Register Low	IF2MSK2L0	IF2MSK20	R/W
000747 _H	CAN0 - IF2 Mask 2 Register High	IF2MSK2H0		R/W
000748 _H	CAN0 - IF2 Arbitration 1 Register Low	IF2ARB1L0	IF2ARB10	R/W
000749 _H	CAN0 - IF2 Arbitration 1 Register High	IF2ARB1H0		R/W
00074A _H	CAN0 - IF2 Arbitration 2 Register Low	IF2ARB2L0	IF2ARB20	R/W
00074B _H	CAN0 - IF2 Arbitration 2 Register High	IF2ARB2H0		R/W
00074C _H	CAN0 - IF2 Message Control Register Low	IF2MCTRL0	IF2MCTR0	R/W
00074D _H	CAN0 - IF2 Message Control Register High	IF2MCTRH0		R/W

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000884 _H -00088F _H	Reserved			-
000890 _H	CAN1 - New Data 1 Register Low	NEWDT1L1	NEWDT11	R
000891 _H	CAN1 - New Data 1 Register High	NEWDT1H1		R
000892 _H	CAN1 - New Data 2 Register Low	NEWDT2L1	NEWDT21	R
000893 _H	CAN1 - New Data 2 Register High	NEWDT2H1		R
000894 _H -00089F _H	Reserved			-
0008A0 _H	CAN1 - Interrupt Pending 1 Register Low	INTPND1L1	INTPND11	R
0008A1 _H	CAN1 - Interrupt Pending 1 Register High	INTPND1H1		R
0008A2 _H	CAN1 - Interrupt Pending 2 Register Low	INTPND2L1	INTPND21	R
0008A3 _H	CAN1 - Interrupt Pending 2 Register High	INTPND2H1		R
0008A4 _H -0008AF _H	Reserved			-
0008B0 _H	CAN1 - Message Valid 1 Register Low	MSGVAL1L1	MSGVAL11	R
0008B1 _H	CAN1 - Message Valid 1 Register High	MSGVAL1H1		R
0008B2 _H	CAN1 - Message Valid 2 Register Low	MSGVAL2L1	MSGVAL21	R
0008B3 _H	CAN1 - Message Valid 2 Register High	MSGVAL2H1		R
0008B4 _H -0008CD _H	Reserved			-
0008CE _H	CAN1 - Output enable register	COER1		R/W
0008CF _H -0009FF _H	Reserved			-
000A00 _H	DMA - IO address block register 0	IOABK0		R/W
000A01 _H	DMA - IO address block register 1	IOABK1		R/W
000A02 _H	DMA - IO address block register 2	IOABK2		R/W
000A03 _H	DMA - IO address block register 3	IOABK3		R/W
000A04 _H	DMA - IO address block register 4	IOABK4		R/W
000A05 _H	DMA - IO address block register 5	IOABK5		R/W
000A06 _H -000BFF _H	Reserved			-

Note: Any write access to reserved addresses in the I/O map should not be performed. A read access to a reserved address results in reading 'X'. Registers of resources which are described in this table, but which are not supported by the device, should also be handled as "Reserved".

Table 5: Interrupt vector table MB96(F)34x

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
30	384 _H	EXTINT13	Yes	30	External Interrupt 13
31	380 _H	EXTINT14	Yes	31	External Interrupt 14
32	37C _H	EXTINT15	Yes	32	External Interrupt 15
33	378 _H	CAN0	No	33	CAN Controller 0 (except MB96(F)34xAyy or MB96(F)34xCyy)
34	374 _H	CAN1	No	34	CAN Controller 1 (except MB96(F)34xAyy, MB96(F)34xCyy, MB96F345Dyy or MB96F345Fyy)
35	370 _H	PPG0	Yes	35	Programmable Pulse Generator 0
36	36C _H	PPG1	Yes	36	Programmable Pulse Generator 1
37	368 _H	PPG2	Yes	37	Programmable Pulse Generator 2
38	364 _H	PPG3	Yes	38	Programmable Pulse Generator 3
39	360 _H	PPG4	Yes	39	Programmable Pulse Generator 4
40	35C _H	PPG5	Yes	40	Programmable Pulse Generator 5
41	358 _H	PPG6	Yes	41	Programmable Pulse Generator 6
42	354 _H	PPG7	Yes	42	Programmable Pulse Generator 7
43	350 _H	PPG8	Yes	43	Programmable Pulse Generator 8
44	34C _H	PPG9	Yes	44	Programmable Pulse Generator 9
45	348 _H	PPG10	Yes	45	Programmable Pulse Generator 10
46	344 _H	PPG11	Yes	46	Programmable Pulse Generator 11
47	340 _H	PPG12	Yes	47	Programmable Pulse Generator 12
48	33C _H	PPG13	Yes	48	Programmable Pulse Generator 13
49	338 _H	PPG14	Yes	49	Programmable Pulse Generator 14
50	334 _H	PPG15	Yes	50	Programmable Pulse Generator 15
51	330 _H	RLT0	Yes	51	Reload Timer 0
52	32C _H	RLT1	Yes	52	Reload Timer 1
53	328 _H	RLT2	Yes	53	Reload Timer 2
54	324 _H	RLT3	Yes	54	Reload Timer 3
55	320 _H	PPGRLT	Yes	55	Reload Timer 6 - dedicated for PPG
56	31C _H	ICU0	Yes	56	Input Capture Unit 0
57	318 _H	ICU1	Yes	57	Input Capture Unit 1
58	314 _H	ICU2	Yes	58	Input Capture Unit 2
59	310 _H	ICU3	Yes	59	Input Capture Unit 3

Table 5: Interrupt vector table MB96(F)34x

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
90	294 _H	LINT7	Yes	90	LIN USART 7 TX
91	290 _H	LINR8	Yes	91	LIN USART 8 RX
92	28C _H	LINT8	Yes	92	LIN USART 8 TX
93	288 _H	LINR9	Yes	93	LIN USART 9 RX
94	284 _H	LINT9	Yes	94	LIN USART 9 TX
95	280 _H	RTC0	No	95	Real Timer Clock
96	27C _H	CAL0	No	96	Clock Calibration Unit
97	278 _H	DFLASH_A	Yes	97	Data Flash A (only MB96F345Dyy, MB96F345Fyy)

13.7 Crystal oscillator and ceramic resonator circuit

Noise at X0, X1 pins or X0A, X1A pins might cause abnormal operation. It is required to provide bypass capacitors with shortest possible distance to X0, X1 pins and X0A, X1A pins, crystal oscillator (or ceramic resonator) and ground lines, and, to the utmost effort, that the lines of oscillation circuit do not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board artwork surrounding X0, X1 pins and X0A, X1A pins with a ground area for stabilizing the operation.

It is highly recommended to evaluate the quartz/MCU or resonator/MCU system at the quartz or resonator manufacturer, especially when using low-Q resonators at higher frequencies.

13.8 Turn on sequence of power supply to A/D converter and analog inputs

It is required to turn the A/D converter power supply (AV_{CC} , $AVRH$, $AVRL$) and analog inputs (ANn) on after turning the digital power supply (V_{CC}) on.

It is also required to turn the digital power off after turning the A/D converter supply and analog inputs off. In this case, the voltage must not exceed $AVRH$ or AV_{CC} (turning the analog and digital power supplies simultaneously on or off is acceptable).

13.9 Pin handling when not using the A/D converter

It is required to connect the unused pins of the A/D converter as $AV_{CC} = V_{CC}$, $AV_{SS} = AVRH = AVRL = V_{SS}$.

13.10 Notes on Power-on

To prevent malfunction of the internal voltage regulator, supply voltage profile while turning the power supply on should be slower than 50 μ s from 0.2 V to 2.7 V.

13.11 Stabilization of power supply voltage

If the power supply voltage varies acutely even within the operation safety range of the V_{CC} power supply voltage, a malfunction may occur. The V_{CC} power supply voltage must therefore be stabilized. As stabilization guidelines, the power supply voltage must be stabilized in such a way that V_{CC} ripple fluctuations (peak to peak value) in the commercial frequencies (50 to 60 Hz) fall within 10% of the standard V_{CC} power supply voltage and the transient fluctuation rate becomes 0.1V/ μ s or less in instantaneous fluctuation for power supply switching.

13.12 Serial communication

There is a possibility to receive wrong data due to noise or other causes on the serial communication. Therefore, design a printed circuit board so as to avoid noise. Consider receiving of wrong data when designing the system. For example apply a checksum and retransmit the data if an error occurs.

13.13 Handling of Data Flash

The Data Flash requires different and additional control signals for parallel programming. Please check with your programming equipment maker for support of this interface.

14. Electrical Characteristics

14.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	
	AV_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$V_{CC} = AV_{CC}$ ^[1]
AD Converter voltage references	AVRH, AVRL	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$AV_{CC} \geq AVRH$, $AV_{CC} \geq AVRL$, $AVRH > AVRL$, $AVRL \geq AV_{SS}$
Input voltage	V_I	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$V_I \leq V_{CC} + 0.3V$ ^[2]
Output voltage	V_O	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$V_O \leq V_{CC} + 0.3V$ ^[2]
Maximum Clamp Current	I_{CLAMP}	-4.0	+4.0	mA	Applicable to general purpose I/O pins ^[3]
Total Maximum Clamp Current	$\Sigma I_{CLAMP} $	-	40	mA	Applicable to general purpose I/O pins ^[3]
"L" level maximum output current	I_{OL1}	-	15	mA	Normal outputs with driving strength set to 5mA
"L" level average output current	I_{OLAV1}	-	5	mA	Normal outputs with driving strength set to 5mA
"L" level maximum overall output current	ΣI_{OL1}	-	100	mA	Normal outputs
"L" level average overall output current	ΣI_{OLAV1}	-	50	mA	Normal outputs
"H" level maximum output current	I_{OH1}	-	-15	mA	Normal outputs with driving strength set to 5mA
"H" level average output current	I_{OHAV1}	-	-5	mA	Normal outputs with driving strength set to 5mA
"H" level maximum overall output current	ΣI_{OH1}	-	-100	mA	Normal outputs
"H" level average overall output current	ΣI_{OHAV1}	-	-50	mA	Normal outputs
Permitted Power dissipation (Flash devices in QFP package) ^[4]	P_D	-	430 ^[5]	mW	$T_A = 105^\circ C$
		-	750 ^[5]	mW	$T_A = 90^\circ C$
		-	540 ^[5]	mW	$T_A = 125^\circ C$, no Flash program/erase ^[6]
Permitted Power dissipation (MB96F346/F347/F348 in LQFP package) ^[4]	P_D	-	375 ^[5]	mW	$T_A = 105^\circ C$
		-	750 ^[5]	mW	$T_A = 85^\circ C$
		-	470 ^[5]	mW	$T_A = 125^\circ C$, no Flash program/erase ^[6]
		-	560 ^[5]	mW	$T_A = 120^\circ C$, no Flash program/erase ^[6]
Permitted Power dissipation (MB96F345 in LQFP package) ^[4]	P_D	-	335 ^[5]	mW	$T_A = 105^\circ C$
		-	670 ^[5]	mW	$T_A = 85^\circ C$
		-	840 ^[5]	mW	$T_A = 75^\circ C$
		-	420 ^[5]	mW	$T_A = 125^\circ C$, no Flash program/erase ^[6]
		-	590 ^[5]	mW	$T_A = 115^\circ C$, no Flash program/erase ^[6]

14.3 DC characteristics

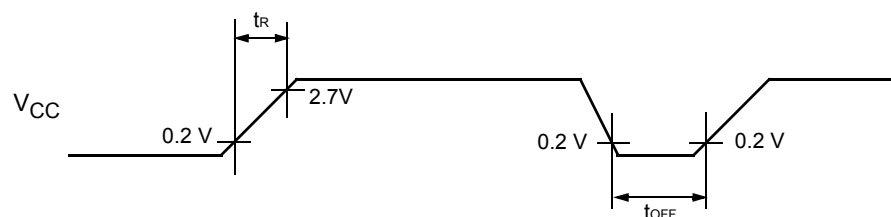
($T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = 0\text{V}$)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input H voltage	V_{IH}	Port inputs Pnn_m	CMOS Hysteresis 0.8/0.2 input selected	$0.8 V_{CC}$	-	$V_{CC} + 0.3$	V	
			CMOS Hysteresis 0.7/0.3 input selected	$0.7 V_{CC}$	-	$V_{CC} + 0.3$	V	$V_{CC} \geq 4.5\text{V}$
			AUTOMOTIVE Hys- teresis input selected	$0.74 V_{CC}$	-	$V_{CC} + 0.3$	V	$V_{CC} < 4.5\text{V}$
			TTL input selected	2.0	-	$V_{CC} + 0.3$	V	
	V_{IHX0F}	X0	External clock in "Fast Clock Input mode"	$0.8 V_{CC}$	-	$V_{CC} + 0.3$	V	Not available in MB96F34xY/R/AxA
	V_{IHX0S}	X0,X1, X0A,X1A	External clock in "oscil- lation mode"	2.5	-	$V_{CC} + 0.3$	V	
	V_{IHR}	RSTX	-	$0.8 V_{CC}$	-	$V_{CC} + 0.3$	V	CMOS Hysteresis input
	V_{IHM}	MD2-MD0	-	$V_{CC} - 0.3$	-	$V_{CC} + 0.3$	V	
Input L voltage	V_{IL}	Port inputs Pnn_m	CMOS Hysteresis 0.8/0.2 input selected	$V_{SS} - 0.3$	-	$0.2 V_{CC}$	V	
			CMOS Hysteresis 0.7/0.3 input selected	$V_{SS} - 0.3$	-	$0.3 V_{CC}$	V	
			AUTOMOTIVE Hys- teresis input selected	$V_{SS} - 0.3$	-	$0.5 V_{CC}$	V	$V_{CC} \geq 4.5\text{V}$
			TTL input selected	$V_{SS} - 0.3$	-	0.8	V	$V_{CC} < 4.5\text{V}$
	V_{ILX0F}	X0	External clock in "Fast Clock Input mode"	$V_{SS} - 0.3$	-	$0.2 V_{CC}$	V	Not available in MB96F34xY/R/AxA
	V_{ILX0S}	X0,X1, X0A,X1A	External clock in "oscillation mode"	$V_{SS} - 0.3$	-	0.4	V	
	V_{ILR}	RSTX	-	$V_{SS} - 0.3$	-	$0.2 V_{CC}$	V	CMOS Hysteresis input
	V_{ILM}	MD2-MD0	-	$V_{SS} - 0.3$	-	$V_{SS} + 0.3$	V	
Output H voltage	V_{OH2}	Normal outputs	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $I_{OH} = -2\text{mA}$	$V_{CC} - 0.5$	-	-	V	Driving strength set to 2mA
			$3.0\text{V} \leq V_{CC} < 4.5\text{V}$ $I_{OH} = -1.6\text{mA}$					
	V_{OH5}	Normal outputs	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $I_{OH} = -5\text{mA}$	$V_{CC} - 0.5$	-	-	V	Driving strength set to 5mA
			$3.0\text{V} \leq V_{CC} < 4.5\text{V}$ $I_{OH} = -3\text{mA}$					
	V_{OH3}	3mA outputs	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $I_{OH} = -3\text{mA}$	$V_{CC} - 0.5$	-	-	V	
			$3.0\text{V} \leq V_{CC} < 4.5\text{V}$ $I_{OH} = -2\text{mA}$					

14.4.4 Power On Reset timing

($T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = 0\text{V}$)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Power on rise time	t_R	V_{CC}	0.05	-	30	ms	
Power off time	t_{OFF}	V_{CC}	1	-	-	ms	



If the power supply is changed too rapidly, a power-on reset may occur.
 We recommend a smooth startup by restraining voltages when changing the power supply voltage during operation, as shown in the figure below.



($T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $I_{O\text{drive}} = 5\text{mA}$, $C_L = 50\text{pF}$)

Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
RDX $\uparrow \Rightarrow$ ALE $\uparrow$ time	t_{RHLH}	RDX, ALE	EACL:STS=1 and EACL:ACE=1	$3t_{\text{CYC}}/2 - 10$	-	ns	
			other ECL:STS, EACL:ACE setting	$t_{\text{CYC}}/2 - 10$	-		
Valid address $\Rightarrow$ ECLK $\uparrow$ time	t_{AVCH}	A[23:16], ECLK	-	$t_{\text{CYC}} - 15$	-	ns	
	t_{ADVCH}	AD[15:0], ECLK		$t_{\text{CYC}}/2 - 15$	-		
RDX $\downarrow \Rightarrow$ ECLK $\uparrow$ time	t_{RLCH}	RDX, ECLK	-	$t_{\text{CYC}}/2 - 10$	-	ns	
ALE $\downarrow \Rightarrow$ RDX $\downarrow$ time	t_{LLRL}	ALE, RDX	EACL:STS=0	$t_{\text{CYC}}/2 - 10$	-	ns	
			EACL:STS=1	- 10	-		
ECLK $\uparrow \Rightarrow$ Valid data input	t_{CHDV}	AD[15:0], ECLK	-	-	$t_{\text{CYC}} - 50$	ns	

($T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 3.0$ to 4.5V , $V_{SS} = 0.0\text{ V}$, $I_{O\text{drive}} = 5\text{mA}$, $C_L = 50\text{pF}$)

Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
ALE pulse width	t _{LHLL}	ALE	EACL:STS=0 and EACL:ACE=0	t _{CYC} /2 – 8	-	ns	
			EACL:STS=1	t _{CYC} – 8	-		
			EACL:STS=0 and EACL:ACE=1	3t _{CYC} /2 – 8	-		
Valid address ⇒ ALE ↓ time	t _{AVLL}	ALE, A[23:16],	EACL:STS=0 and EACL:ACE=0	t _{CYC} – 20	-	ns	
			EACL:STS=1 and EACL:ACE=0	3t _{CYC} /2 – 20	-		
			EACL:STS=0 and EACL:ACE=1	2t _{CYC} – 20	-		
			EACL:STS=1 and EACL:ACE=1	5t _{CYC} /2 – 20	-		
	t _{ADVLL}	ALE, AD[15:0]	EACL:STS=0 and EACL:ACE=0	t _{CYC} /2 – 20	-	ns	
			EACL:STS=1 and EACL:ACE=0	t _{CYC} – 20	-		
			EACL:STS=0 and EACL:ACE=1	3t _{CYC} /2 – 20	-		
			EACL:STS=1 and EACL:ACE=1	2t _{CYC} – 20	-		
ALE ↓ ⇒ Address valid time	t _{LLAX}	ALE, AD[15:0]	EACL:STS=0	t _{CYC} /2 – 20	-	ns	
			EACL:STS=1	-20	-		
Valid address ⇒ RDX ↓ time	t _{AVRL}	RDX, A[23:16]	EACL:ACE=0	3t _{CYC} /2 – 20	-	ns	
			EACL:ACE=1	5t _{CYC} /2 – 20	-		
	t _{ADVRL}	RDX, AD[15:0]	EACL:ACE=0	t _{CYC} – 20	-	ns	
			EACL:ACE=1	2t _{CYC} – 20	-		

($T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 3.0$ to 4.5V , $V_{SS} = 0.0\text{V}$, $I_{Odrive} = 5\text{mA}$, $C_L = 50\text{pF}$)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
WRX pulse width	t_{WLWH}	WRX, WRXL, WRHX	-	$t_{CYC} - 8$	-	ns	w/o cycle extension
Valid data output $\Rightarrow$ WRX $\uparrow$ time	t_{DVWH}	WRX, WRLX, WRHX, AD[15:0]	-	$t_{CYC} - 25$	-	ns	w/o cycle extension
WRX $\uparrow \Rightarrow$ Data hold time	t_{WHDX}	WRX, WRLX, WRHX, AD[15:0]	-	$t_{CYC}/2 - 20$	-	ns	
WRX $\uparrow \Rightarrow$ Address valid time	t_{WHAX}	WRX, WRLX, WRHX, A[23:16]	-	$t_{CYC}/2 - 20$	-	ns	
WRX $\uparrow \Rightarrow$ ALE $\uparrow$ time	t_{WHLH}	WRX, WRLX, WRHX, ALE	EBM:ACE=1 and EACL:STS=1	$2t_{CYC} - 15$	-	ns	
			other EBM:ACE and EACL:STS setting	$t_{CYC} - 15$	-		
WRX $\downarrow \Rightarrow$ ECLK $\uparrow$ time	t_{WLCH}	WRX, WRLX, WRHX, ECLK	-	$t_{CYC}/2 - 15$	-	ns	
CSn $\Rightarrow$ WRX time	t_{CSLWL}	WRX, WRLX, WRHX, CSn	EACL:ACE=0	-	$3t_{CYC}/2 - 20$	ns	
			EACL:ACE=1	-	$5t_{CYC}/2 - 20$		
WRX $\Rightarrow$ CSn time	t_{WHCSH}	WRX, WRLX, WRHX, CSn	-	$t_{CYC}/2 - 20$	-	ns	

14.7 Low Voltage Detector Characteristics

($T_A = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$, $V_{CC} = AV_{CC} = 3.0\text{V} - 5.5\text{V}$, $V_{SS} = AV_{SS} = 0\text{V}$)

Parameter	Symbol	Value [1]		Value [2]		Unit	Remarks
		Min	Max	Min	Max		
Stabilization time	$T_{LVDSTAB}$	-	75	-	110	μs	After power-up or change of detection level
Level 0	V_{DL0}	2.7	2.9	2.65	2.95	V	CILCR:LVL[3:0]="0000"
Level 1	V_{DL1}	2.9	3.1	2.85	3.2	V	CILCR:LVL[3:0]="0001"
Level 2	V_{DL2}	3.1	3.3	3.05	3.4	V	CILCR:LVL[3:0]="0010"
Level 3	V_{DL3}	3.5	3.75	3.45	3.85	V	CILCR:LVL[3:0]="0011"
Level 4	V_{DL4}	3.6	3.85	3.55	3.95	V	CILCR:LVL[3:0]="0100"
Level 5	V_{DL5}	3.7	3.95	3.65	4.1	V	CILCR:LVL[3:0]="0101"
Level 6	V_{DL6}	3.8	4.05	3.75	4.2	V	CILCR:LVL[3:0]="0110"
Level 7	V_{DL7}	3.9	4.15	3.85	4.3	V	CILCR:LVL[3:0]="0111"
Level 8	V_{DL8}	4.0	4.25	3.95	4.4	V	CILCR:LVL[3:0]="1000"
Level 9	V_{DL9}	4.1	4.35	4.05	4.5	V	CILCR:LVL[3:0]="1001"
Level 10	V_{DL10}	not used		not used			
Level 11	V_{DL11}	not used		not used			
Level 12	V_{DL12}	not used		not used			
Level 13	V_{DL13}	not used		not used			
Level 14	V_{DL14}	not used		not used			
Level 15	V_{DL15}	not used		not used			

[1]: valid for all devices except devices listed under "[2]"

[2]: valid for: MB96F345

CILCR:LVL[3:0] are the low voltage detector level select bits of the CILCR register.

Levels 10 to 15 are not used in this device.

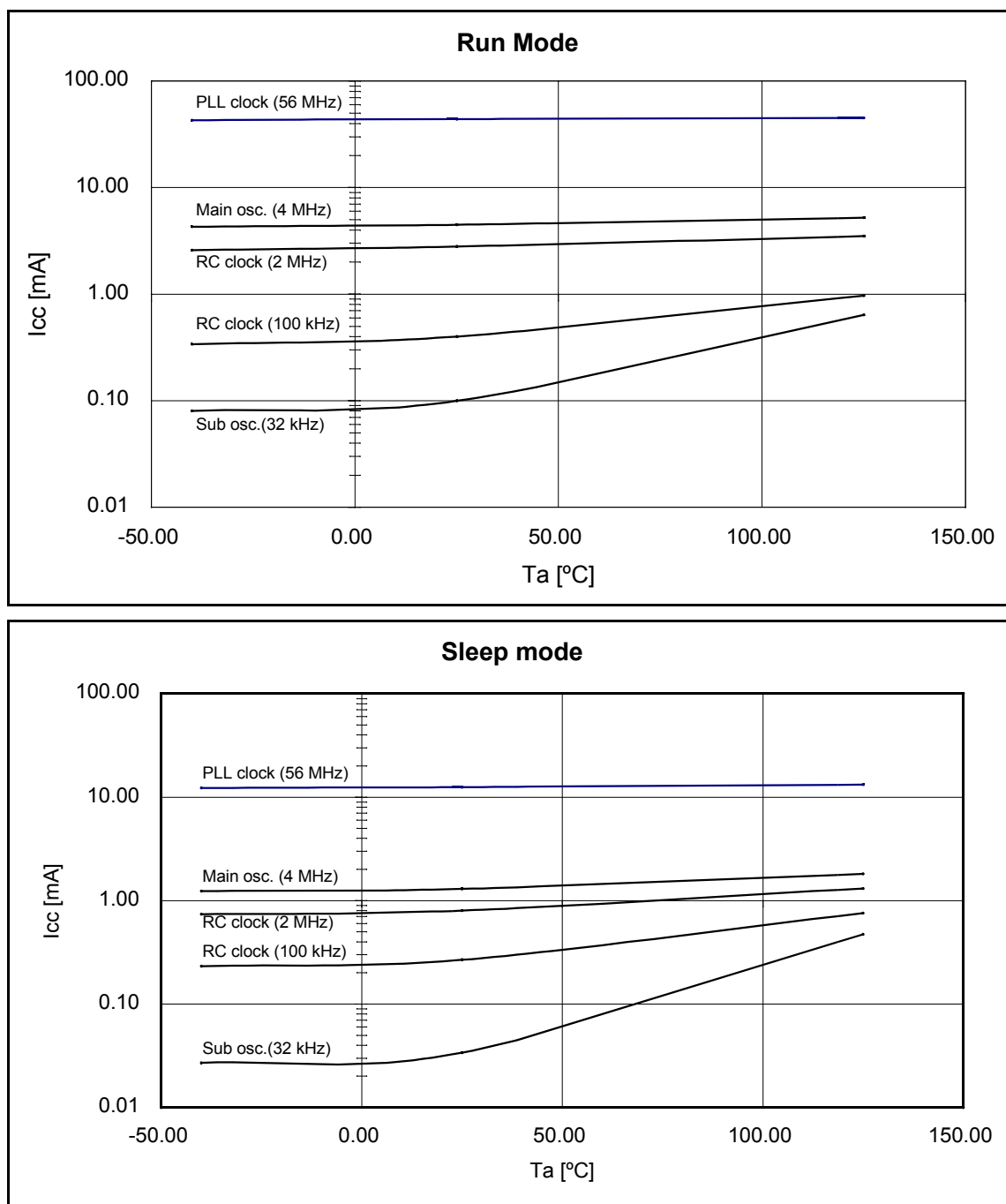
For correct detection, the slope of the voltage level must satisfy $\left| \frac{dV}{dt} \right| \leq 0.004 \frac{V}{\mu\text{s}}$.

Faster variations are regarded as noise and may not be detected.

The functional operation of the MCU is guaranteed down to the minimum low voltage detection level of $V_{CC} = 2.7\text{V}$. The electrical characteristics however are only valid in the specified range (usually down to 3.0V).

15. Example Characteristics

The diagrams below show the characteristics of one measured sample with typical process parameters.



18. Ordering Information

18.1 MCU with CAN Controller

Part number	Flash/ROM	Subclock	Persistent Low Voltage Reset	Package
MB96345YSA PQC-GSE2 ^[1]	ROM (160KB)	No	Yes	100 pin Plastic QFP (FPT-100P-M22)
MB96345RSA PQC-GSE2 ^[1]			No	
MB96345YWA PQC-GSE2 ^[1]		Yes	Yes	
MB96345RWA PQC-GSE2 ^[1]			No	
MB96345YSA PMC-GSE2 ^[1]		No	Yes	100 pin Plastic LQFP (FPT-100P-M20)
MB96345RSA PMC-GSE2 ^[1]			No	
MB96345YWA PMC-GSE2 ^[1]		Yes	Yes	
MB96345RWA PMC-GSE2 ^[1]			No	
MB96346YSA PQC-GSE2 ^[1]	ROM (288KB)	No	Yes	100 pin Plastic QFP (FPT-100P-M22)
MB96346RSA PQC-GSE2 ^[1]			No	
MB96346YWA PQC-GSE2 ^[1]		Yes	Yes	
MB96346RWA PQC-GSE2 ^[1]			No	
MB96346YSA PMC-GSE2 ^[1]		No	Yes	100 pin Plastic LQFP (FPT-100P-M20)
MB96346RSA PMC-GSE2 ^[1]			No	
MB96346YWA PMC-GSE2 ^[1]		Yes	Yes	
MB96346RWA PMC-GSE2 ^[1]			No	
MB96F345FSA PQC-GSE2 ^[1]	Flash A (160KB) Data Flash A (64KB)	No	Yes	100 pin Plastic QFP (FPT-100P-M22)
MB96F345DSA PQC-GSE2 ^[1]			No	
MB96F345FWA PQC-GSE2 ^[1]		Yes	Yes	
MB96F345DWA PQC-GSE2 ^[1]			No	
MB96F345FSA PMC-GSE2 ^[1]		No	Yes	100 pin Plastic LQFP (FPT-100P-M20)
MB96F345DSA PMC-GSE2 ^[1]			No	
MB96F345FWA PMC-GSE2 ^[1]		Yes	Yes	
MB96F345DWA PMC-GSE2 ^[1]			No	
MB96F346YSB PQC-GSE2	Flash A (288KB)	No	Yes	100 pin Plastic QFP (FPT-100P-M22)
MB96F346RSB PQC-GSE2			No	
MB96F346YWB PQC-GSE2		Yes	Yes	
MB96F346RWB PQC-GSE2			No	
MB96F346YSB PMC-GSE2		No	Yes	100 pin Plastic LQFP (FPT-100P-M20)
MB96F346RSB PMC-GSE2			No	
MB96F346YWB PMC-GSE2		Yes	Yes	
MB96F346RWB PMC-GSE2			No	

19. Revision History

Revision	Date	Modification
Prelim 1	2007-05-07	Creation
Prelim 2	2007-05-10	External bus hold timing update
Prelim 3	2007-05-23	Electrical characteristics updates
Prelim 4	2007-08-02	Electrical characteristics updates, Product lineup, changes and ordering information
Prelim 5	2007-09-12	Addition of the electrical characteristic examples and the LVD characteristics specifications, updates of the DC characteristics. Pin circuit type drawing modifications.
Prelim 6	2007-11-21	LVD typo correction. Update of the DC characteristics. Typos corrections.
Prelim 7	2007-12-04	Absolute maximum rating asterisks numbering corrected. Typos page 59: Hardware -> Hardware. IO map table regenerated. Typos corrections. IO circuit drawings modified. Renaming of the Main/Satellite Flash into Flash memory A/B. Memory map reworked.
Prelim 8	2008-02-04	■ Satellite Flash -> 32kB Data Flash ■ MB96345 added (under development) ■ MB96F348 TSA/HSA/TWA/HWA removed (outdated devices) ■ Block diagram and pin assignment corrected (existing resource pins) ■ Pin function table corrected ■ I/O circuit type diagrams corrected ■ Memory map cleaned up ■ "Flash sector configuration" replaced by corrected "User ROM Memory map for Flash devices", "ROM configuration" replaced by "User ROM Memory map for Mask ROM devices" ■ Parallel Flash programming pinning removed ■ IO map table regenerated: □ Port register: Naming style corrected □ Memory control registers renamed (Main/Sat -> A/B) □ addresses after 000BFFh removed ■ Absolute maximum ratings: Pd and Ta specified more precisely ■ oscillator input levels in oscillation mode with external clock added ■ Run and Sleep mode currents: 96/48MHz and 72/36MHz settings added ■ Run mode current spec in 48/24MHz mode corrected ■ Maximum CLKS1/2 frequency for all devices correctly specified ■ Maximum CLKP2 for MB96F34xY/R/Axx corrected ■ External bus timings: missing conditions added and readability improved ■ Alarm comparator spec updated (transition voltages defined) ■ MB96V300A removed ■ Ordering information updated ■ Typos and formatting corrected