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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

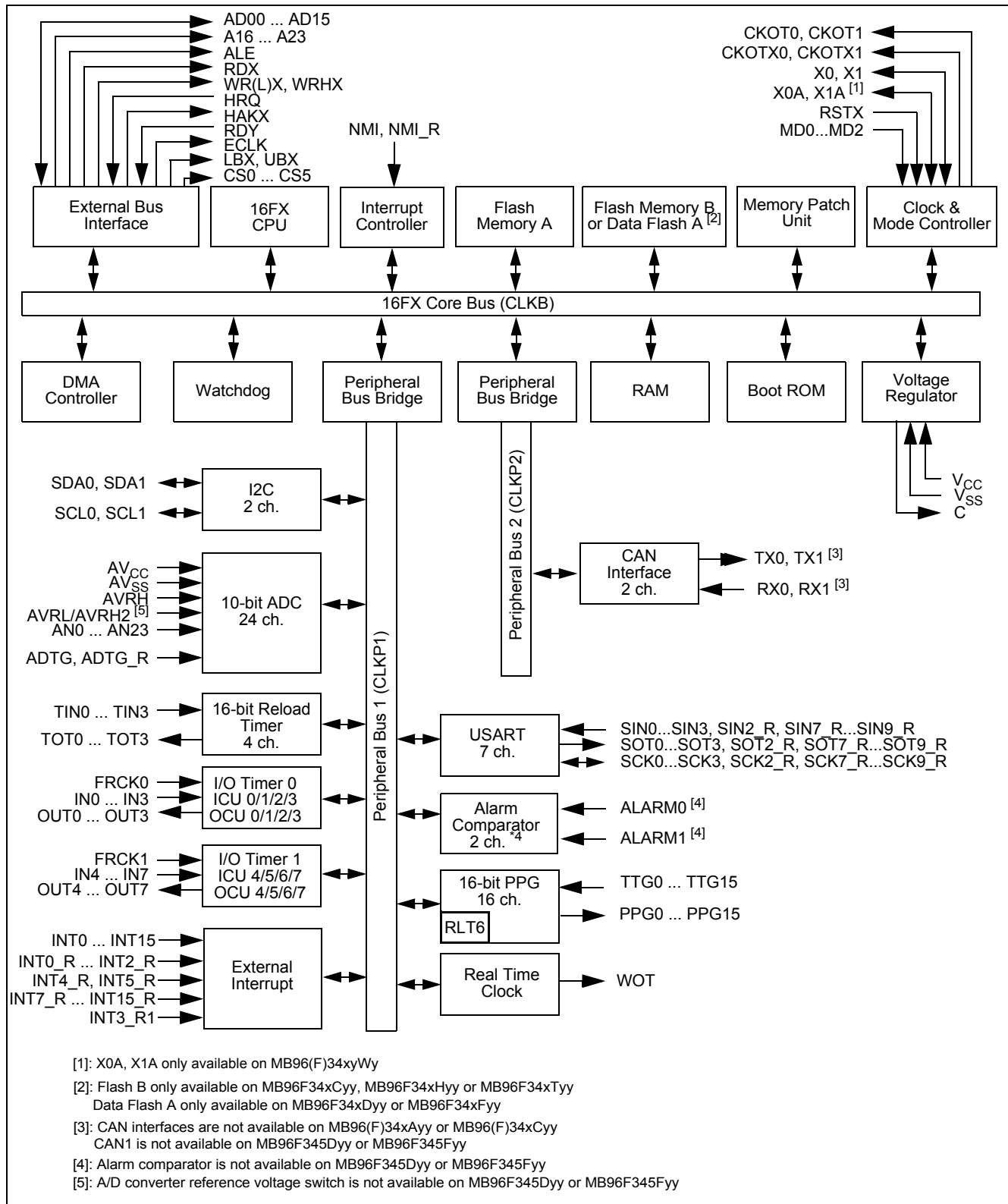
Applications of "[Embedded - Microcontrollers](#)"

Details

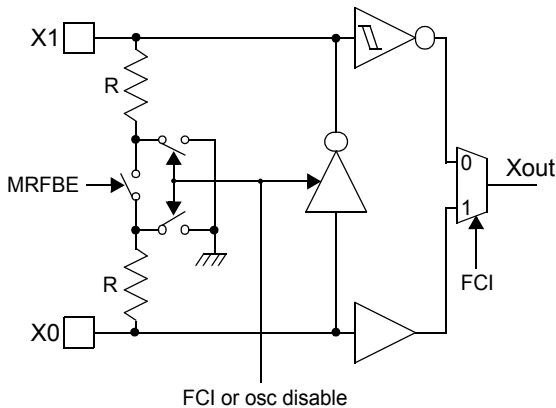
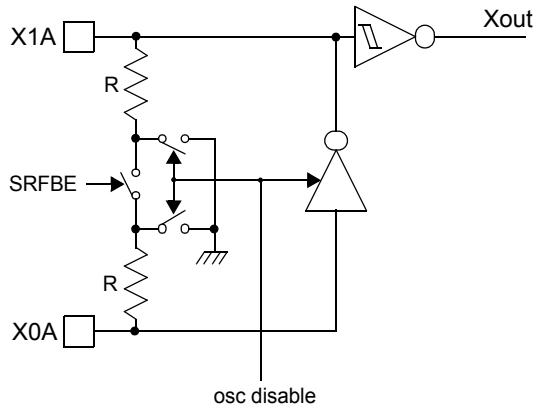
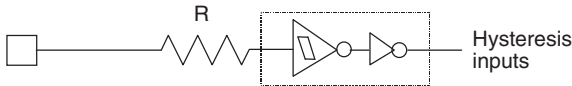
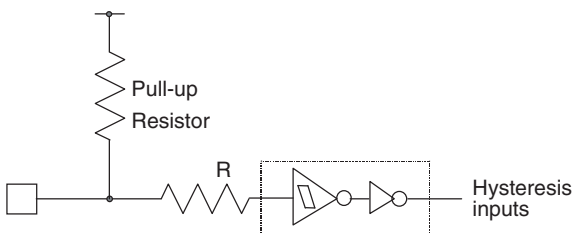
Product Status	Active
Core Processor	F ² MC-16FX
Core Size	16-Bit
Speed	56MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, LVR, POR, PWM, WDT
Number of I/O	82
Program Memory Size	576KB (576K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-PQFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f348hsbpqc-gse2

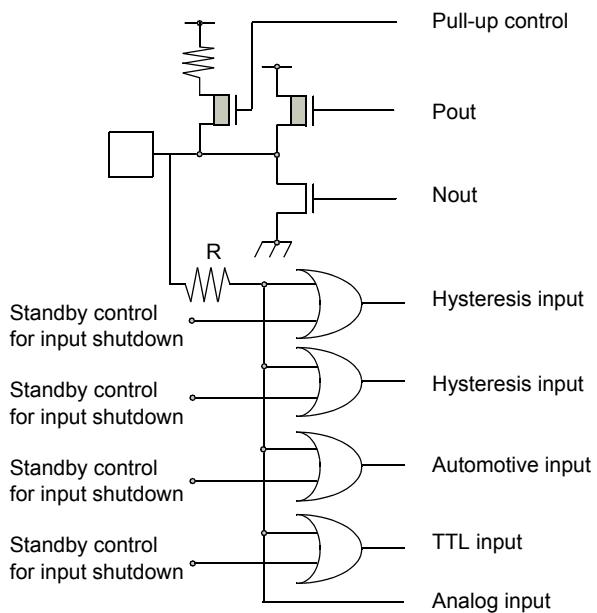
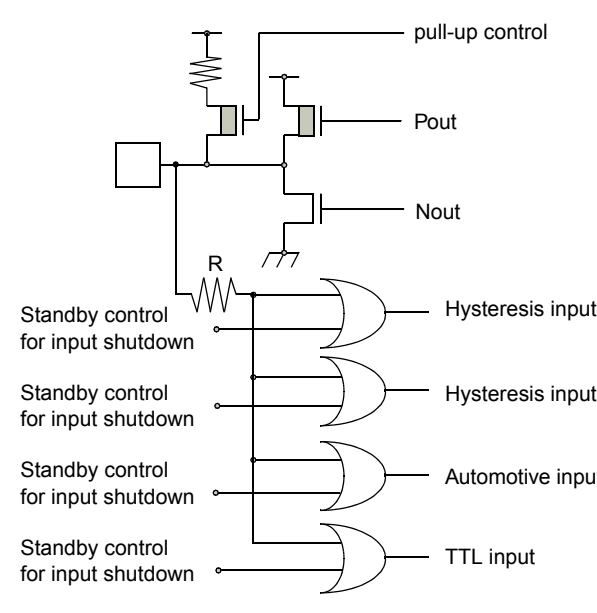
2. Block Diagram

Figure 1. Block diagram of MB96(F)34x



6. I/O Circuit Type

Type	Circuit	Remarks
A		High-speed oscillation circuit: ■ Programmable between oscillation mode (external crystal or resonator connected to X0/X1 pins) and Fast external Clock Input (FCI) mode (external clock connected to X0 pin) ■ Programmable feedback resistor = approx. $2 * 0.5 \text{ M}\Omega$. Feedback resistor is grounded in the center when the oscillator is disabled or in FCI mode
B		Low-speed oscillation circuit: ■ Programmable feedback resistor = approx. $2 * 5 \text{ M}\Omega$. Feedback resistor is grounded in the center when the oscillator is disabled
C		■ Mask ROM and EVA device: CMOS Hysteresis input pin ■ Flash device: CMOS input pin
E		■ CMOS Hysteresis input pin ■ Pull-up resistor value: approx. $50 \text{ k}\Omega$

Type	Circuit	Remarks
I	 Pull-up control Pout Nout R Standby control for input shutdown Hysteresis input Hysteresis input Automotive input TTL input Analog input	■ CMOS level output (programmable $I_{OL} = 5\text{mA}$, $I_{OH} = -5\text{mA}$ and $I_{OL} = 2\text{mA}$, $I_{OH} = -2\text{mA}$) ■ 2 different CMOS hysteresis inputs with input shutdown function * ■ Automotive input with input shutdown function ■ TTL input with input shutdown function * ■ Programmable pull-up resistor: 50kΩ approx. ■ Analog input *MB96F345Dyy or MB96F345Fyy: Only Automotive input and CMOS hysteresis input (0.7/0.3) are supported
N	 pull-up control Pout Nout R Standby control for input shutdown Hysteresis input Hysteresis input Automotive input TTL input	■ CMOS level output ($I_{OL} = 3\text{mA}$, $I_{OH} = -3\text{mA}$) ■ 2 different CMOS hysteresis inputs with input shutdown function * ■ Automotive input with input shutdown function ■ TTL input with input shutdown function * ■ Programmable pull-up resistor: 50kΩ approx. *MB96F345Dyy or MB96F345Fyy: Only Automotive input and CMOS hysteresis input (0.7/0.3) are supported

		MB96F348Y MB96F348R MB96F348A	MB96F348T MB96F348H MB96F348C	
Alternative mode CPU address	Flash memory mode address	Flash size 544kByte	Flash size 576kByte	
FF:FFFF _H	3F:FFFF _H	S39 - 64K	S39 - 64K	Flash A
FF:0000 _H	3F:0000 _H			
FE:FFFF _H	3E:FFFF _H	S38 - 64K	S38 - 64K	
FE:0000 _H	3E:0000 _H			
FD:FFFF _H	3D:FFFF _H	S37 - 64K	S37 - 64K	
FD:0000 _H	3D:0000 _H			
FC:FFFF _H	3C:FFFF _H	S36 - 64K	S36 - 64K	
FC:0000 _H	3C:0000 _H			
FB:FFFF _H	3B:FFFF _H	S35 - 64K	S35 - 64K	
FB:0000 _H	3B:0000 _H			
FA:FFFF _H	3A:FFFF _H	S34 - 64K	S34 - 64K	
FA:0000 _H	3A:0000 _H			
F9:FFFF _H	39:FFFF _H	S33 - 64K	S33 - 64K	
F9:0000 _H	39:0000 _H			
F8:FFFF _H	38:FFFF _H	S32 - 64K	S32 - 64K	
F8:0000 _H	38:0000 _H			
F7:FFFF _H	37:FFFF _H			
F7:0000 _H	37:0000 _H			
F6:FFFF _H	36:FFFF _H			
F6:0000 _H	36:0000 _H			
F5:FFFF _H	35:FFFF _H			
F5:0000 _H	35:0000 _H			
F4:FFFF _H	34:FFFF _H			
F4:0000 _H	34:0000 _H			
F3:FFFF _H	33:FFFF _H	External bus	External bus	
F3:0000 _H	33:0000 _H			
F2:FFFF _H	32:FFFF _H			
F2:0000 _H	32:0000 _H			
F1:FFFF _H	31:FFFF _H			
F1:0000 _H	31:0000 _H			
F0:FFFF _H	30:FFFF _H			
F0:0000 _H	30:0000 _H			
E0:FFFF _H				
E0:0000 _H				
DF:FFFF _H		Reserved	Reserved	
DF:8000 _H				
DF:7FFF _H	1F:7FFF _H	SA3 - 8K	SA3 - 8K	Flash A
DF:6000 _H	1F:6000 _H			
DF:5FFF _H	1F:5FFF _H	SA2 - 8K	SA2 - 8K	
DF:4000 _H	1F:4000 _H			
DF:3FFF _H	1F:3FFF _H	SA1 - 8K	SA1 - 8K	
DF:2000 _H	1F:2000 _H			
DF:1FFF _H	1F:1FFF _H	SA0 - 8K [1]	SA0 - 8K [1]	
DF:0000 _H	1F:0000 _H			
DE:FFFF _H				
DE:8000 _H				

11. I/O Map

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000000 _H	I/O Port P00 - Port Data Register	PDR00		R/W
000001 _H	I/O Port P01 - Port Data Register	PDR01		R/W
000002 _H	I/O Port P02 - Port Data Register	PDR02		R/W
000003 _H	I/O Port P03 - Port Data Register	PDR03		R/W
000004 _H	I/O Port P04 - Port Data Register	PDR04		R/W
000005 _H	I/O Port P05 - Port Data Register	PDR05		R/W
000006 _H	I/O Port P06 - Port Data Register	PDR06		R/W
000007 _H	I/O Port P07 - Port Data Register	PDR07		R/W
000008 _H	I/O Port P08 - Port Data Register	PDR08		R/W
000009 _H	I/O Port P09 - Port Data Register	PDR09		R/W
00000A _H	I/O Port P10 - Port Data Register	PDR10		R/W
00000B _H -000017 _H	Reserved			-
000018 _H	ADC0 - Control Status register Low	ADCSL	ADCS	R/W
000019 _H	ADC0 - Control Status register High	ADCSH		R/W
00001A _H	ADC0 - Data Register Low	ADCRL	ADCR	R
00001B _H	ADC0 - Data Register High	ADCRH		R
00001C _H	ADC0 - Setting Register		ADSR	R/W
00001D _H	ADC0 - Setting Register			R/W
00001E _H	ADC0 - Extended Configuration Register	ADECR		R/W
00001F _H	Reserved			-
000020 _H	FRT0 - Data register of free-running timer		TCDT0	R/W
000021 _H	FRT0 - Data register of free-running timer			R/W
000022 _H	FRT0 - Control status register of free-running timer Low	TCCSL0	TCCS0	R/W
000023 _H	FRT0 - Control status register of free-running timer High	TCCSH0		R/W
000024 _H	FRT1 - Data register of free-running timer		TCDT1	R/W
000025 _H	FRT1 - Data register of free-running timer			R/W
000026 _H	FRT1 - Control status register of free-running timer Low	TCCSL1	TCCS1	R/W
000027 _H	FRT1 - Control status register of free-running timer High	TCCSH1		R/W
000028 _H	OCU0 - Output Compare Control Status	OCS0		R/W
000029 _H	OCU1 - Output Compare Control Status	OCS1		R/W
00002A _H	OCU0 - Compare Register		OCCP0	R/W

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0000A1 _H	PPG4 - Duty cycle register			W
0000A2 _H	PPG4 - Control status register Low	PCNL4	PCN4	R/W
0000A3 _H	PPG4 - Control status register High	PCNH4		R/W
0000A4 _H	PPG5 - Timer register		PTMR5	R
0000A5 _H	PPG5 - Timer register			R
0000A6 _H	PPG5 - Period setting register		PCSR5	W
0000A7 _H	PPG5 - Period setting register			W
0000A8 _H	PPG5 - Duty cycle register		PDUT5	W
0000A9 _H	PPG5 - Duty cycle register			W
0000AA _H	PPG5 - Control status register Low	PCNL5	PCN5	R/W
0000AB _H	PPG5 - Control status register High	PCNH5		R/W
0000AC _H	I2C0 - Bus Status Register	IBSR0		R
0000AD _H	I2C0 - Bus Control Register	IBCR0		R/W
0000AE _H	I2C0 - Ten bit Slave address Register Low	ITBAL0	ITBA0	R/W
0000AF _H	I2C0 - Ten bit Slave address Register High	ITBAH0		R/W
0000B0 _H	I2C0 - Ten bit Address mask Register Low	ITMKL0	ITMK0	R/W
0000B1 _H	I2C0 - Ten bit Address mask Register High	ITMKH0		R/W
0000B2 _H	I2C0 - Seven bit Slave address Register	ISBA0		R/W
0000B3 _H	I2C0 - Seven bit Address mask Register	ISMK0		R/W
0000B4 _H	I2C0 - Data Register	IDAR0		R/W
0000B5 _H	I2C0 - Clock Control Register	ICCR0		R/W
0000B6 _H	I2C1 - Bus Status Register	IBSR1		R
0000B7 _H	I2C1 - Bus Control Register	IBCR1		R/W
0000B8 _H	I2C1 - Ten bit Slave address Register Low	ITBAL1	ITBA1	R/W
0000B9 _H	I2C1 - Ten bit Slave address Register High	ITBAH1		R/W
0000BA _H	I2C1 - Ten bit Address mask Register Low	ITMKL1	ITMK1	R/W
0000BB _H	I2C1 - Ten bit Address mask Register High	ITMKH1		R/W
0000BC _H	I2C1 - Seven bit Slave address Register	ISBA1		R/W
0000BD _H	I2C1 - Seven bit Address mask Register	ISMK1		R/W
0000BE _H	I2C1 - Data Register	IDAR1		R/W
0000BF _H	I2C1 - Clock Control Register	ICCR1		R/W
0000C0 _H	USART0 - Serial Mode Register	SMR0		R/W

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0000DE _H	USART3 - Serial Mode Register	SMR3		R/W
0000DF _H	USART3 - Serial Control Register	SCR3		R/W
0000E0 _H	USART3 - TX Register	TDR3		W
0000E0 _H	USART3 - RX Register	RDR3		R
0000E1 _H	USART3 - Serial Status	SSR3		R/W
0000E2 _H	USART3 - Control/Com. Register	ECCR3		R/W
0000E3 _H	USART3 - Ext. Status Register	ESCR3		R/W
0000E4 _H	USART3 - Baud Rate Generator Register Low	BGRL3	BGR3	R/W
0000E5 _H	USART3 - Baud Rate Generator Register High	BGRH3		R/W
0000E6 _H	USART3 - Extended Serial Interrupt Register	ESIR3		R/W
0000E7 _H -0000EF _H	Reserved			-
0000F0 _H -0000FF _H	External Bus area	EXTBUS0		R/W
000100 _H	DMA0 - Buffer address pointer low byte	BAPL0		R/W
000101 _H	DMA0 - Buffer address pointer middle byte	BAPM0		R/W
000102 _H	DMA0 - Buffer address pointer high byte	BAPH0		R/W
000103 _H	DMA0 - DMA control register	DMACS0		R/W
000104 _H	DMA0 - I/O register address pointer low byte	IOAL0	IOA0	R/W
000105 _H	DMA0 - I/O register address pointer high byte	IOAH0		R/W
000106 _H	DMA0 - Data counter low byte	DCTL0	DCT0	R/W
000107 _H	DMA0 - Data counter high byte	DCTH0		R/W
000108 _H	DMA1 - Buffer address pointer low byte	BAPL1		R/W
000109 _H	DMA1 - Buffer address pointer middle byte	BAPM1		R/W
00010A _H	DMA1 - Buffer address pointer high byte	BAPH1		R/W
00010B _H	DMA1 - DMA control register	DMACS1		R/W
00010C _H	DMA1 - I/O register address pointer low byte	IOAL1	IOA1	R/W
00010D _H	DMA1 - I/O register address pointer high byte	IOAH1		R/W
00010E _H	DMA1 - Data counter low byte	DCTL1	DCT1	R/W
00010F _H	DMA1 - Data counter high byte	DCTH1		R/W
000110 _H	DMA2 - Buffer address pointer low byte	BAPL2		R/W
000111 _H	DMA2 - Buffer address pointer middle byte	BAPM2		R/W
000112 _H	DMA2 - Buffer address pointer high byte	BAPH2		R/W
000113 _H	DMA2 - DMA control register	DMACS2		R/W

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0003B9 _H	Memory Patch function - Patch address 0 middle	PFAM0		R/W
0003BA _H	Memory Patch function - Patch address 0 high	PFAH0		R/W
0003BB _H	Memory Patch function - Patch address 1 low	PFAL1		R/W
0003BC _H	Memory Patch function - Patch address 1 middle	PFAM1		R/W
0003BD _H	Memory Patch function - Patch address 1 high	PFAH1		R/W
0003BE _H	Memory Patch function - Patch address 2 low	PFAL2		R/W
0003BF _H	Memory Patch function - Patch address 2 middle	PFAM2		R/W
0003C0 _H	Memory Patch function - Patch address 2 high	PFAH2		R/W
0003C1 _H	Memory Patch function - Patch address 3 low	PFAL3		R/W
0003C2 _H	Memory Patch function - Patch address 3 middle	PFAM3		R/W
0003C3 _H	Memory Patch function - Patch address 3 high	PFAH3		R/W
0003C4 _H	Memory Patch function - Patch address 4 low	PFAL4		R/W
0003C5 _H	Memory Patch function - Patch address 4 middle	PFAM4		R/W
0003C6 _H	Memory Patch function - Patch address 4 high	PFAH4		R/W
0003C7 _H	Memory Patch function - Patch address 5 low	PFAL5		R/W
0003C8 _H	Memory Patch function - Patch address 5 middle	PFAM5		R/W
0003C9 _H	Memory Patch function - Patch address 5 high	PFAH5		R/W
0003CA _H	Memory Patch function - Patch address 6 low	PFAL6		R/W
0003CB _H	Memory Patch function - Patch address 6 middle	PFAM6		R/W
0003CC _H	Memory Patch function - Patch address 6 high	PFAH6		R/W
0003CD _H	Memory Patch function - Patch address 7 low	PFAL7		R/W
0003CE _H	Memory Patch function - Patch address 7 middle	PFAM7		R/W
0003CF _H	Memory Patch function - Patch address 7 high	PFAH7		R/W
0003D0 _H	Memory Patch function - Patch data 0 Low	PFDL0	PFD0	R/W
0003D1 _H	Memory Patch function - Patch data 0 High	PFDH0		R/W
0003D2 _H	Memory Patch function - Patch data 1 Low	PFDL1	PFD1	R/W
0003D3 _H	Memory Patch function - Patch data 1 High	PFDH1		R/W
0003D4 _H	Memory Patch function - Patch data 2 Low	PFDL2	PFD2	R/W
0003D5 _H	Memory Patch function - Patch data 2 High	PFDH2		R/W
0003D6 _H	Memory Patch function - Patch data 3 Low	PFDL3	PFD3	R/W
0003D7 _H	Memory Patch function - Patch data 3 High	PFDH3		R/W
0003D8 _H	Memory Patch function - Patch data 4 Low	PFDL4	PFD4	R/W

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000407 _H	PLL Control register High	PLLCRH		R/W
000408 _H	RC clock timer control register	RCTCR		R/W
000409 _H	Main clock timer control register	MCTCR		R/W
00040A _H	Sub clock timer control register	SCTCR		R/W
00040B _H	Reset cause and clock status register with clear function	RCCSRC		R
00040C _H	Reset configuration register	RCR		R/W
00040D _H	Reset cause and clock status register	RCCSR		R
00040E _H	Watch dog timer configuration register	WDTC		R/W
00040F _H	Watch dog timer clear pattern register	WDTCP		W
000410 _H -000414 _H	Reserved			-
000415 _H	Clock output activation register	COAR		R/W
000416 _H	Clock output configuration register 0	COCR0		R/W
000417 _H	Clock output configuration register 1	COCR1		R/W
000418 _H	Clock Modulator control register	CMCR		R/W
000419 _H	Reserved			-
00041A _H	Clock Modulator Parameter register Low	CMPRL	CMPR	R/W
00041B _H	Clock Modulator Parameter register High	CMPRH		R/W
00041C _H -00042B _H	Reserved			-
00042C _H	Voltage Regulator Control register	VRCR		R/W
00042D _H	Clock Input and LVD Control Register	CILCR		R/W
00042E _H -00042F _H	Reserved			-
000430 _H	I/O Port P00 - Data Direction Register	DDR00		R/W
000431 _H	I/O Port P01 - Data Direction Register	DDR01		R/W
000432 _H	I/O Port P02 - Data Direction Register	DDR02		R/W
000433 _H	I/O Port P03 - Data Direction Register	DDR03		R/W
000434 _H	I/O Port P04 - Data Direction Register	DDR04		R/W
000435 _H	I/O Port P05 - Data Direction Register	DDR05		R/W
000436 _H	I/O Port P06 - Data Direction Register	DDR06		R/W
000437 _H	I/O Port P07 - Data Direction Register	DDR07		R/W
000438 _H	I/O Port P08 - Data Direction Register	DDR08		R/W
000439 _H	I/O Port P09 - Data Direction Register	DDR09		R/W
00043A _H	I/O Port P10 - Data Direction Register	DDR10		R/W

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000801 _H	CAN1 - Control register High (reserved)	CTRLRH1		R
000802 _H	CAN1 - Status register Low	STATRL1	STATR1	R/W
000803 _H	CAN1 - Status register High (reserved)	STATRH1		R
000804 _H	CAN1 - Error Counter Low (Transmit)	ERRCNTL1	ERRCNT1	R
000805 _H	CAN1 - Error Counter High (Receive)	ERRCNTH1		R
000806 _H	CAN1 - Bit Timing Register Low	BTRL1	BTR1	R/W
000807 _H	CAN1 - Bit Timing Register High	BTRH1		R/W
000808 _H	CAN1 - Interrupt Register Low	INTRL1	INTR1	R
000809 _H	CAN1 - Interrupt Register High	INTRH1		R
00080A _H	CAN1 - Test Register Low	TESTRL1	TESTR1	R/W
00080B _H	CAN1 - Test Register High (reserved)	TESTRH1		R
00080C _H	CAN1 - BRP Extension register Low	BRPERL1	BRPER1	R/W
00080D _H	CAN1 - BRP Extension register High (reserved)	BRPERH1		R
00080E _H -00080F _H	Reserved			-
000810 _H	CAN1 - IF1 Command request register Low	IF1CREQL1	IF1CREQ1	R/W
000811 _H	CAN1 - IF1 Command request register High	IF1CREQH1		R/W
000812 _H	CAN1 - IF1 Command Mask register Low	IF1CMSKL1	IF1CMSK1	R/W
000813 _H	CAN1 - IF1 Command Mask register High (reserved)	IF1CMSKH1		R
000814 _H	CAN1 - IF1 Mask 1 Register Low	IF1MSK1L1	IF1MSK11	R/W
000815 _H	CAN1 - IF1 Mask 1 Register High	IF1MSK1H1		R/W
000816 _H	CAN1 - IF1 Mask 2 Register Low	IF1MSK2L1	IF1MSK21	R/W
000817 _H	CAN1 - IF1 Mask 2 Register High	IF1MSK2H1		R/W
000818 _H	CAN1 - IF1 Arbitration 1 Register Low	IF1ARB1L1	IF1ARB11	R/W
000819 _H	CAN1 - IF1 Arbitration 1 Register High	IF1ARB1H1		R/W
00081A _H	CAN1 - IF1 Arbitration 2 Register Low	IF1ARB2L1	IF1ARB21	R/W
00081B _H	CAN1 - IF1 Arbitration 2 Register High	IF1ARB2H1		R/W
00081C _H	CAN1 - IF1 Message Control Register Low	IF1MCTRL1	IF1MCTR1	R/W
00081D _H	CAN1 - IF1 Message Control Register High	IF1MCTRH1		R/W
00081E _H	CAN1 - IF1 Data A1 Low	IF1DTA1L1	IF1DTA11	R/W
00081F _H	CAN1 - IF1 Data A1 High	IF1DTA1H1		R/W
000820 _H	CAN1 - IF1 Data A2 Low	IF1DTA2L1	IF1DTA21	R/W
000821 _H	CAN1 - IF1 Data A2 High	IF1DTA2H1		R/W

($T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = 0\text{V}$)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Output L voltage	V_{OL2}	Normal outputs	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $I_{OL} = +2\text{mA}$	-	-	0.4	V	Driving strength set to 2mA
			$3.0\text{V} \leq V_{CC} < 4.5\text{V}$ $I_{OL} = +1.6\text{mA}$					
	V_{OL5}	Normal outputs	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $I_{OL} = +5\text{mA}$	-	-	0.4	V	Driving strength set to 5mA
			$3.0\text{V} \leq V_{CC} < 4.5\text{V}$ $I_{OL} = +3\text{mA}$					
	V_{OL3}	3mA outputs	$3.0\text{V} \leq V_{CC} \leq 5.5\text{V}$ $I_{OL} = +3\text{mA}$	-	-	0.4	V	
Input leak current	I_{IL}	Pnn_m	$V_{SS} < V_I < V_{CC}$ $AV_{SS}, AVR_L < V_I < AV_{CC}, AVR_H$	-1	-	+1	μA	Single port pin
Pull-up resistance	R_{UP}	Pnn_m, RSTX	$V_{CC} = 3.3\text{V} \pm 10\%$	40	100	160	k Ω	
			$V_{CC} = 5.0\text{V} \pm 10\%$	25	50	100	k Ω	

($T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = 0\text{V}$)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Run modes ^[1]	I_{CCRCH}	RC Run mode with $CLKS1/2 = CLKB = CLKP1/2 = 2\text{MHz}$ (CLKMC, CLKPLL and CLKSC stopped)	+25°C	2.9	4	mA	Flash devices at 1 Flash wait state
			+125°C	3.5	6.5		
			+25°C	1.7	2.7	mA	MB96345/346 at 1 ROM wait state
			+125°C	2.3	4.7		
	I_{CCRCL}	RC Run mode with $CLKS1/2 = CLKB = CLKP1/2 = 100\text{kHz}$, SMCR:LPMS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)	+25°C	0.4	0.6	mA	MB96F346/F347/F348 at 1 Flash wait state
			+125°C	0.9	3.5		
			+25°C	0.18	0.3	mA	MB96F345 at 1 Flash wait state
			+125°C	0.68	3.3		
			+25°C	0.4	0.6	mA	MB96345/346 at 1 ROM wait state
			+125°C	0.9	2.4		
		RC Run mode with $CLKS1/2 = CLKB = CLKP1/2 = 100\text{kHz}$, SMCR:LPMS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode, no Flash programming/erasing allowed)	+25°C	0.15	0.25	mA	Flash devices at 1 Flash wait state
			+125°C	0.65	3.2		
			+25°C	0.15	0.25	mA	MB96345/346 at 1 ROM wait state
			+125°C	0.65	2.1		
	I_{CCSUB}	Sub Run mode with $CLKS1/2 = CLKB = CLKP1/2 = 32\text{kHz}$ (CLKMC, CLKPLL and CLKRC stopped, no Flash programming/erasing allowed)	+25°C	0.1	0.2	mA	Flash devices at 1 Flash wait state
			+125°C	0.6	3		
			+25°C	0.1	0.2	mA	MB96345/346 at 1 ROM wait state
			+125°C	0.6	2		

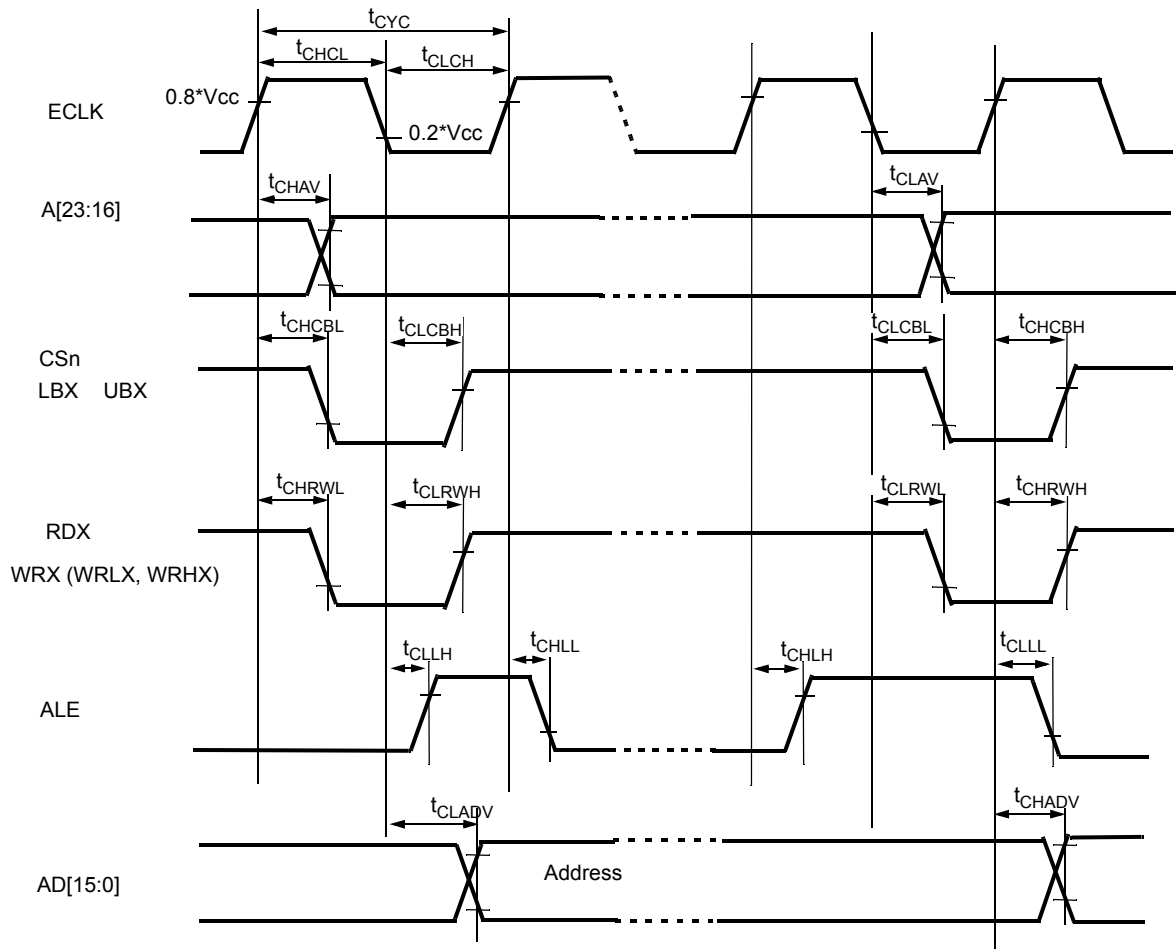
($T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = 0\text{V}$)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current for active Clock modulator	I_{CCLOMO}	Clock modulator enabled (CMCR:PDX = 1)	-	3	4.5	mA	Must be added to all current above
Flash Write/Erase current	$I_{CCFLASH}$	Current for one Flash module	-	15	40	mA	Must be added to all current above
	$I_{CCDFLASH}$	Current for one Data Flash module		10	20	mA	Must be added to all current above
Input capacitance	C_{IN}	-	-	5	15	pF	Other than C, AV_{CC} , AV_{SS} , AVRH, AVRL, V_{CC} , V_{SS}

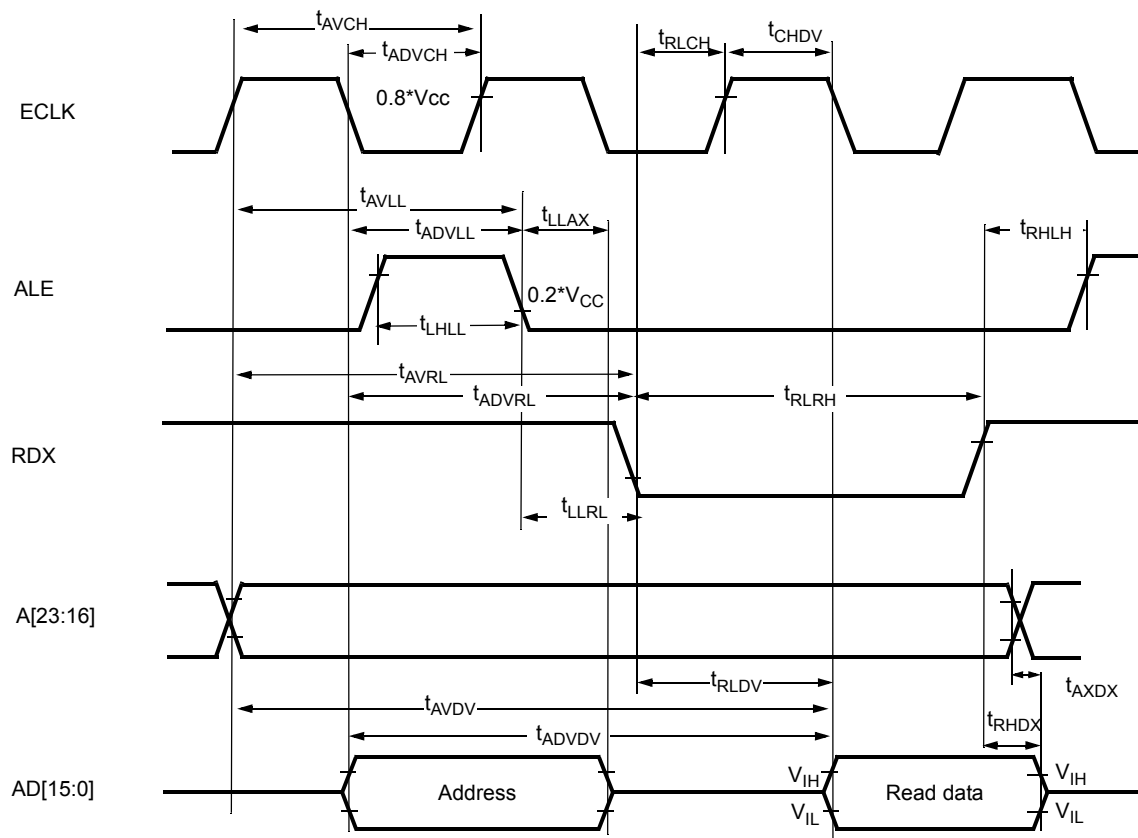
[1]: The power supply current is measured with a 4MHz external clock connected to the Main oscillator and a 32kHz external clock connected to the Sub oscillator. See chapter "Standby mode and voltage regulator control circuit" of the Hardware Manual for further details about voltage regulator control.

($T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 3.0$ to 4.5V , $V_{SS} = 0.0\text{V}$, $I_{Odrive} = 5\text{mA}$, $C_L = 50\text{pF}$)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
ECLK	t_{CYC}	ECLK	-	30	-	ns	
	t_{CHCL}			$t_{CYC}/2-8$	$t_{CYC}/2+8$		
	t_{CLCH}			$t_{CYC}/2-8$	$t_{CYC}/2+8$		
ECLK → UBX/ LBX / CSn time	t_{CHCBH}	CSn, UBX, LBX, ECLK	-	-25	25	ns	
	t_{CHCBL}			-25	25		
	t_{CLCBH}			-25	25		
	t_{CLCBL}			-25	25		
ECLK → ALE time	t_{CHLH}	ALE, ECLK	-	-15	15	ns	
	t_{CHLL}			-15	15		
	t_{CLLH}			-15	15		
	t_{CLLL}			-15	15		
ECLK → address valid time	t_{CHAV}	A[23:16], ECLK	-	-20	20	ns	
	t_{CLAV}			-20	20		
	t_{CLADV}	AD[15:0], ECLK	-	-20	20	ns	
	t_{CHADV}			-20	20		
ECLK → RDX /WRX time	t_{CHRWL}	RDX, WRX, WRLX, WRHX, ECLK	-	-15	15	ns	
	t_{CHRWL}			-15	15		
	t_{CLRWH}			-15	15		
	t_{CLRWL}			-15	15		



Refer to the Hardware Manual for detailed Timing Charts



Refer to the Hardware Manual for detailed Timing Charts

($T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 3.0$ to 4.5V , $V_{SS} = 0.0\text{V}$, $I_{Odrive} = 5\text{mA}$, $C_L = 50\text{pF}$)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
WRX pulse width	t_{WLWH}	WRX, WRXL, WRHX	-	$t_{CYC} - 8$	-	ns	w/o cycle extension
Valid data output $\Rightarrow$ WRX $\uparrow$ time	t_{DVWH}	WRX, WRLX, WRHX, AD[15:0]	-	$t_{CYC} - 25$	-	ns	w/o cycle extension
WRX $\uparrow \Rightarrow$ Data hold time	t_{WHDX}	WRX, WRLX, WRHX, AD[15:0]	-	$t_{CYC}/2 - 20$	-	ns	
WRX $\uparrow \Rightarrow$ Address valid time	t_{WHAX}	WRX, WRLX, WRHX, A[23:16]	-	$t_{CYC}/2 - 20$	-	ns	
WRX $\uparrow \Rightarrow$ ALE $\uparrow$ time	t_{WHLH}	WRX, WRLX, WRHX, ALE	EBM:ACE=1 and EACL:STS=1	$2t_{CYC} - 15$	-	ns	
			other EBM:ACE and EACL:STS setting	$t_{CYC} - 15$	-		
WRX $\downarrow \Rightarrow$ ECLK $\uparrow$ time	t_{WLCH}	WRX, WRLX, WRHX, ECLK	-	$t_{CYC}/2 - 15$	-	ns	
CSn $\Rightarrow$ WRX time	t_{CSLWL}	WRX, WRLX, WRHX, CSn	EACL:ACE=0	-	$3t_{CYC}/2 - 20$	ns	
			EACL:ACE=1	-	$5t_{CYC}/2 - 20$		
WRX $\Rightarrow$ CSn time	t_{WHCSH}	WRX, WRLX, WRHX, CSn	-	$t_{CYC}/2 - 20$	-	ns	

14.7 Low Voltage Detector Characteristics

($T_A = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$, $V_{CC} = AV_{CC} = 3.0\text{V} - 5.5\text{V}$, $V_{SS} = AV_{SS} = 0\text{V}$)

Parameter	Symbol	Value [1]		Value [2]		Unit	Remarks
		Min	Max	Min	Max		
Stabilization time	$T_{LVDSTAB}$	-	75	-	110	μs	After power-up or change of detection level
Level 0	V_{DL0}	2.7	2.9	2.65	2.95	V	CILCR:LVL[3:0]="0000"
Level 1	V_{DL1}	2.9	3.1	2.85	3.2	V	CILCR:LVL[3:0]="0001"
Level 2	V_{DL2}	3.1	3.3	3.05	3.4	V	CILCR:LVL[3:0]="0010"
Level 3	V_{DL3}	3.5	3.75	3.45	3.85	V	CILCR:LVL[3:0]="0011"
Level 4	V_{DL4}	3.6	3.85	3.55	3.95	V	CILCR:LVL[3:0]="0100"
Level 5	V_{DL5}	3.7	3.95	3.65	4.1	V	CILCR:LVL[3:0]="0101"
Level 6	V_{DL6}	3.8	4.05	3.75	4.2	V	CILCR:LVL[3:0]="0110"
Level 7	V_{DL7}	3.9	4.15	3.85	4.3	V	CILCR:LVL[3:0]="0111"
Level 8	V_{DL8}	4.0	4.25	3.95	4.4	V	CILCR:LVL[3:0]="1000"
Level 9	V_{DL9}	4.1	4.35	4.05	4.5	V	CILCR:LVL[3:0]="1001"
Level 10	V_{DL10}	not used		not used			
Level 11	V_{DL11}	not used		not used			
Level 12	V_{DL12}	not used		not used			
Level 13	V_{DL13}	not used		not used			
Level 14	V_{DL14}	not used		not used			
Level 15	V_{DL15}	not used		not used			

[1]: valid for all devices except devices listed under "[2]"

[2]: valid for: MB96F345

CILCR:LVL[3:0] are the low voltage detector level select bits of the CILCR register.

Levels 10 to 15 are not used in this device.

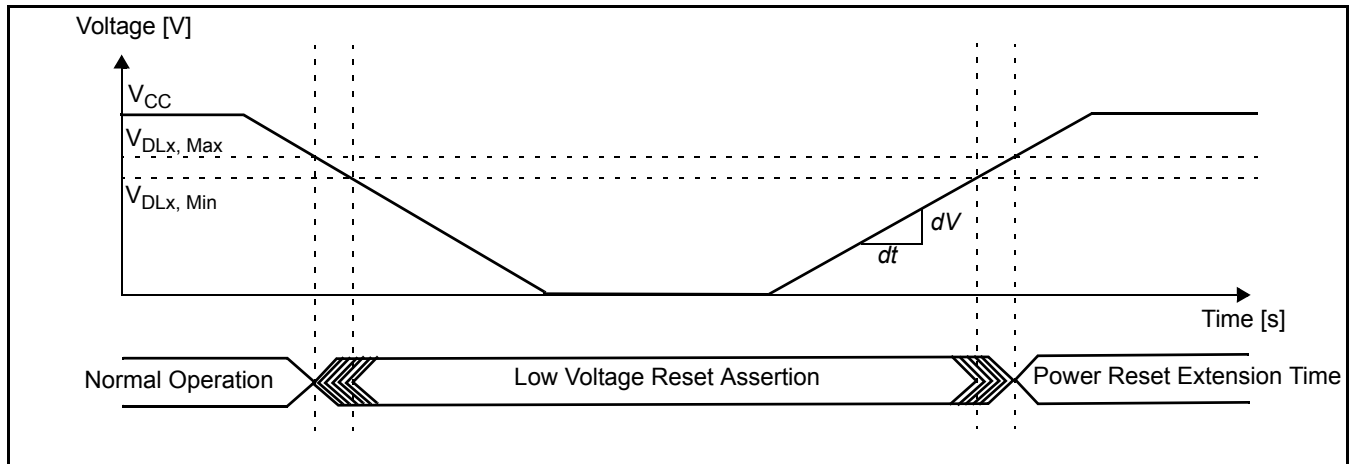
For correct detection, the slope of the voltage level must satisfy $\left| \frac{dV}{dt} \right| \leq 0.004 \frac{V}{\mu\text{s}}$.

Faster variations are regarded as noise and may not be detected.

The functional operation of the MCU is guaranteed down to the minimum low voltage detection level of $V_{CC} = 2.7\text{V}$. The electrical characteristics however are only valid in the specified range (usually down to 3.0V).

14.7.1 Low Voltage Detector Operation

In the following figure, the occurrence of a low voltage condition is illustrated. For a detailed description of the reset and startup behavior, please refer to the corresponding hardware manual chapter.



14.8 Flash Memory Program/erase Characteristics

($T_A = -40^{\circ}\text{C}$ to 105°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = 0\text{V}$)

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time Program/Data Flash (Main Flash)	-	0.9	3.6	s	Without erasure pre-programming time
Sector erase time Data Flash	-	0.5	2	s	Without erasure pre-programming time
	-	0.8	3.6	s	Including erasure pre-programming time
Chip erase time Program/Data Flash (Main Flash)	-	n*0.9	n*3.6	s	Without erasure pre-programming time (n is the number of Flash sector of the device)
Chip erase time Data Flash	-	2.5	10	s	Without erasure pre-programming time
	-	3.7	16.4	s	Including erasure pre-programming time
Word (16-bit width) programming time Program/Data Flash (Main Flash)	-	23	370	us	Without overhead time for submitting write command
Byte (8-bit width) programming time Data Flash	-	15	100	us	Without overhead time for submitting write command
Program/Erase cycle	10000	-	-	cycle	100 000 Program/Erase cycles are under evaluation by Cypress
Flash data retention time	20	-	-	year	[1]

[1]: This value was converted from the results of evaluating the reliability of the technology (using Arrhenius equation to convert high temperature measurements into normalized value at 85°C)