Infineon Technologies - MB96F348RSAPMCR-GSE2 Datasheet

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What is "Embedded - Microcontrollers"?

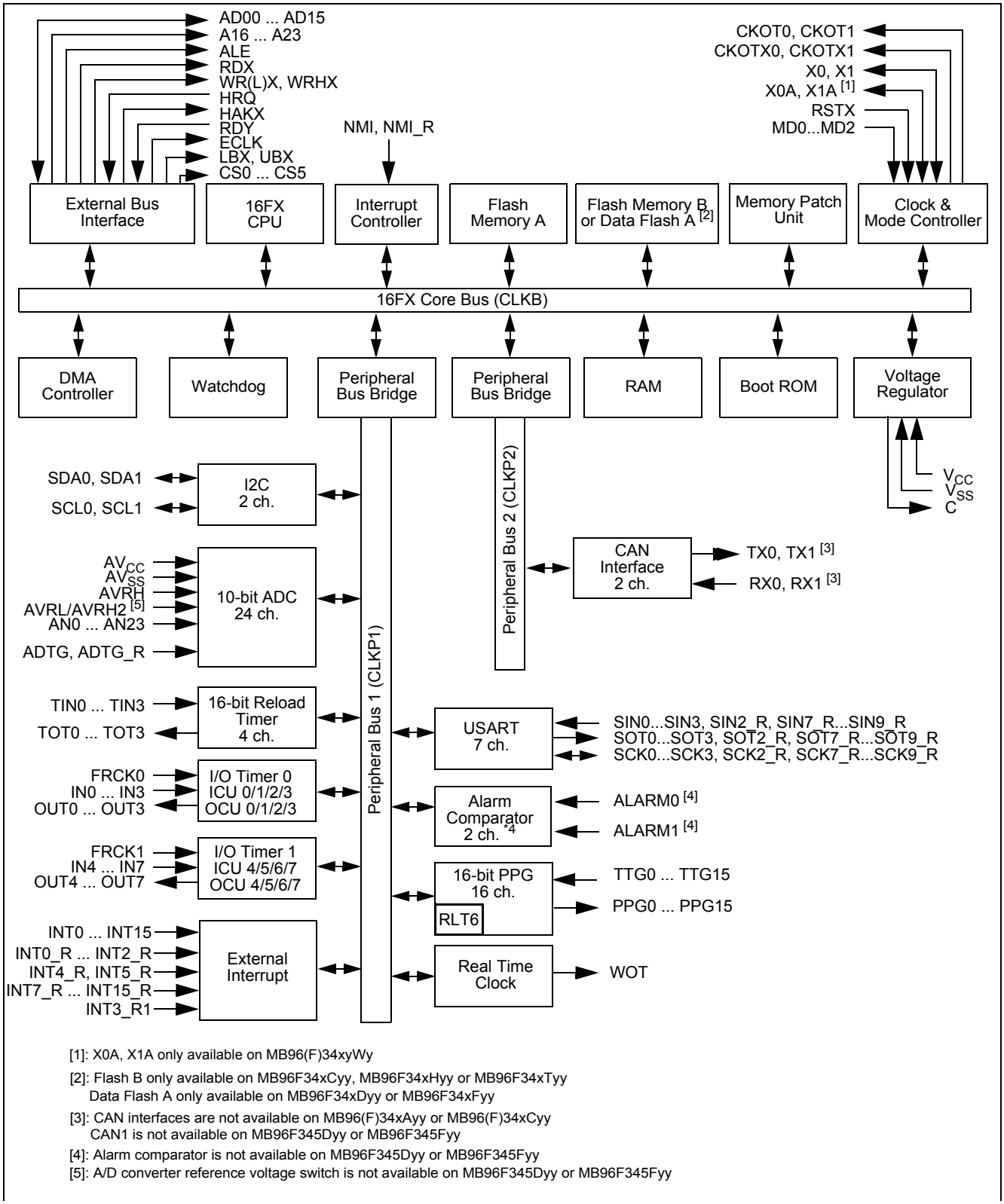
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	56MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, LVR, POR, PWM, WDT
Number of I/O	82
Program Memory Size	544KB (544K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f348rsapmcr-gse2

2. Block Diagram

Figure 1. Block diagram of MB96(F)34x



[1]: X0A, X1A only available on MB96(F)34xyWy

[2]: Flash B only available on MB96F34xCyy, MB96F34xHyy or MB96F34xTyy
Data Flash A only available on MB96F34xDyy or MB96F34xFyy

[3]: CAN interfaces are not available on MB96(F)34xAyy or MB96(F)34xCyy
CAN1 is not available on MB96F345Dyy or MB96F345Fyy

[4]: Alarm comparator is not available on MB96F345Dyy or MB96F345Fyy

[5]: A/D converter reference voltage switch is not available on MB96F345Dyy or MB96F345Fyy

Table 1: Pin Function description

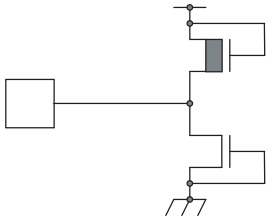
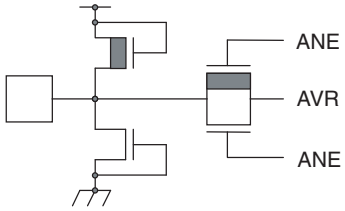
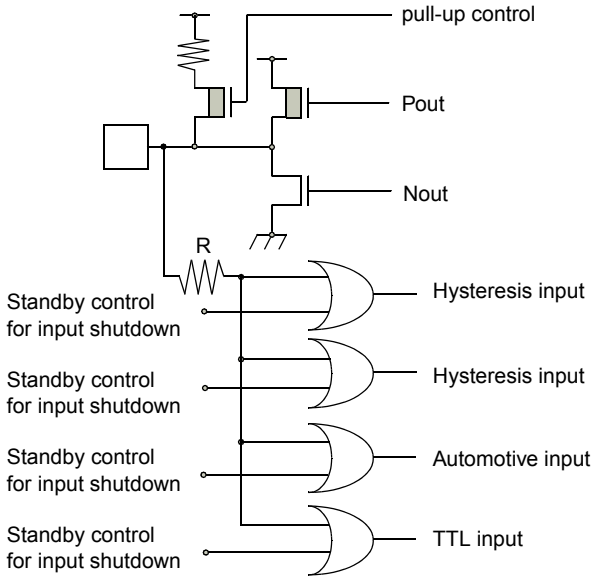
Pin name	Feature	Description
RDY	External bus	External bus interface external wait state request input
RSTX	Core	Reset input
RXn	CAN	CAN interface n RX input
SCKn	USART	USART n serial clock input/output
SCKn_R	USART	Relocated USART n serial clock input/output
SCLn	I2C	I^2C interface n clock I/O input/output
SDAn	I2C	I^2C interface n serial data I/O input/output
SINn	USART	USART n serial data input
SINn_R	USART	Relocated USART n serial data input
SOTn	USART	USART n serial data output
SOTn_R	USART	Relocated USART n serial data output
TINn	Reload Timer	Reload Timer n event input
TOTn	Reload Timer	Reload Timer n output
TTGn	PPG	Programmable Pulse Generator n trigger input
TXn	CAN	CAN interface n TX output
UBX	External bus	External Bus Interface Upper Byte select strobe output
V_{CC}	Supply	Power supply
V_{SS}	Supply	Power supply
WOT	RTC	Real Timer clock output
WRHX	External bus	External bus High byte write strobe output
WRLX/WRX	External bus	External bus Low byte / Word write strobe output
X0	Clock	Oscillator input
X0A	Clock	Subclock Oscillator input (only for devices with suffix "W")
X1	Clock	Oscillator output
X1A	Clock	Subclock Oscillator output (only for devices with suffix "W")

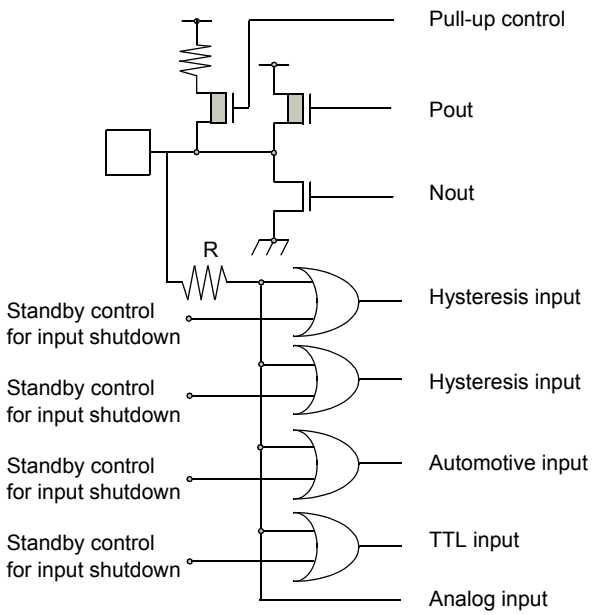
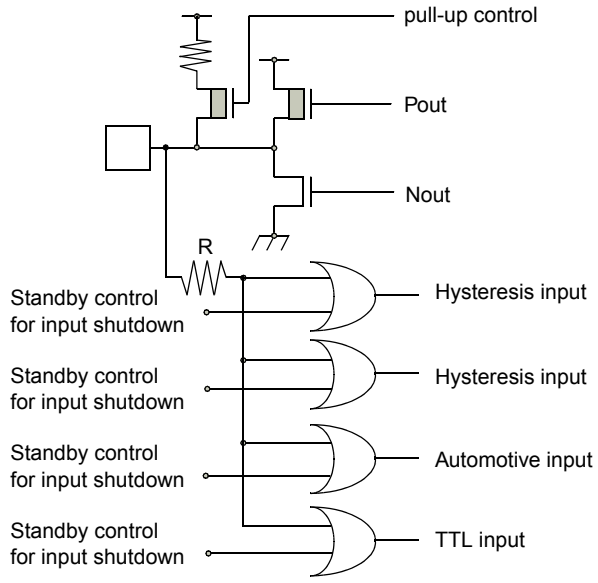
5. Pin Circuit Type

Table 2: Pin circuit types

FPT-100P-M20		FPT-100P-M22	
Pin no.	Circuit type [1]	Pin no.	Circuit type [1]
1-10	H	1-12	H
11,12	B [2]	13, 14	B [2]
11,12	H [3]	13, 14	H [3]
13,14	Supply	15,16	Supply
15	F	17	F
16,17	H	18,19	H
18-21	N	20-23	N
22-29	I	24-31	I
30	Supply	32	Supply
31-32	G	33-34	G
33	Supply	35	Supply
34 to 41	I	36 to 43	I
42	Supply	44	Supply
43 to 48	I	45 to 50	I
49 to 51	C	51 to 53	C
52	E	54	E
53 to 54	I	55 to 56	I
55 to 62	H	57 to 64	H
63, 64	Supply	65, 66	Supply
65 to 87	H	67 to 89	H
88,89	Supply	90, 91	Supply
90, 91	A	92, 93	A
92-100	H	94 to 100	H

[1]: Please refer to “ I/O Circuit Type” for details on the I/O circuit types
[2]: Devices with suffix ”W”
[3]: Devices without suffix ”W”

Type	Circuit	Remarks
F		■ Power supply input protection circuit
G		■ A/D converter ref+ (AVRH/AVRH2) power supply input pin with protection circuit ■ Flash devices do not have a protection circuit against VCC for pins AVRH/AVRH2 ■ Devices without AVRH reference switch do not have an analog switch for the AVRL pin
H		■ CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) ■ 2 different CMOS hysteresis inputs with input shutdown function * ■ Automotive input with input shutdown function ■ TTL input with input shutdown function * ■ Programmable pull-up resistor: 50kΩ approx. *MB96F345Dyy or MB96F345Fyy: Only Automotive input and CMOS hysteresis input (0.7/0.3) are supported

Type	Circuit	Remarks
I		■ CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) ■ 2 different CMOS hysteresis inputs with input shutdown function * ■ Automotive input with input shutdown function ■ TTL input with input shutdown function * ■ Programmable pull-up resistor: 50kΩ approx. ■ Analog input *MB96F345Dyy or MB96F345Fyy: Only Automotive input and CMOS hysteresis input (0.7/0.3) are supported
N		■ CMOS level output (I_{OL} = 3mA, I_{OH} = -3mA) ■ 2 different CMOS hysteresis inputs with input shutdown function * ■ Automotive input with input shutdown function ■ TTL input with input shutdown function * ■ Programmable pull-up resistor: 50kΩ approx. *MB96F345Dyy or MB96F345Fyy: Only Automotive input and CMOS hysteresis input (0.7/0.3) are supported

8. User ROM Memory Map For Flash Devices

MB96F345D
MB96F345F

Alternative mode CPU address	Flash memory mode address	Flash size 160kByte +64KByte Data Flash	
$FF:FFFF_H$ $FF:0000_H$	$3F:FFFF_H$ $3F:0000_H$	S39 - 64K	Flash A
$FE:FFFF_H$ $FE:0000_H$	$3E:FFFF_H$ $3E:0000_H$	S38 - 64K	
$FD:FFFF_H$ $FD:0000_H$	$3D:FFFF_H$ $3D:0000_H$	External bus	
$FC:FFFF_H$ $FC:0000_H$	$3C:FFFF_H$ $3C:0000_H$		
$FB:FFFF_H$ $FB:0000_H$	$3B:FFFF_H$ $3B:0000_H$		
$FA:FFFF_H$ $FA:0000_H$	$3A:FFFF_H$ $3A:0000_H$		
$F9:FFFF_H$ $F9:0000_H$	$39:FFFF_H$ $39:0000_H$		
$F8:FFFF_H$ $F8:0000_H$	$38:FFFF_H$ $38:0000_H$		
$F7:FFFF_H$ $F7:0000_H$	$37:FFFF_H$ $37:0000_H$		
$F6:FFFF_H$ $F6:0000_H$	$36:FFFF_H$ $36:0000_H$		
$F5:FFFF_H$ $F5:0000_H$	$35:FFFF_H$ $35:0000_H$		
$F4:FFFF_H$ $F4:0000_H$	$34:FFFF_H$ $34:0000_H$		
$F3:FFFF_H$ $F3:0000_H$	$33:FFFF_H$ $33:0000_H$		
$F2:FFFF_H$ $F2:0000_H$	$32:FFFF_H$ $32:0000_H$		
$F1:FFFF_H$ $F1:0000_H$	$31:FFFF_H$ $31:0000_H$		
$F0:FFFF_H$ $F0:0000_H$	$30:FFFF_H$ $30:0000_H$		
$E0:FFFF_H$ $E0:0000_H$			
$DF:FFFF_H$ $DF:8000_H$		Reserved	
$DF:7FFF_H$ $DF:6000_H$	$1F:7FFF_H$ $1F:6000_H$	SA3 - 8K	Flash A
$DF:5FFF_H$ $DF:4000_H$	$1F:5FFF_H$ $1F:4000_H$	SA2 - 8K	
$DF:3FFF_H$ $DF:2000_H$	$1F:3FFF_H$ $1F:2000_H$	SA1 - 8K	
$DF:1FFF_H$ $DF:0000_H$	$1F:1FFF_H$ $1F:0000_H$	SA0 - 8K [1]	
$DE:FFFF_H$ $DE:0000_H$		Reserved	
$0E:FFFF_H$ $0E:FF00_H$	$(0E:FFFF_H)$ $(0E:FF00_H)$	SDA0-256 [2]	Data Flash A
$0E:FEFF_H$ $0E:0000_H$		Reserved	
$0D:FFFF_H$ $0D:C000_H$	$(0F:FFFF_H)$ $(0F:C000_H)$	SDA4-16K	Data Flash A
$0D:BFFF_H$ $0D:8000_H$	$(0F:BFFF_H)$ $(0F:8000_H)$	SDA3-16K	
$0D:7FFF_H$ $0D:4000_H$	$(0F:7FFF_H)$ $(0F:4000_H)$	SDA2-16K	
$0D:3FFF_H$ $0D:0000_H$	$(0F:3FFF_H)$ $(0F:0000_H)$	SDA1-16K	
$0C:FFFF_H$ $0C:0000_H$		Reserved	

[1]: Sector SA0 contains the ROM Configuration Block RCBA at CPU address $DF:0000_H$ - $DF:007F_H$

[2]: Sector SDA0 contains the ROM Configuration Block RCBDA at CPU address $DE:FF00_H$ - $DE:FF2F_H$

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000081_H	PPG1 - Timer register			R
000082_H	PPG1 - Period setting register		PCSR1	W
000083_H	PPG1 - Period setting register			W
000084_H	PPG1 - Duty cycle register		PDUT1	W
000085_H	PPG1 - Duty cycle register			W
000086_H	PPG1 - Control status register Low	PCNL1	PCN1	R/W
000087_H	PPG1 - Control status register High	PCNH1		R/W
000088_H	PPG2 - Timer register		PTMR2	R
000089_H	PPG2 - Timer register			R
$00008A_H$	PPG2 - Period setting register		PCSR2	W
$00008B_H$	PPG2 - Period setting register			W
$00008C_H$	PPG2 - Duty cycle register		PDUT2	W
$00008D_H$	PPG2 - Duty cycle register			W
$00008E_H$	PPG2 - Control status register Low	PCNL2	PCN2	R/W
$00008F_H$	PPG2 - Control status register High	PCNH2		R/W
000090_H	PPG3 - Timer register		PTMR3	R
000091_H	PPG3 - Timer register			R
000092_H	PPG3 - Period setting register		PCSR3	W
000093_H	PPG3 - Period setting register			W
000094_H	PPG3 - Duty cycle register		PDUT3	W
000095_H	PPG3 - Duty cycle register			W
000096_H	PPG3 - Control status register Low	PCNL3	PCN3	R/W
000097_H	PPG3 - Control status register High	PCNH3		R/W
000098_H	PPG7-PPG4 - General Control register 1 Low	GCN1L1	GCN11	R/W
000099_H	PPG7-PPG4 - General Control register 1 High	GCN1H1		R/W
$00009A_H$	PPG7-PPG4 - General Control register 2 Low	GCN2L1	GCN21	R/W
$00009B_H$	PPG7-PPG4 - General Control register 2 High	GCN2H1		R/W
$00009C_H$	PPG4 - Timer register		PTMR4	R
$00009D_H$	PPG4 - Timer register			R
$00009E_H$	PPG4 - Period setting register		PCSR4	W
$00009F_H$	PPG4 - Period setting register			W
$0000A0_H$	PPG4 - Duty cycle register		PDUT4	W

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$0000A1_H$	PPG4 - Duty cycle register			W
$0000A2_H$	PPG4 - Control status register Low	PCNL4	PCN4	R/W
$0000A3_H$	PPG4 - Control status register High	PCNH4		R/W
$0000A4_H$	PPG5 - Timer register		PTMR5	R
$0000A5_H$	PPG5 - Timer register			R
$0000A6_H$	PPG5 - Period setting register		PCSR5	W
$0000A7_H$	PPG5 - Period setting register			W
$0000A8_H$	PPG5 - Duty cycle register		PDUT5	W
$0000A9_H$	PPG5 - Duty cycle register			W
$0000AA_H$	PPG5 - Control status register Low	PCNL5	PCN5	R/W
$0000AB_H$	PPG5 - Control status register High	PCNH5		R/W
$0000AC_H$	I2C0 - Bus Status Register	IBSR0		R
$0000AD_H$	I2C0 - Bus Control Register	IBCR0		R/W
$0000AE_H$	I2C0 - Ten bit Slave address Register Low	ITBAL0	ITBA0	R/W
$0000AF_H$	I2C0 - Ten bit Slave address Register High	ITBAH0		R/W
$0000B0_H$	I2C0 - Ten bit Address mask Register Low	ITMKL0	ITMK0	R/W
$0000B1_H$	I2C0 - Ten bit Address mask Register High	ITMKH0		R/W
$0000B2_H$	I2C0 - Seven bit Slave address Register	ISBA0		R/W
$0000B3_H$	I2C0 - Seven bit Address mask Register	ISMK0		R/W
$0000B4_H$	I2C0 - Data Register	IDAR0		R/W
$0000B5_H$	I2C0 - Clock Control Register	ICCR0		R/W
$0000B6_H$	I2C1 - Bus Status Register	IBSR1		R
$0000B7_H$	I2C1 - Bus Control Register	IBCR1		R/W
$0000B8_H$	I2C1 - Ten bit Slave address Register Low	ITBAL1	ITBA1	R/W
$0000B9_H$	I2C1 - Ten bit Slave address Register High	ITBAH1		R/W
$0000BA_H$	I2C1 - Ten bit Address mask Register Low	ITMKL1	ITMK1	R/W
$0000BB_H$	I2C1 - Ten bit Address mask Register High	ITMKH1		R/W
$0000BC_H$	I2C1 - Seven bit Slave address Register	ISBA1		R/W
$0000BD_H$	I2C1 - Seven bit Address mask Register	ISMK1		R/W
$0000BE_H$	I2C1 - Data Register	IDAR1		R/W
$0000BF_H$	I2C1 - Clock Control Register	ICCR1		R/W
$0000C0_H$	USART0 - Serial Mode Register	SMR0		R/W

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000715_H	CAN0 - IF1 Mask 1 Register High	IF1MSK1H0		R/W
000716_H	CAN0 - IF1 Mask 2 Register Low	IF1MSK2L0	IF1MSK20	R/W
000717_H	CAN0 - IF1 Mask 2 Register High	IF1MSK2H0		R/W
000718_H	CAN0 - IF1 Arbitration 1 Register Low	IF1ARB1L0	IF1ARB10	R/W
000719_H	CAN0 - IF1 Arbitration 1 Register High	IF1ARB1H0		R/W
$00071A_H$	CAN0 - IF1 Arbitration 2 Register Low	IF1ARB2L0	IF1ARB20	R/W
$00071B_H$	CAN0 - IF1 Arbitration 2 Register High	IF1ARB2H0		R/W
$00071C_H$	CAN0 - IF1 Message Control Register Low	IF1MCTRL0	IF1MCTR0	R/W
$00071D_H$	CAN0 - IF1 Message Control Register High	IF1MCTRH0		R/W
$00071E_H$	CAN0 - IF1 Data A1 Low	IF1DTA1L0	IF1DTA10	R/W
$00071F_H$	CAN0 - IF1 Data A1 High	IF1DTA1H0		R/W
000720_H	CAN0 - IF1 Data A2 Low	IF1DTA2L0	IF1DTA20	R/W
000721_H	CAN0 - IF1 Data A2 High	IF1DTA2H0		R/W
000722_H	CAN0 - IF1 Data B1 Low	IF1DTB1L0	IF1DTB10	R/W
000723_H	CAN0 - IF1 Data B1 High	IF1DTB1H0		R/W
000724_H	CAN0 - IF1 Data B2 Low	IF1DTB2L0	IF1DTB20	R/W
000725_H	CAN0 - IF1 Data B2 High	IF1DTB2H0		R/W
000726_H-$00073F_H$	Reserved			-
000740_H	CAN0 - IF2 Command request register Low	IF2CREQL0	IF2CREQ0	R/W
000741_H	CAN0 - IF2 Command request register High	IF2CREQH0		R/W
000742_H	CAN0 - IF2 Command Mask register Low	IF2CMSKL0	IF2CMSK0	R/W
000743_H	CAN0 - IF2 Command Mask register High (reserved)	IF2CMSKH0		R
000744_H	CAN0 - IF2 Mask 1 Register Low	IF2MSK1L0	IF2MSK10	R/W
000745_H	CAN0 - IF2 Mask 1 Register High	IF2MSK1H0		R/W
000746_H	CAN0 - IF2 Mask 2 Register Low	IF2MSK2L0	IF2MSK20	R/W
000747_H	CAN0 - IF2 Mask 2 Register High	IF2MSK2H0		R/W
000748_H	CAN0 - IF2 Arbitration 1 Register Low	IF2ARB1L0	IF2ARB10	R/W
000749_H	CAN0 - IF2 Arbitration 1 Register High	IF2ARB1H0		R/W
$00074A_H$	CAN0 - IF2 Arbitration 2 Register Low	IF2ARB2L0	IF2ARB20	R/W
$00074B_H$	CAN0 - IF2 Arbitration 2 Register High	IF2ARB2H0		R/W
$00074C_H$	CAN0 - IF2 Message Control Register Low	IF2MCTRL0	IF2MCTR0	R/W
$00074D_H$	CAN0 - IF2 Message Control Register High	IF2MCTRH0		R/W

13. Handling Devices

Special care is required for the following when handling the device:

- Latch-up prevention
- Unused pins handling
- External clock usage
- Unused sub clock signal
- Notes on PLL clock mode operation
- Power supply pins (V_{CC}/V_{SS})
- Crystal oscillator circuit
- Turn on sequence of power supply to A/D converter and analog inputs
- Pin handling when not using the A/D converter
- Notes on energization
- Stabilization of power supply voltage
- Serial communication
- Handling of Data Flash

13.1 Latch-up prevention

CMOS IC chips may suffer latch-up under the following conditions:

- A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V_{CC} pins and V_{SS} pins.
- The AV_{CC} power supply is applied before the V_{CC} voltage.

Latch-up may increase the power supply current dramatically, causing thermal damages to the device.

For the same reason, extra care is required to not let the analog power-supply voltage (AV_{CC}, AVRH) exceed the digital power-supply voltage.

13.2 Unused pins handling

Unused input pins can be left open when the input is disabled (corresponding bit of Port Input Enable register PIER = 0).

Leaving unused input pins open when the input is enabled may result in misbehavior and possible permanent damage of the device. They must therefore be pulled up or pulled down through resistors. To prevent latch-up, those resistors should be more than 2 kΩ.

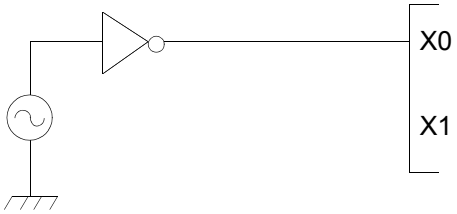
Unused bidirectional pins can be set either to the output state and be then left open, or to the input state with either input disabled or external pull-up/pull-down resistor as described above.

13.3 External clock usage

The permitted frequency range of an external clock depends on the oscillator type and configuration. See AC Characteristics for detailed modes and frequency limits. Single and opposite phase external clocks must be connected as follows:

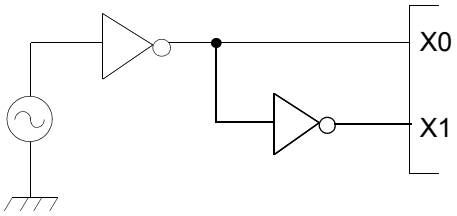
13.3.1 Single phase external clock

■ When using a single phase external clock, X0 pin must be driven and X1 pin left open.



13.3.2 Opposite phase external clock

■ When using an opposite phase external clock, X1 (X1A) must be supplied with a clock signal which has the opposite phase to the X0 (X0A) pins.



13.4 Unused sub clock signal

If the pins X0A and X1A are not connected to an oscillator, a pull-down resistor must be connected on the X0A pin and the X1A pin must be left open.

13.5 Notes on PLL clock mode operation

If the PLL clock mode is selected and no external oscillator is operating or no external clock is supplied, the microcontroller attempts to work with the free oscillating PLL. Performance of this operation, however, cannot be guaranteed.

13.6 Power supply pins (V_{CC}/v_{SS})

It is required that all V_{CC}-level as well as all V_{SS}-level power supply pins are at the same potential. If there is more than one V_{CC} or V_{SS} level, the device may operate incorrectly or be damaged even within the guaranteed operating range.

V_{CC} and V_{SS} must be connected to the device from the power supply with lowest possible impedance.

As a measure against power supply noise, it is required to connect a bypass capacitor of about 0.1 μF between V_{CC} and V_{SS} as close as possible to V_{CC} and V_{SS} pins.

13.7 Crystal oscillator and ceramic resonator circuit

Noise at X0, X1 pins or X0A, X1A pins might cause abnormal operation. It is required to provide bypass capacitors with shortest possible distance to X0, X1 pins and X0A, X1A pins, crystal oscillator (or ceramic resonator) and ground lines, and, to the utmost effort, that the lines of oscillation circuit do not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board art work surrounding X0, X1 pins and X0A, X1A pins with a ground area for stabilizing the operation.

It is highly recommended to evaluate the quartz/MCU or resonator/MCU system at the quartz or resonator manufacturer, especially when using low-Q resonators at higher frequencies.

13.8 Turn on sequence of power supply to A/D converter and analog inputs

It is required to turn the A/D converter power supply (AV_{CC}, AVRH, AVRL) and analog inputs (ANn) on after turning the digital power supply (V_{CC}) on.

It is also required to turn the digital power off after turning the A/D converter supply and analog inputs off. In this case, the voltage must not exceed AVRH or AV_{CC} (turning the analog and digital power supplies simultaneously on or off is acceptable).

13.9 Pin handling when not using the A/D converter

It is required to connect the unused pins of the A/D converter as $AV_{CC} = V_{CC}$, AV_{SS} = AVRH = AVRL = V_{SS}.

13.10 Notes on Power-on

To prevent malfunction of the internal voltage regulator, supply voltage profile while turning the power supply on should be slower than 50µs from 0.2 V to 2.7 V.

13.11 Stabilization of power supply voltage

If the power supply voltage varies acutely even within the operation safety range of the Vcc power supply voltage, a malfunction may occur. The Vcc power supply voltage must therefore be stabilized. As stabilization guidelines, the power supply voltage must be stabilized in such a way that Vcc ripple fluctuations (peak to peak value) in the commercial frequencies (50 to 60 Hz) fall within 10% of the standard Vcc power supply voltage and the transient fluctuation rate becomes 0.1V/µs or less in instantaneous fluctuation for power supply switching.

13.12 Serial communication

There is a possibility to receive wrong data due to noise or other causes on the serial communication.Therefore, design a printed circuit board so as to avoid noise.Consider receiving of wrong data when designing the system. For example apply a checksum and retransmit the data if an error occurs.

13.13 Handling of Data Flash

The Data Flash requires different and additional control signals for parallel programming. Please check with your programming equipment maker for support of this interface.

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Permitted Power dissipation (Mask ROM devices) [4]	P_D	-	350	mW	T_A=105°C
		-	360	mW	T_A=125°C [6]
Operating ambient temperature	T_A	0	+70	°C	MB96V300B
		-40	+105		
		-40	+125		[6]
Storage temperature	T_{STG}	-55	+150	°C	

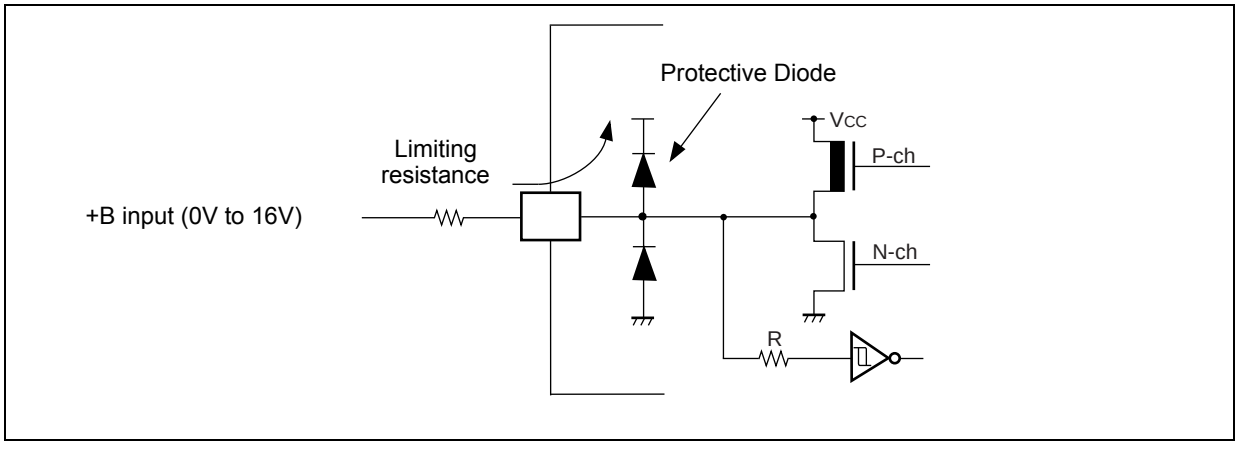
[1]: AV_{CC} and V_{CC} must be set to the same voltage. It is required that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} neither when the power is switched on.

[2]: V_I and V_O should not exceed V_{CC} + 0.3 V. V_I should also not exceed the specified ratings. However if the maximum current to/from a input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating. Input/output voltages of standard ports depend on V_{CC}.

[3]:

- Applicable to all general purpose I/O pins (Pnn_m)
- Use within recommended operating conditions.
- Use at DC voltage (current)
- The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the Power reset (except devices with persistent low voltage reset in internal vector mode).

Sample recommended circuits:



(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Timer modes[1]	I_{CCTPLL}	PLL Timer mode with CLKMC = 4MHz, CLKPLL = 48MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	1.6	2	mA	Flash devices
			+125°C	2.1	5		
			+25°C	1.6	2	mA	MB96345/346
			+125°C	2.1	4		
	$I_{CCTMAIN}$	Main Timer mode with CLKMC = 4MHz, SMCR:LPMSS = 0 (CLKPLL, CLKRC and CLKSC stopped. Voltage regulator in high power mode)	+25°C	0.35	0.5	mA	MB96F346/F347/F348
			+125°C	0.85	3.3		
			+25°C	0.13	0.2	mA	MB96F345
			+125°C	0.63	3		
			+25°C	0.35	0.5	mA	MB96345/346
			+125°C	0.85	2.3		
		Main Timer mode with CLKMC = 4MHz, SMCR:LPMSS = 1 (CLKPLL, CLKRC and CLKSC stopped. Voltage regulator in low power mode)	+25°C	0.1	0.15	mA	Flash devices
			+125°C	0.6	2.9		
			+25°C	0.1	0.15		MB96345/346
			+125°C	0.6	1.9		
	I_{CCTRCH}	RC Timer mode with CLKRC = 2MHz, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)	+25°C	0.35	0.5	mA	MB96F346/F347/F348
			+125°C	0.85	3.3		
			+25°C	0.13	0.2	mA	MB96F345
			+125°C	0.63	3		
			+25°C	0.35	0.5	mA	MB96345/346
			+125°C	0.85	2.3		
		RC Timer mode with CLKRC = 2MHz, SMCR:LPMSS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode)	+25°C	0.1	0.15	mA	Flash devices
			+125°C	0.6	2.9		
			+25°C	0.1	0.15	mA	MB96345/346
			+125°C	0.6	1.9		

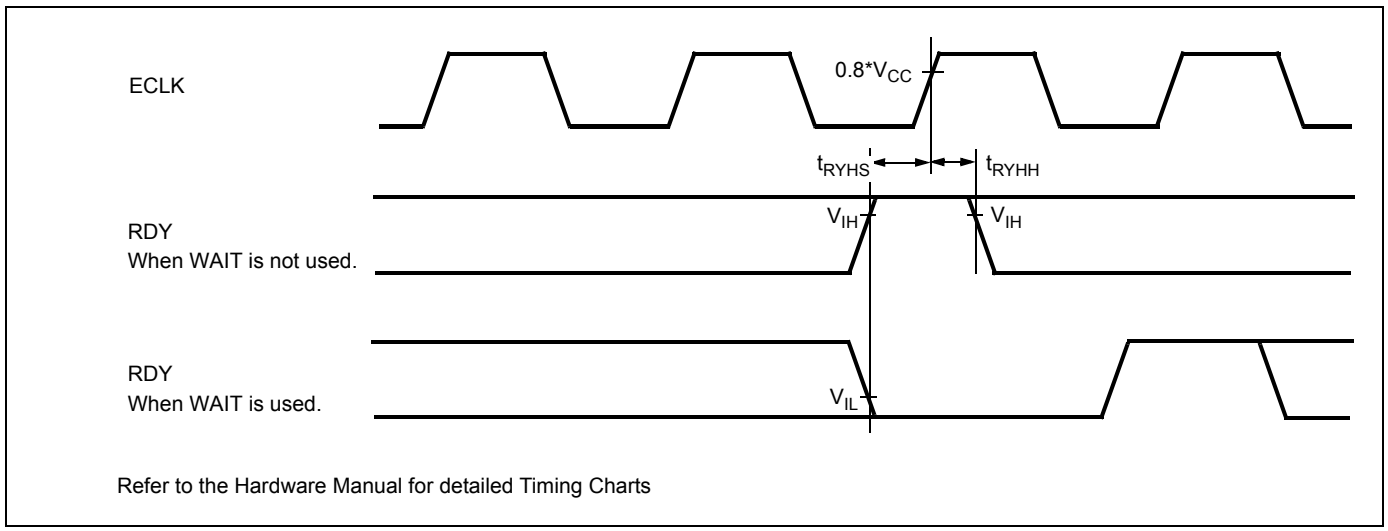
(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current for active Clock modulator	$I_{CCCLOMO}$	Clock modulator enabled (CMCR:PDX = 1)	-	3	4.5	mA	Must be added to all current above
Flash Write/Erase current	$I_{CCFLASH}$	Current for one Flash module	-	15	40	mA	Must be added to all current above
	$I_{CCDFLASH}$	Current for one Data Flash module		10	20	mA	Must be added to all current above
Input capacitance	C_{IN}	-	-	5	15	pF	Other than C, AV_{CC}, AV_{SS}, AVRH, AVRL, V_{CC}, V_{SS}
[1]: The power supply current is measured with a 4MHz external clock connected to the Main oscillator and a 32kHz external clock connected to the Sub oscillator. See chapter “Standby mode and voltage regulator control circuit” of the Hardware Manual for further details about voltage regulator control.							

14.4.8 Bus Timing (Read)

(T_A = –40°C to +125°C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
ALE pulse width	t_{LHLL}	ALE	EACL:STS=0 and EACL:ACE=0	$t_{CYC}/2 - 5$	-	ns	
			EACL:STS=1	$t_{CYC} - 5$	-		
			EACL:STS=0 and EACL:ACE=1	$3t_{CYC}/2 - 5$	-		
Valid address ⇒ ALE ↓ time	t_{AVLL}	ALE, A[23:16],	EACL:STS=0 and EACL:ACE=0	$t_{CYC} - 15$	-	ns	
			EACL:STS=1 and EACL:ACE=0	$3t_{CYC}/2 - 15$	-		
			EACL:STS=0 and EACL:ACE=1	$2t_{CYC} - 15$	-		
			EACL:STS=1 and EACL:ACE=1	$5t_{CYC}/2 - 15$	-		
	t_{ADVLL}	ALE,AD[15:0]	EACL:STS=0 and EACL:ACE=0	$t_{CYC}/2 - 15$	-	ns	
			EACL:STS=1 and EACL:ACE=0	$t_{CYC} - 15$	-		
			EACL:STS=0 and EACL:ACE=1	$3t_{CYC}/2 - 15$	-		
			EACL:STS=1 and EACL:ACE=1	$2t_{CYC} - 15$	-		
ALE ↓ ⇒ Address valid time	t_{LLAX}	ALE, AD[15:0]	EACL:STS=0	$t_{CYC}/2 - 15$	-	ns	
			EACL:STS=1	-15	-		
Valid address ⇒ RDX ↓ time	t_{AVRL}	RDX, A[23:16]	EACL:ACE=0	$3t_{CYC}/2 - 15$	-	ns	
			EACL:ACE=1	$5t_{CYC}/2 - 15$	-		
	t_{ADVRL}	RDX, AD[15:0]	EACL:ACE=0	$t_{CYC} - 15$	-	ns	
			EACL:ACE=1	$2t_{CYC} - 15$	-		
Valid address ⇒ Valid data input	t_{AVDV}	A[23:16], AD[15:0]	EACL:ACE=0	-	$3t_{CYC} - 55$	ns	w/o cycle extension
			EACL:ACE=1	-	$4t_{CYC} - 55$		
	t_{ADVDV}	AD[15:0]	EACL:ACE=0	-	$5t_{CYC}/2 - 55$	ns	w/o cycle extension
			EACL:ACE=1	-	$7t_{CYC}/2 - 55$		
RDX pulse width	t_{RLRH}	RDX	-	$3\ t_{CYC}/2 - 5$	-	ns	w/o cycle extension
RDX ↓ ⇒ Valid data input	t_{RLDV}	RDX, AD[15:0]	-	-	$3\ t_{CYC}/2 - 50$	ns	w/o cycle extension
RDX ↑ ⇒ Data hold time	t_{RHDX}	RDX, AD[15:0]	-	0	-	ns	
Address valid ⇒ Data hold time	t_{AXDX}	A[23:16], AD[15:0]	-	0	-	ns	



Refer to the Hardware Manual for detailed Timing Charts

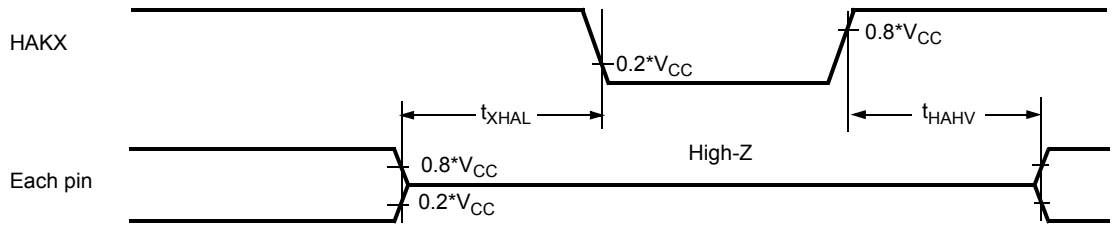
14.4.11 Hold Timing

(T_A = –40°C to +125°C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min	Max		
Pin floating ⇒ HAKX ↓ time	t_{XHAL}	HAKX	-	t_{CYC} – 20	t_{CYC} + 20	ns	
HAKX ↑ time ⇒ Pin valid time	t_{HAHV}	HAKX		t_{CYC} – 20	t_{CYC} + 20	ns	

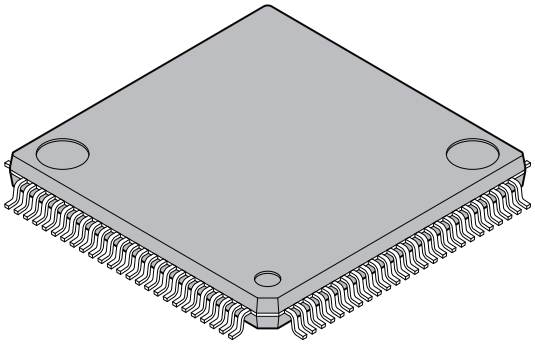
(T_A = –40°C to +125°C, V_{CC} = 3.0 to 4.5V, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min	Max		
Pin floating ⇒ HAKX ↓ time	t_{XHAL}	HAKX	-	t_{CYC} – 25	t_{CYC} + 25	ns	
HAKX ↑ time ⇒ Pin valid time	t_{HAHV}	HAKX		t_{CYC} – 25	t_{CYC} + 25	ns	



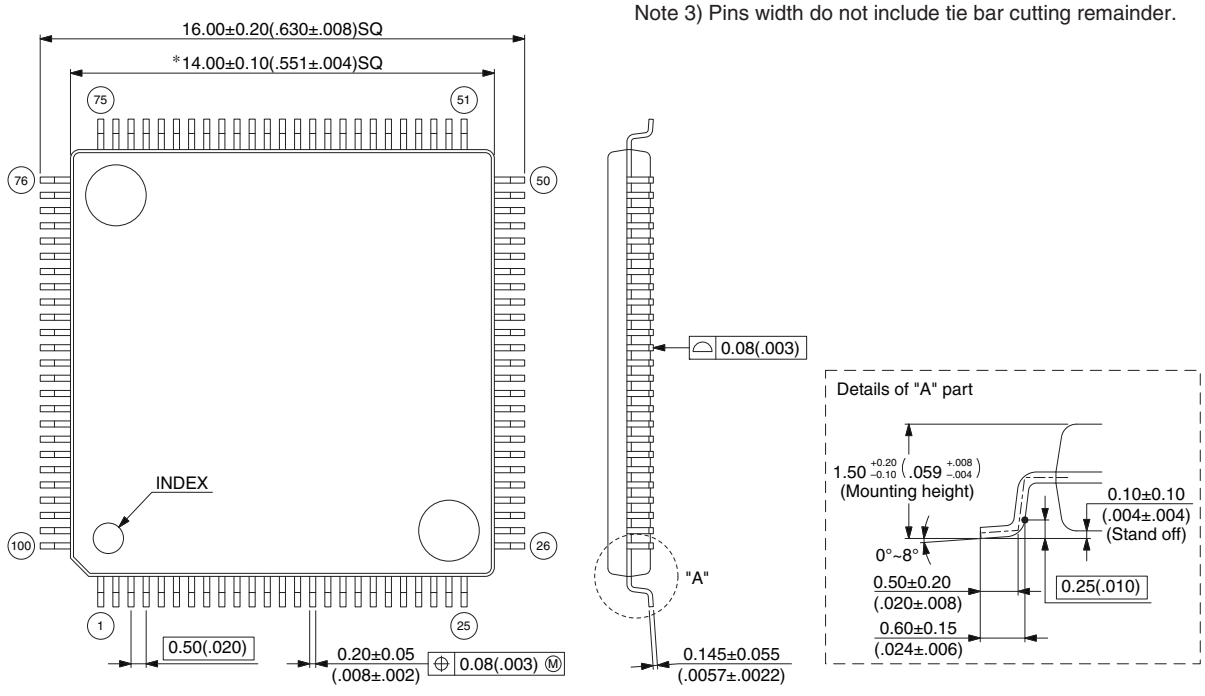
Refer to the Hardware Manual for detailed Timing Charts

16. Package Dimension MB96(F)34x LQFP 100P

100-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	14.0 mm × 14.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm Max
	Weight	0.65 g
(FPT-100P-M20)	Code (Reference)	P-LFQFP100-14×14-0.50

100-pin plastic LQFP
(FPT-100P-M20)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



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Dimensions in mm (inches).
Note: The values in parentheses are reference values

18.2 MCU without CAN Controller

Part number	Flash/ROM	Subclock	Package
MB96F346ASB PQC-GSE2	Flash A (288KB)	No	100 pin Plastic QFP (FPT-100P-M22)
MB96F346AWB PQC-GSE2		Yes	
MB96F346ASB PMC-GSE2		No	100 pin Plastic LQFP (FPT-100P-M20)
MB96F346AWB PMC-GSE2		Yes	
MB96F347ASB PQC-GSE2	Flash A (416KB)	No	100 pin Plastic QFP (FPT-100P-M22)
MB96F347AWB PQC-GSE2		Yes	
MB96F347ASB PMC-GSE2		No	100 pin Plastic LQFP (FPT-100P-M20)
MB96F347AWB PMC-GSE2		Yes	
MB96F348ASB PQC-GSE2	Flash A (544KB)	No	100 pin Plastic QFP (FPT-100P-M22)
MB96F348AWB PQC-GSE2		Yes	
MB96F348ASB PMC-GSE2		No	100 pin Plastic LQFP (FPT-100P-M20)
MB96F348AWB PMC-GSE2		Yes	
MB96F348CSC PQC-GSE2	Flash A (544KB) Flash B (32KB)	No	100 pin Plastic QFP (FPT-100P-M22)
MB96F348CWC PQC-GSE2		Yes	
MB96F348CSC PMC-GSE2		No	100 pin Plastic LQFP (FPT-100P-M20)
MB96F348CWC PMC-GSE2		Yes	

[1]: These devices are under development and specification is preliminary. These products under development may change its specification without notice.

This datasheet is also valid for the following outdated devices:

MB96F346YSA, MB96F346RSA, MB96F346YWA, MB96F346RWA,
MB96F347YSA, MB96F347RSA, MB96F347YWA, MB96F347RWA,
MB96F348YSA, MB96F348RSA, MB96F348YWA, MB96F348RWA,
MB96F348TSB, MB96F348HSB, MB96F348TWB, MB96F348HWB,
MB96F346ASA, MB96F346AWA,
MB96F347ASA, MB96F347AWA,
MB96F348ASA, MB96F348AWA,
MB96F348CSB, MB96F348CWB

Revision	Date	Modification
9	2009-01-09	■ Format adjusted to official Cypress datasheet standard (mainly style changes and official notes and disclaimer added) ■ Numbering of Electrical Characteristics subchapters automated ■ Note about devices under development modified ■ I/O map: Note added about reserved addresses ■ ICCSPLL for CLKS1=96MHz mode: increased by 1mA ■ Serial programming interface: Note about handshaking pins improved ■ specified AD converter channel offset to 4LSB ■ package code of MB96V300 corrected in ordering information ■ Added voltage condition to pull-up resistance spec ■ Lineup: Term “Data Flash” replaced by “independent 32KB Flash” ■ Ordering information: column “Independent 32KB Data Flash” replaced by new column “Flash/ROM”, column “Remarks” removed ■ Official package dimension drawing with additional notes added ■ Empty pages removed ■ Alarm comparator: Power supply current max values increased, comparison time reduced, mode transition time and power-up stabilization time newly added ■ Handling devices: Notes added about Serial communication and about using ceramic resonators. ■ Feature list and AC Characteristics: 16MHz maximum frequency is valid for crystal oscillators. For resonators, maximum frequency depends on Q-factor ■ AC characteristics: PLL phase skew spec added, CLKVCO min=64MHz ■ VOL3 spec improved: spec valid for 3mA load for full Vcc range ■ MB96F345 added ■ Preliminary DC spec of MB96345/346 added ■ Permitted power dissipation of Flash devices in QFP package improved ■ C-Pin cap spec updated: 4.7uF-10uF capacitor with tolerance permitted ■ “Preliminary” watermark removed
10	To be released	■ I/O map: IOABK0-5 added at address 000A00H-000A05H ■ Ordering Information: Suffix “A” added to all MB96F345 device versions ■ AD converter I_{AIN} spec improved: 1uA valid up to 105deg, 1.2uA above 105deg