Infineon Technologies - MB96F348RSAPQCR-GSE2 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	56MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, LVR, POR, PWM, WDT
Number of I/O	82
Program Memory Size	544KB (544K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-PQFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f348rsapqcr-gse2

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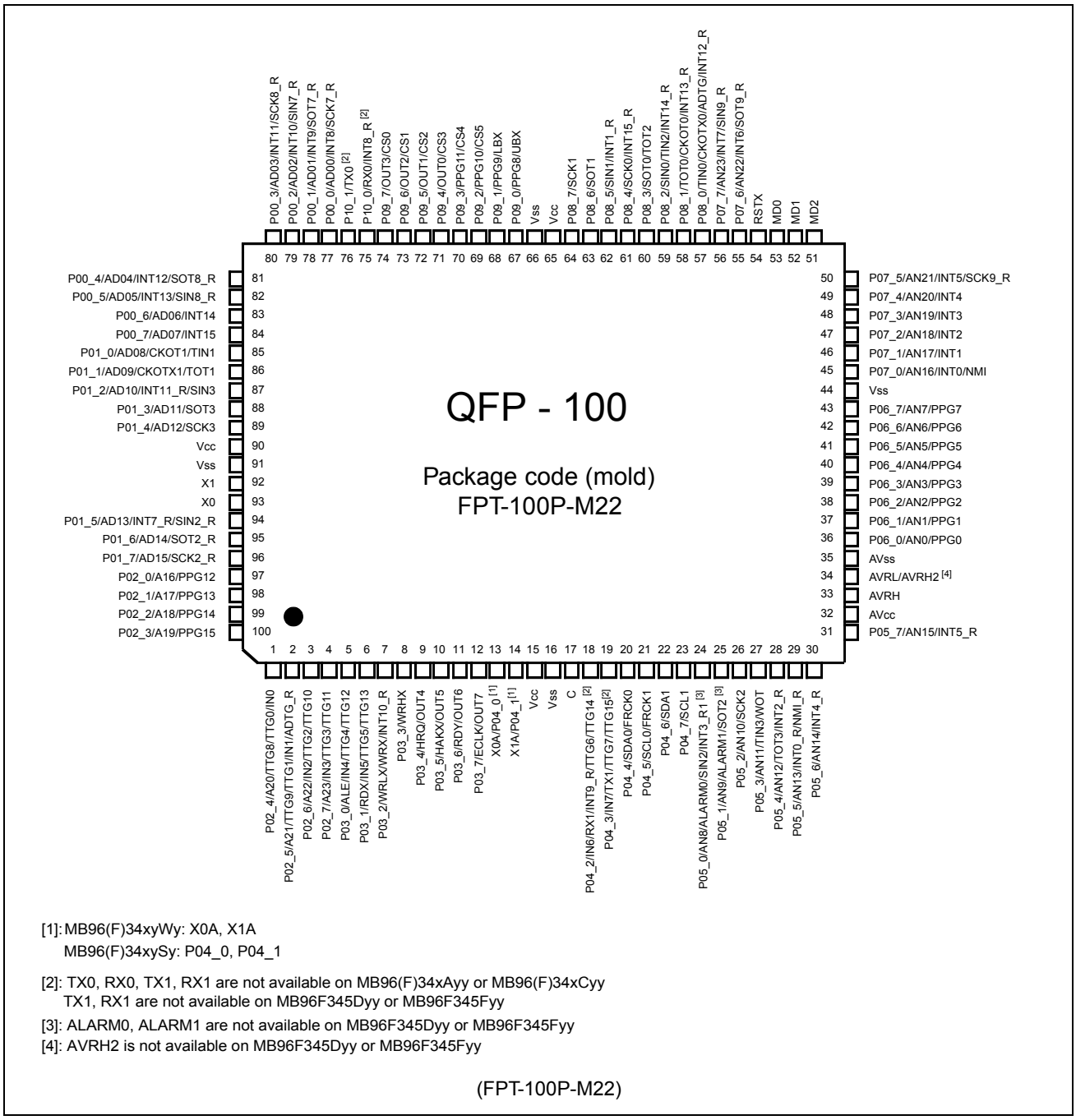
3. Pin Assignments

Figure 2. Pin assignment of MB96(F)34x (FPT-100P-M22)



[1]: MB96(F)34xyWy: X0A, X1A
MB96(F)34xySy: P04_0, P04_1

[2]: TX0, RX0, TX1, RX1 are not available on MB96(F)34xAyy or MB96(F)34xCyy
TX1, RX1 are not available on MB96F345Dyy or MB96F345Fyy

[3]: ALARM0, ALARM1 are not available on MB96F345Dyy or MB96F345Fyy

[4]: AVRH2 is not available on MB96F345Dyy or MB96F345Fyy

(FPT-100P-M22)

Remark:

MB96(F)34x products are pin-compatible to F^{2}MC-16LX family MB90340 series.

8. User ROM Memory Map For Flash Devices

MB96F345D
MB96F345F

Alternative mode CPU address	Flash memory mode address	Flash size 160kByte +64KByte Data Flash	
$FF:FFFF_H$ $FF:0000_H$	$3F:FFFF_H$ $3F:0000_H$	S39 - 64K	Flash A
$FE:FFFF_H$ $FE:0000_H$	$3E:FFFF_H$ $3E:0000_H$	S38 - 64K	
$FD:FFFF_H$ $FD:0000_H$	$3D:FFFF_H$ $3D:0000_H$	External bus	
$FC:FFFF_H$ $FC:0000_H$	$3C:FFFF_H$ $3C:0000_H$		
$FB:FFFF_H$ $FB:0000_H$	$3B:FFFF_H$ $3B:0000_H$		
$FA:FFFF_H$ $FA:0000_H$	$3A:FFFF_H$ $3A:0000_H$		
$F9:FFFF_H$ $F9:0000_H$	$39:FFFF_H$ $39:0000_H$		
$F8:FFFF_H$ $F8:0000_H$	$38:FFFF_H$ $38:0000_H$		
$F7:FFFF_H$ $F7:0000_H$	$37:FFFF_H$ $37:0000_H$		
$F6:FFFF_H$ $F6:0000_H$	$36:FFFF_H$ $36:0000_H$		
$F5:FFFF_H$ $F5:0000_H$	$35:FFFF_H$ $35:0000_H$		
$F4:FFFF_H$ $F4:0000_H$	$34:FFFF_H$ $34:0000_H$		
$F3:FFFF_H$ $F3:0000_H$	$33:FFFF_H$ $33:0000_H$		
$F2:FFFF_H$ $F2:0000_H$	$32:FFFF_H$ $32:0000_H$		
$F1:FFFF_H$ $F1:0000_H$	$31:FFFF_H$ $31:0000_H$		
$F0:FFFF_H$ $F0:0000_H$	$30:FFFF_H$ $30:0000_H$		
$E0:FFFF_H$ $E0:0000_H$			
$DF:FFFF_H$ $DF:8000_H$		Reserved	
$DF:7FFF_H$ $DF:6000_H$	$1F:7FFF_H$ $1F:6000_H$	SA3 - 8K	Flash A
$DF:5FFF_H$ $DF:4000_H$	$1F:5FFF_H$ $1F:4000_H$	SA2 - 8K	
$DF:3FFF_H$ $DF:2000_H$	$1F:3FFF_H$ $1F:2000_H$	SA1 - 8K	
$DF:1FFF_H$ $DF:0000_H$	$1F:1FFF_H$ $1F:0000_H$	SA0 - 8K [1]	
$DE:FFFF_H$ $DE:0000_H$		Reserved	
$0E:FFFF_H$ $0E:FF00_H$	$(0E:FFFF_H)$ $(0E:FF00_H)$	SDA0-256 [2]	Data Flash A
$0E:FEFF_H$ $0E:0000_H$		Reserved	
$0D:FFFF_H$ $0D:C000_H$	$(0F:FFFF_H)$ $(0F:C000_H)$	SDA4-16K	Data Flash A
$0D:BFFF_H$ $0D:8000_H$	$(0F:BFFF_H)$ $(0F:8000_H)$	SDA3-16K	
$0D:7FFF_H$ $0D:4000_H$	$(0F:7FFF_H)$ $(0F:4000_H)$	SDA2-16K	
$0D:3FFF_H$ $0D:0000_H$	$(0F:3FFF_H)$ $(0F:0000_H)$	SDA1-16K	
$0C:FFFF_H$ $0C:0000_H$		Reserved	

[1]: Sector SA0 contains the ROM Configuration Block RCBA at CPU address $DF:0000_H$ - $DF:007F_H$

[2]: Sector SDA0 contains the ROM Configuration Block RCBDA at CPU address $DE:FF00_H$ - $DE:FF2F_H$

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$0004B3_H$-$0004BB_H$	Reserved			-
$0004BC_H$	I/O Port P00 - External Pin State Register	EPSR00		R
$0004BD_H$	I/O Port P01 - External Pin State Register	EPSR01		R
$0004BE_H$	I/O Port P02 - External Pin State Register	EPSR02		R
$0004BF_H$	I/O Port P03 - External Pin State Register	EPSR03		R
$0004C0_H$	I/O Port P04 - External Pin State Register	EPSR04		R
$0004C1_H$	I/O Port P05 - External Pin State Register	EPSR05		R
$0004C2_H$	I/O Port P06 - External Pin State Register	EPSR06		R
$0004C3_H$	I/O Port P07 - External Pin State Register	EPSR07		R
$0004C4_H$	I/O Port P08 - External Pin State Register	EPSR08		R
$0004C5_H$	I/O Port P09 - External Pin State Register	EPSR09		R
$0004C6_H$	I/O Port P10 - External Pin State Register	EPSR10		R
$0004C7_H$-$0004CF_H$	Reserved			-
$0004D0_H$	ADC analog input enable register 0	ADER0		R/W
$0004D1_H$	ADC analog input enable register 1	ADER1		R/W
$0004D2_H$	ADC analog input enable register 2	ADER2		R/W
$0004D3_H$	ADC analog input enable register 3	ADER3		R/W
$0004D4_H$	ADC analog input enable register 4	ADER4		R/W
$0004D5_H$	Reserved			-
$0004D6_H$	Peripheral Resource Relocation Register 0	PRRR0		R/W
$0004D7_H$	Peripheral Resource Relocation Register 1	PRRR1		R/W
$0004D8_H$	Peripheral Resource Relocation Register 2	PRRR2		R/W
$0004D9_H$	Peripheral Resource Relocation Register 3	PRRR3		R/W
$0004DA_H$	Peripheral Resource Relocation Register 4	PRRR4		R/W
$0004DB_H$	Peripheral Resource Relocation Register 5	PRRR5		R/W
$0004DC_H$	Peripheral Resource Relocation Register 6	PRRR6		R/W
$0004DD_H$	Peripheral Resource Relocation Register 7	PRRR7		R/W
$0004DE_H$	Peripheral Resource Relocation Register 8	PRRR8		R/W
$0004DF_H$	Peripheral Resource Relocation Register 9	PRRR9		R/W
$0004E0_H$	RTC - Sub Second Register L	WTBRL0	WTBR0	R/W
$0004E1_H$	RTC - Sub Second Register M	WTBRH0		R/W
$0004E2_H$	RTC - Sub-Second Register H	WTBR1		R/W

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$0006EB_H$	External Bus - Area configuration register 5 High	EACH5		R/W
$0006EC_H$	External Bus - Area select register 2	EAS2		R/W
$0006ED_H$	External Bus - Area select register 3	EAS3		R/W
$0006EE_H$	External Bus - Area select register 4	EAS4		R/W
$0006EF_H$	External Bus - Area select register 5	EAS5		R/W
$0006F0_H$	External Bus - Mode register	EBM		R/W
$0006F1_H$	External Bus - Clock and Function register	EBCF		R/W
$0006F2_H$	External Bus - Address output enable register 0	EBAE0		R/W
$0006F3_H$	External Bus - Address output enable register 1	EBAE1		R/W
$0006F4_H$	External Bus - Address output enable register 2	EBAE2		R/W
$0006F5_H$	External Bus - Control signal register	EBCS		R/W
$0006F6_H$-$0006FF_H$	Reserved			-
000700_H	CAN0 - Control register Low	CTRLRL0	CTRLR0	R/W
000701_H	CAN0 - Control register High (reserved)	CTRLRH0		R
000702_H	CAN0 - Status register Low	STATRL0	STATR0	R/W
000703_H	CAN0 - Status register High (reserved)	STATRH0		R
000704_H	CAN0 - Error Counter Low (Transmit)	ERRCNTL0	ERRCNT0	R
000705_H	CAN0 - Error Counter High (Receive)	ERRCNTH0		R
000706_H	CAN0 - Bit Timing Register Low	BTRL0	BTR0	R/W
000707_H	CAN0 - Bit Timing Register High	BTRH0		R/W
000708_H	CAN0 - Interrupt Register Low	INTRL0	INTR0	R
000709_H	CAN0 - Interrupt Register High	INTRH0		R
$00070A_H$	CAN0 - Test Register Low	TESTRL0	TESTR0	R/W
$00070B_H$	CAN0 - Test Register High (reserved)	TESTRH0		R
$00070C_H$	CAN0 - BRP Extension register Low	BRPERL0	BRPER0	R/W
$00070D_H$	CAN0 - BRP Extension register High (reserved)	BRPERH0		R
$00070E_H$-$00070F_H$	Reserved			-
000710_H	CAN0 - IF1 Command request register Low	IF1CREQL0	IF1CREQ0	R/W
000711_H	CAN0 - IF1 Command request register High	IF1CREQH0		R/W
000712_H	CAN0 - IF1 Command Mask register Low	IF1CMSKL0	IF1CMSK0	R/W
000713_H	CAN0 - IF1 Command Mask register High (reserved)	IF1CMSKH0		R
000714_H	CAN0 - IF1 Mask 1 Register Low	IF1MSK1L0	IF1MSK10	R/W

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000715_H	CAN0 - IF1 Mask 1 Register High	IF1MSK1H0		R/W
000716_H	CAN0 - IF1 Mask 2 Register Low	IF1MSK2L0	IF1MSK20	R/W
000717_H	CAN0 - IF1 Mask 2 Register High	IF1MSK2H0		R/W
000718_H	CAN0 - IF1 Arbitration 1 Register Low	IF1ARB1L0	IF1ARB10	R/W
000719_H	CAN0 - IF1 Arbitration 1 Register High	IF1ARB1H0		R/W
$00071A_H$	CAN0 - IF1 Arbitration 2 Register Low	IF1ARB2L0	IF1ARB20	R/W
$00071B_H$	CAN0 - IF1 Arbitration 2 Register High	IF1ARB2H0		R/W
$00071C_H$	CAN0 - IF1 Message Control Register Low	IF1MCTRL0	IF1MCTR0	R/W
$00071D_H$	CAN0 - IF1 Message Control Register High	IF1MCTRH0		R/W
$00071E_H$	CAN0 - IF1 Data A1 Low	IF1DTA1L0	IF1DTA10	R/W
$00071F_H$	CAN0 - IF1 Data A1 High	IF1DTA1H0		R/W
000720_H	CAN0 - IF1 Data A2 Low	IF1DTA2L0	IF1DTA20	R/W
000721_H	CAN0 - IF1 Data A2 High	IF1DTA2H0		R/W
000722_H	CAN0 - IF1 Data B1 Low	IF1DTB1L0	IF1DTB10	R/W
000723_H	CAN0 - IF1 Data B1 High	IF1DTB1H0		R/W
000724_H	CAN0 - IF1 Data B2 Low	IF1DTB2L0	IF1DTB20	R/W
000725_H	CAN0 - IF1 Data B2 High	IF1DTB2H0		R/W
000726_H-$00073F_H$	Reserved			-
000740_H	CAN0 - IF2 Command request register Low	IF2CREQL0	IF2CREQ0	R/W
000741_H	CAN0 - IF2 Command request register High	IF2CREQH0		R/W
000742_H	CAN0 - IF2 Command Mask register Low	IF2CMSKL0	IF2CMSK0	R/W
000743_H	CAN0 - IF2 Command Mask register High (reserved)	IF2CMSKH0		R
000744_H	CAN0 - IF2 Mask 1 Register Low	IF2MSK1L0	IF2MSK10	R/W
000745_H	CAN0 - IF2 Mask 1 Register High	IF2MSK1H0		R/W
000746_H	CAN0 - IF2 Mask 2 Register Low	IF2MSK2L0	IF2MSK20	R/W
000747_H	CAN0 - IF2 Mask 2 Register High	IF2MSK2H0		R/W
000748_H	CAN0 - IF2 Arbitration 1 Register Low	IF2ARB1L0	IF2ARB10	R/W
000749_H	CAN0 - IF2 Arbitration 1 Register High	IF2ARB1H0		R/W
$00074A_H$	CAN0 - IF2 Arbitration 2 Register Low	IF2ARB2L0	IF2ARB20	R/W
$00074B_H$	CAN0 - IF2 Arbitration 2 Register High	IF2ARB2H0		R/W
$00074C_H$	CAN0 - IF2 Message Control Register Low	IF2MCTRL0	IF2MCTR0	R/W
$00074D_H$	CAN0 - IF2 Message Control Register High	IF2MCTRH0		R/W

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$00074E_H$	CAN0 - IF2 Data A1 Low	IF2DTA1L0	IF2DTA10	R/W
$00074F_H$	CAN0 - IF2 Data A1 High	IF2DTA1H0		R/W
000750_H	CAN0 - IF2 Data A2 Low	IF2DTA2L0	IF2DTA20	R/W
000751_H	CAN0 - IF2 Data A2 High	IF2DTA2H0		R/W
000752_H	CAN0 - IF2 Data B1 Low	IF2DTB1L0	IF2DTB10	R/W
000753_H	CAN0 - IF2 Data B1 High	IF2DTB1H0		R/W
000754_H	CAN0 - IF2 Data B2 Low	IF2DTB2L0	IF2DTB20	R/W
000755_H	CAN0 - IF2 Data B2 High	IF2DTB2H0		R/W
000756_H-$00077F_H$	Reserved			-
000780_H	CAN0 - Transmission Request 1 Register Low	TREQR1L0	TREQR10	R
000781_H	CAN0 - Transmission Request 1 Register High	TREQR1H0		R
000782_H	CAN0 - Transmission Request 2 Register Low	TREQR2L0	TREQR20	R
000783_H	CAN0 - Transmission Request 2 Register High	TREQR2H0		R
000784_H-$00078F_H$	Reserved			-
000790_H	CAN0 - New Data 1 Register Low	NEWDT1L0	NEWDT10	R
000791_H	CAN0 - New Data 1 Register High	NEWDT1H0		R
000792_H	CAN0 - New Data 2 Register Low	NEWDT2L0	NEWDT20	R
000793_H	CAN0 - New Data 2 Register High	NEWDT2H0		R
000794_H-$00079F_H$	Reserved			-
$0007A0_H$	CAN0 - Interrupt Pending 1 Register Low	INTPND1L0	INTPND10	R
$0007A1_H$	CAN0 - Interrupt Pending 1 Register High	INTPND1H0		R
$0007A2_H$	CAN0 - Interrupt Pending 2 Register Low	INTPND2L0	INTPND20	R
$0007A3_H$	CAN0 - Interrupt Pending 2 Register High	INTPND2H0		R
$0007A4_H$-$0007AF_H$	Reserved			-
$0007B0_H$	CAN0 - Message Valid 1 Register Low	MSGVAL1L0	MSGVAL10	R
$0007B1_H$	CAN0 - Message Valid 1 Register High	MSGVAL1H0		R
$0007B2_H$	CAN0 - Message Valid 2 Register Low	MSGVAL2L0	MSGVAL20	R
$0007B3_H$	CAN0 - Message Valid 2 Register High	MSGVAL2H0		R
$0007B4_H$-$0007CD_H$	Reserved			-
$0007CE_H$	CAN0 - Output enable register	COER0		R/W
$0007CF_H$-$0007FF_H$	Reserved			-
000800_H	CAN1 - Control register Low	CTRLRL1	CTRLR1	R/W

12. Interrupt Vector Table

Table 5: Interrupt vector table MB96(F)34x

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
0	$3FC_H$	CALLV0	No	-	
1	$3F8_H$	CALLV1	No	-	
2	$3F4_H$	CALLV2	No	-	
3	$3F0_H$	CALLV3	No	-	
4	$3EC_H$	CALLV4	No	-	
5	$3E8_H$	CALLV5	No	-	
6	$3E4_H$	CALLV6	No	-	
7	$3E0_H$	CALLV7	No	-	
8	$3DC_H$	RESET	No	-	
9	$3D8_H$	INT9	No	-	
10	$3D4_H$	EXCEPTION	No	-	
11	$3D0_H$	NMI	No	-	Non-Maskable Interrupt
12	$3CC_H$	DLY	No	12	Delayed Interrupt
13	$3C8_H$	RC_TIMER	No	13	RC Timer
14	$3C4_H$	MC_TIMER	No	14	Main Clock Timer
15	$3C0_H$	SC_TIMER	No	15	Sub Clock Timer
16	$3BC_H$	RESERVED	No	16	Reserved
17	$3B8_H$	EXTINT0	Yes	17	External Interrupt 0
18	$3B4_H$	EXTINT1	Yes	18	External Interrupt 1
19	$3B0_H$	EXTINT2	Yes	19	External Interrupt 2
20	$3AC_H$	EXTINT3	Yes	20	External Interrupt 3
21	$3A8_H$	EXTINT4	Yes	21	External Interrupt 4
22	$3A4_H$	EXTINT5	Yes	22	External Interrupt 5
23	$3A0_H$	EXTINT6	Yes	23	External Interrupt 6
24	$39C_H$	EXTINT7	Yes	24	External Interrupt 7
25	398_H	EXTINT8	Yes	25	External Interrupt 8
26	394_H	EXTINT9	Yes	26	External Interrupt 9
27	390_H	EXTINT10	Yes	27	External Interrupt 10
28	$38C_H$	EXTINT11	Yes	28	External Interrupt 11
29	388_H	EXTINT12	Yes	29	External Interrupt 12

14. Electrical Characteristics

14.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	V_{SS} - 0.3	V_{SS} + 6.0	V	
	AV_{CC}	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_{CC} = AV_{CC}$ [1]
AD Converter voltage references	AVRH, AVRL	V_{SS} - 0.3	V_{SS} + 6.0	V	$AV_{CC} \geq AVRH$, $AV_{CC} \geq AVRL$, $AVRH > AVRL$, $AVRL \geq AV_{SS}$
Input voltage	V_I	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_I \leq V_{CC}$ + 0.3V [2]
Output voltage	V_O	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_O \leq V_{CC}$ + 0.3V [2]
Maximum Clamp Current	I_{CLAMP}	-4.0	+4.0	mA	Applicable to general purposeI/O pins [3]
Total Maximum Clamp Current	$\Sigma\|I_{CLAMP}\|$	-	40	mA	Applicable to general purposeI/O pins [3]
“L” level maximum output current	I_{OL1}	-	15	mA	Normal outputs with driving strength set to 5mA
“L” level average output current	I_{OLAV1}	-	5	mA	Normal outputs with driving strength set to 5mA
“L” level maximum overall output current	ΣI_{OL1}	-	100	mA	Normal outputs
“L” level average overall output current	ΣI_{OLAV1}	-	50	mA	Normal outputs
”H” level maximum output current	I_{OH1}	-	-15	mA	Normal outputs with driving strength set to 5mA
”H” level average output current	I_{OHAV1}	-	-5	mA	Normal outputs with driving strength set to 5mA
”H” level maximum overall output current	ΣI_{OH1}	-	-100	mA	Normal outputs
”H” level average overall output current	ΣI_{OHAV1}	-	-50	mA	Normal outputs
Permitted Power dissipation (Flash devices in QFP package) [4]	P_D	-	430[5]	mW	T_A=105°C
		-	750[5]	mW	T_A=90°C
		-	540[5]	mW	T_A=125°C, no Flash program/erase [6]
Permitted Power dissipation (MB96F346/F347/F348 in LQFP package) [4]	P_D	-	375[5]	mW	T_A=105°C
		-	750[5]	mW	T_A=85°C
		-	470[5]	mW	T_A=125°C, no Flash program/erase [6]
		-	560[5]	mW	T_A=120°C, no Flash program/erase [6]
Permitted Power dissipation (MB96F345 in LQFP package) [4]	P_D	-	335[5]	mW	T_A=105°C
		-	670[5]	mW	T_A=85°C
		-	840[5]	mW	T_A=75°C
		-	420[5]	mW	T_A=125°C, no Flash program/erase [6]
		-	590[5]	mW	T_A=115°C, no Flash program/erase [6]

14.3 DC characteristics

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input H voltage	V_{IH}	Port inputs Pnn_m	CMOS Hysteresis 0.8/0.2 input selected	0.8 V_{CC}	-	V_{CC} + 0.3	V	
			CMOS Hysteresis 0.7/0.3 input selected	0.7 V_{CC}	-	V_{CC} + 0.3	V	$V_{CC} \geq 4.5V$
				0.74 V_{CC}	-	V_{CC} + 0.3	V	$V_{CC} < 4.5V$
			AUTOMOTIVE Hysteresis input selected	0.8 V_{CC}	-	V_{CC} + 0.3	V	
			TTL input selected	2.0	-	V_{CC} + 0.3	V	
	V_{IHX0F}	X0	External clock in “Fast Clock Input mode”	0.8 V_{CC}	-	V_{CC} + 0.3	V	Not available in MB96F34xY/R/AxA
	V_{IHX0S}	X0,X1, X0A,X1A	External clock in “oscillation mode”	2.5	-	V_{CC} + 0.3	V	
	V_{IHR}	RSTX	-	0.8 V_{CC}	-	V_{CC} + 0.3	V	CMOS Hysteresis input
	V_{IHM}	MD2-MD0	-	V_{CC} - 0.3	-	V_{CC} + 0.3	V	
Input L voltage	V_{IL}	Port inputs Pnn_m	CMOS Hysteresis 0.8/0.2 input selected	V_{SS} - 0.3	-	0.2 V_{CC}	V	
			CMOS Hysteresis 0.7/0.3 input selected	V_{SS} - 0.3	-	0.3 V_{CC}	V	
			AUTOMOTIVE Hysteresis input selected	V_{SS} - 0.3	-	0.5 V_{CC}	V	$V_{CC} \geq 4.5V$
				V_{SS} - 0.3	-	0.46 V_{CC}		$V_{CC} < 4.5V$
			TTL input selected	V_{SS} - 0.3	-	0.8	V	
	V_{ILX0F}	X0	External clock in “Fast Clock Input mode”	V_{SS} - 0.3	-	0.2 V_{CC}	V	Not available in MB96F34xY/R/AxA
	V_{ILX0S}	X0,X1, X0A,X1A	External clock in “oscillation mode”	V_{SS} - 0.3	-	0.4	V	
	V_{ILR}	RSTX	-	V_{SS} - 0.3	-	0.2 V_{CC}	V	CMOS Hysteresis input
	V_{ILM}	MD2-MD0	-	V_{SS} - 0.3	-	V_{SS} + 0.3	V	
Output H voltage	V_{OH2}	Normal outputs	$4.5V \leq V_{CC} \leq 5.5V$, I_{OH} = -2mA / $3.0V \leq V_{CC} < 4.5V$, I_{OH} = -1.6mA	V_{CC} - 0.5	-	-	V	Driving strength set to 2mA
	V_{OH5}	Normal outputs	$4.5V \leq V_{CC} \leq 5.5V$, I_{OH} = -5mA / $3.0V \leq V_{CC} < 4.5V$, I_{OH} = -3mA	V_{CC} - 0.5	-	-	V	Driving strength set to 5mA
	V_{OH3}	3mA outputs	$4.5V \leq V_{CC} \leq 5.5V$, I_{OH} = -3mA / $3.0V \leq V_{CC} < 4.5V$, I_{OH} = -2mA	V_{CC} - 0.5	-	-	V	

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

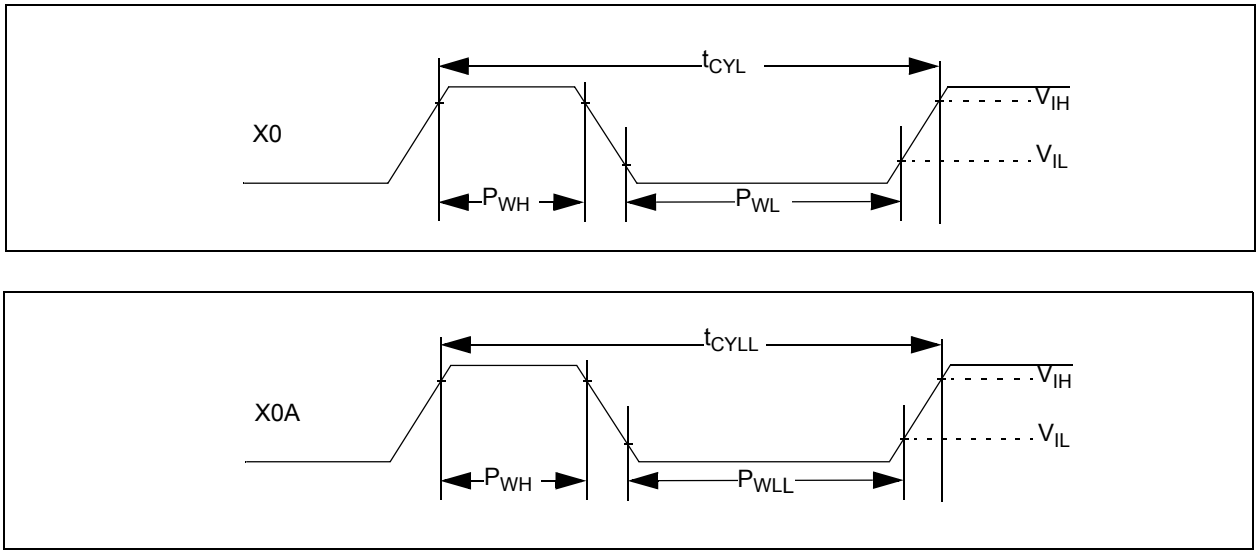
Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Timer modes[1]	I_{CCTRCL}	RC Timer mode with CLKRC = 100kHz, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)	+25°C	0.3	0.45	mA	MB96F346/F347/F348
			+125°C	0.8	3.2		
			+25°C	0.08	0.15	mA	MB96F345
			+125°C	0.58	2.95		
			+25°C	0.3	0.45	mA	MB96345/346
			+125°C	0.8	2.2		
		RC Timer mode with CLKRC = 100kHz, SMCR:LPMSS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode)	+25°C	0.05	0.1	mA	Flash devices
			+125°C	0.55	2.85		
			+25°C	0.05	0.1	mA	MB96345/346
			+125°C	0.55	1.85		
	I_{CCTSUB}	Sub Timer mode with CLKSC = 32kHz (CLKMC, CLKPLL and CLKRC stopped)	+25°C	0.03	0.1	mA	Flash devices
			+125°C	0.53	2.85		
			+25°C	0.03	0.1	mA	MB96345/346
			+125°C	0.53	1.85		
Power supply current in Stop Mode	I_{CCH}	VRCR:LPMB[2:0] = 110_B (Core voltage at 1.8V)	+25°C	0.02	0.08	mA	Flash devices
			+125°C	0.52	2.8		
			+25°C	0.02	0.08	mA	MB96345/346
			+125°C	0.52	1.8		
		VRCR:LPMB[2:0] = 000_B (Core voltage at 1.2V)	+25°C	0.015	0.06	mA	Flash devices
			+125°C	0.4	2.3		
			+25°C	0.015	0.06	mA	MB96345/346
			+125°C	0.4	1.4		
Power supply current for active Low Voltage detector	I_{CCLVD}	Low voltage detector enabled (RCR:LVDE = 1)	-	5	10	µA	MB96F345 Must be added to all current above
			+25°C	90	140	µA	Other devices Must be added to all current above
			+125°C	100	150		

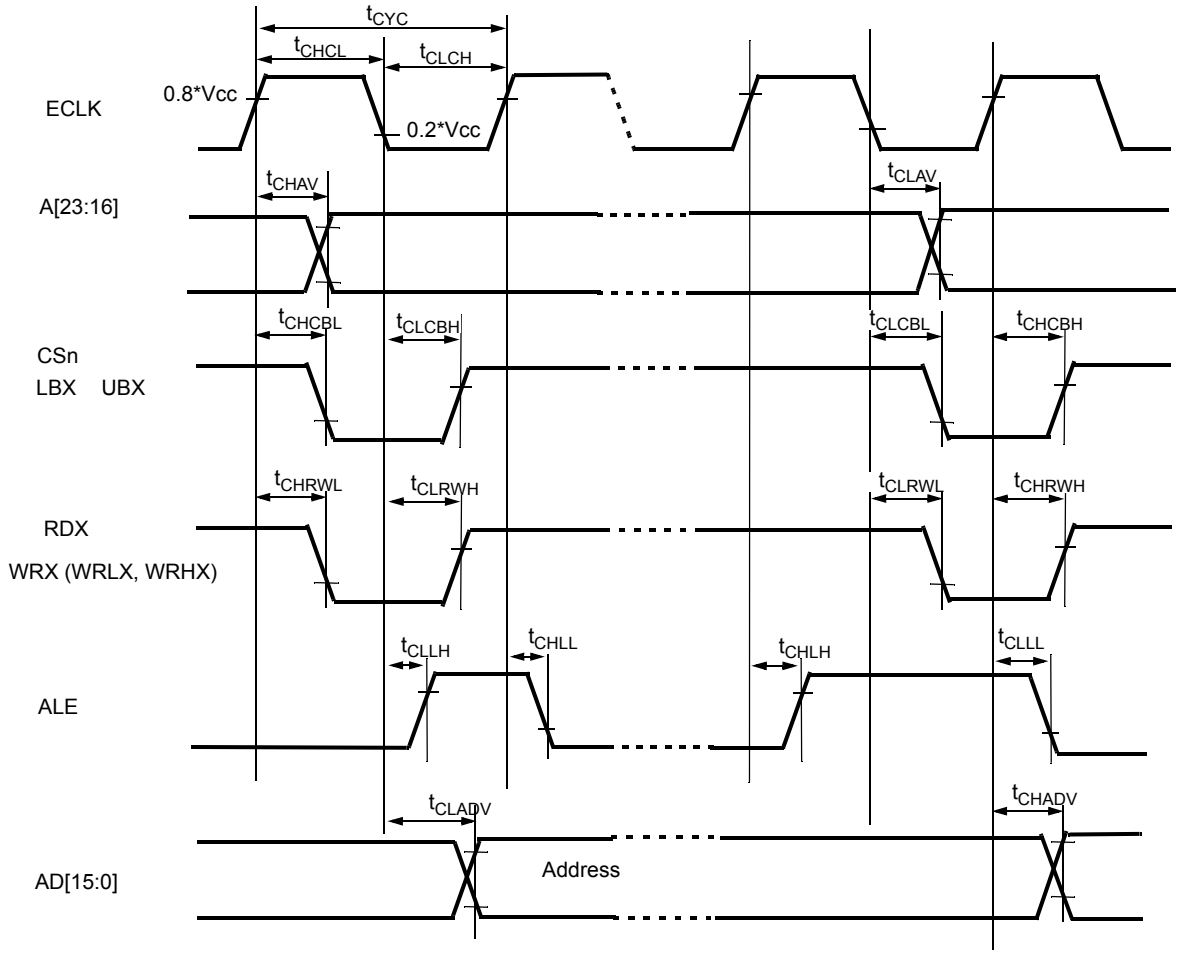
14.4 AC Characteristics

14.4.1 Source Clock timing

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_C	X0, X1	3	-	16	MHz	When using a crystal oscillator, PLL off
			0	-	16	MHz	When using an opposite phase external clock, PLL off
			3.5	-	16	MHz	When using a crystal oscillator or opposite phase external clock, PLL on
Clock frequency	f_{FCI}	X0	0	-	56	MHz	When using a single phase external clock in “Fast Clock Input mode” (not available in MB96F34xY/R/AxA), PLL off
			3.5	-	56	MHz	When using a single phase external clock in “Fast Clock Input mode” (not available in MB96F34xY/R/AxA), PLL on
Clock frequency	f_{CL}	X0A, X1A	32	32.768	100	kHz	When using an oscillation circuit
			0	-	100	kHz	When using an opposite phase external clock
		X0A	0	-	50	kHz	When using a single phase external clock
Clock frequency	f_{CR}	-	50	100	200	kHz	When using slow frequency of RC oscillator
			1	2	4	MHz	When using fast frequency of RC oscillator
PLL Clock frequency	f_{CLKVCO}	-	64	-	200	MHz	Permitted VCO output frequency of PLL (CLKVCO)
PLL Phase Jitter	T_{PSKEW}	-	-	-	± 5	ns	For CLKMC (PLL input clock) ≥ 4MHz
Input clock pulse width	P_{WH}, P_{WL}	X0,X1	8	-	-	ns	Duty ratio is about 30% to 70%
Input clock pulse width	P_{WHL}, P_{WLL}	X0A,X1A	5	-	-	µs	





Refer to the Hardware Manual for detailed Timing Charts

(T_A = –40°C to +125°C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
RDX ↑ ⇒ ALE ↑ time	t_{RHLH}	RDX, ALE	EACL:STS=1 and EACL:ACE=1	$3t_{CYC}/2 - 10$	-	ns	
			other ECL:STS, EACL:ACE setting	$t_{CYC}/2 - 10$	-		
Valid address ⇒ ECLK ↑ time	t_{AVCH}	A[23:16], ECLK	-	$t_{CYC} - 15$	-	ns	
	t_{ADVCH}	AD[15:0], ECLK		$t_{CYC}/2 - 15$	-		
RDX ↓ ⇒ ECLK ↑ time	t_{RLCH}	RDX, ECLK	-	$t_{CYC}/2 - 10$	-	ns	
ALE ↓ ⇒ RDX ↓ time	t_{LLRL}	ALE, RDX	EACL:STS=0	$t_{CYC}/2 - 10$	-	ns	
			EACL:STS=1	– 10	-		
ECLK↑ ⇒ Valid data input	t_{CHDV}	AD[15:0], ECLK	-	-	$t_{CYC} - 50$	ns	

(T_A = –40°C to +125°C, V_{CC} = 3.0 to 4.5V, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
ALE pulse width	t_{LHLL}	ALE	EACL:STS=0 and EACL:ACE=0	$t_{CYC}/2 - 8$	-	ns	
			EACL:STS=1	$t_{CYC} - 8$	-		
			EACL:STS=0 and EACL:ACE=1	$3t_{CYC}/2 - 8$	-		
Valid address ⇒ ALE ↓ time	t_{AVLL}	ALE, A[23:16],	EACL:STS=0 and EACL:ACE=0	$t_{CYC} - 20$	-	ns	
			EACL:STS=1 and EACL:ACE=0	$3t_{CYC}/2 - 20$	-		
			EACL:STS=0 and EACL:ACE=1	$2t_{CYC} - 20$	-		
			EACL:STS=1 and EACL:ACE=1	$5t_{CYC}/2 - 20$	-		
	t_{ADVLL}	ALE, AD[15:0]	EACL:STS=0 and EACL:ACE=0	$t_{CYC}/2 - 20$	-	ns	
			EACL:STS=1 and EACL:ACE=0	$t_{CYC} - 20$	-		
			EACL:STS=0 and EACL:ACE=1	$3t_{CYC}/2 - 20$	-		
			EACL:STS=1 and EACL:ACE=1	$2t_{CYC} - 20$	-		
ALE ↓ ⇒ Address valid time	t_{LLAX}	ALE, AD[15:0]	EACL:STS=0	$t_{CYC}/2 - 20$	-	ns	
			EACL:STS=1	-20	-		
Valid address ⇒ RDX ↓ time	t_{AVRL}	RDX, A[23:16]	EACL:ACE=0	$3t_{CYC}/2 - 20$	-	ns	
			EACL:ACE=1	$5t_{CYC}/2 - 20$	-		
	t_{ADVRL}	RDX, AD[15:0]	EACL:ACE=0	$t_{CYC} - 20$	-	ns	
			EACL:ACE=1	$2t_{CYC} - 20$	-		

(T_A = −40°C to +125°C, V_{CC} = 3.0 to 4.5V, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

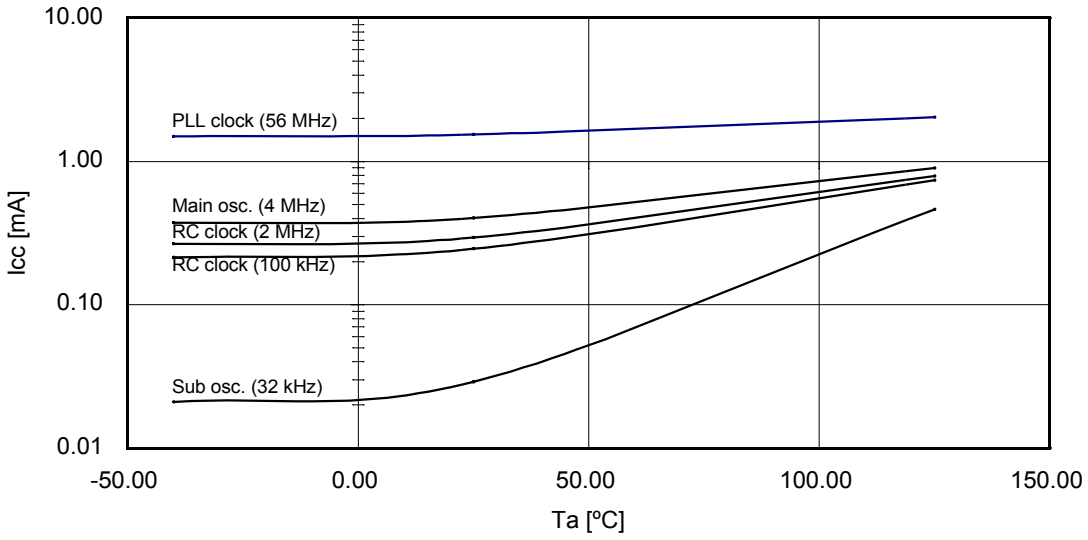
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
WRX pulse width	t_{WLWH}	WRX, WRXL, WRHX	-	t_{CYC} − 8	-	ns	w/o cycle extension
Valid data output ⇒ WRX ↑ time	t_{DVWH}	WRX, WRLX, WRHX, AD[15:0]	-	t_{CYC} − 25	-	ns	w/o cycle extension
WRX ↑ ⇒ Data hold time	t_{WHDX}	WRX, WRLX, WRHX, AD[15:0]	-	$t_{CYC}/2$ − 20	-	ns	
WRX ↑ ⇒ Address valid time	t_{WHAX}	WRX, WRLX, WRHX, A[23:16]	-	$t_{CYC}/2$ − 20	-	ns	
WRX ↑ ⇒ ALE ↑ time	t_{WHLH}	WRX, WRLX, WRHX, ALE	EBM:ACE=1 and EACL:STS=1	$2t_{CYC}$ − 15	-	ns	
			other EBM:ACE and EACL:STS setting	t_{CYC} − 15	-		
WRX ↓ ⇒ ECLK ↑ time	t_{WLCH}	WRX, WRLX, WRHX, ECLK	-	$t_{CYC}/2$ − 15	-	ns	
CSn ⇒ WRX time	t_{CSLWL}	WRX, WRLX, WRHX, CSn	EACL:ACE=0	-	$3t_{CYC}/2$ − 20	ns	
			EACL:ACE=1	-	$5t_{CYC}/2$ − 20		
WRX ⇒ CSn time	t_{WHCSH}	WRX, WRLX, WRHX, CSn	-	$t_{CYC}/2$ − 20	-	ns	

14.6 Alarm Comparator

(T_A = -40 °C to +125 °C, V_{CC} = AV_{CC} = 3.0V - 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Power supply current	I_{A5ALMF}	AV_{CC}	-	25	45	µA	Alarm comparator enabled in fast mode (one channel)
	I_{A5ALMS}		-	7	13	µA	Alarm comparator enabled in slow mode (one channel)
	I_{A5ALMH}		-	-	5	µA	Alarm comparator disabled
ALARM pin input current	I_{ALIN}	ALARM0, ALARM1	-1	-	+1	µA	T_A = 25 °C
			-3	-	+3	µA	T_A = 125 °C
ALARM pin input voltage range	V_{ALIN}		0	-	AV_{CC}	V	
External low threshold high->low transition	$V_{EVTL(H->L)}$		0.36 * AV_{CC} -0.25	0.36 * AV_{CC} -0.1	-	V	INTREF = 0
External low threshold low->high transition	$V_{EVTL(L->H)}$		-	0.36 * AV_{CC} +0.1	0.36 * AV_{CC} +0.25	V	
External high threshold high->low transition	$V_{EVTH(H->L)}$		0.78 * AV_{CC} -0.25	0.78 * AV_{CC} -0.1	-	V	
External high threshold low->high transition	$V_{EVTH(L->H)}$			0.78 * AV_{CC} +0.1	0.78 * AV_{CC} +0.25	V	
Internal low threshold high->low transition	$V_{IVTL(H->L)}$		0.9	1.1	-	V	INTREF = 1
Internal low threshold low->high transition	$V_{IVTL(L->H)}$		-	1.3	1.55	V	
Internal high threshold high->low transition	$V_{IVTH(H->L)}$		2.2	2.4	-	V	
Internal high threshold low->high transition	$V_{IVTH(L->H)}$		-	2.6	2.85	V	
Switching hysteresis	V_{HYS}		50	-	300	mV	
Comparison time	t_{COMPF}		-	0.1	1	µs	CMD = 1 (fast)
	t_{COMPS}		-	1	10	µs	CMD = 0 (slow)
Power-up stabilization time after enabling alarm comparator	t_{PD}		-	1	5	ms	Threshold levels specified above are not guaranteed within this time
Slow/Fast mode transition time	t_{CMD}		-	100	500	µs	

Timer mode



Stop mode

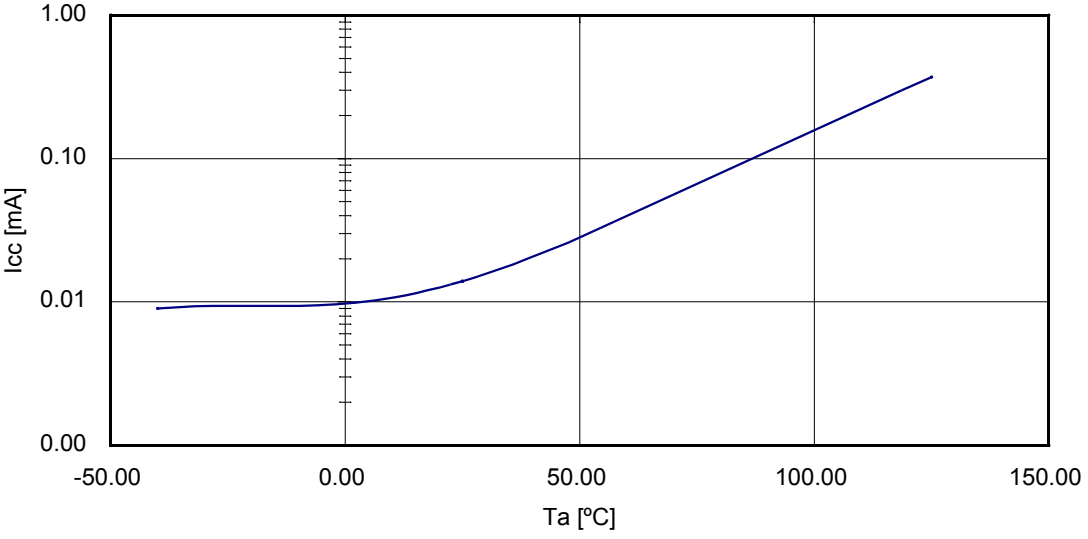
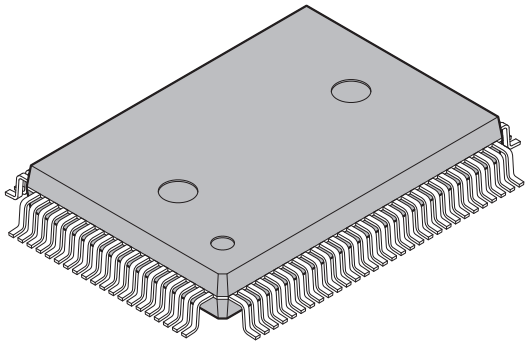


Table 6: Used settings

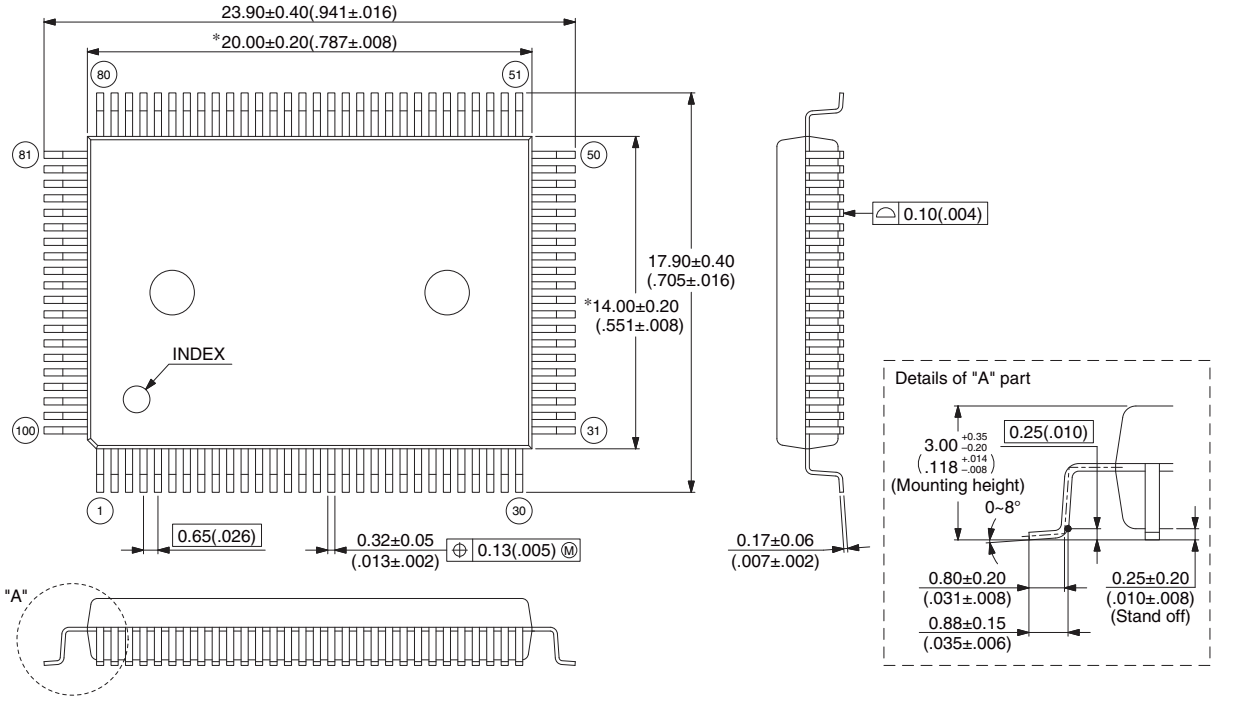
Mode	Selected Source Clock	Clock/Regulator Settings
Timer mode	PLL	CLKMC = 4 MHz, CLKPLL = 56 MHz (System clocks are stopped in this mode) Regulator in High Power Mode, Core Voltage = 1.9 V
	Main osc.	CLKMC = 4 MHz (System clocks are stopped in this mode) Regulator in High Power Mode, Core Voltage = 1.8 V
	RC clock fast	CLKRC = 2 MHz (System clocks are stopped in this mode) Regulator in High Power Mode, Core Voltage = 1.8 V
	RC clock slow	CLKRC = 100 kHz (System clocks are stopped in this mode) Regulator in High Power Mode, Core Voltage = 1.8 V
	Sub osc.	CLKSC = 100 kHz (System clocks are stopped in this mode) Regulator in Low Power Mode A, Core Voltage = 1.8 V
Stop mode	stopped	(All clocks are stopped in this mode) Regulator in Low Power Mode B, Core Voltage = 1.8 V

17. Package Dimension MB96(F)34x QFP 100P

100-pin plastic QFP		
	Lead pitch	0.65 mm
	Package width × package length	14.00 mm × 20.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	3.35 mm MAX
	Code (Reference)	P-QFP100-14×20-0.65
(FPT-100P-M22)		

100-pin plastic QFP
(FPT-100P-M22)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

19. Revision History

Revision	Date	Modification
Prelim 1	2007-05-07	Creation
Prelim 2	2007-05-10	External bus hold timing update
Prelim 3	2007-05-23	Electrical characteristics updates
Prelim 4	2007-08-02	Electrical characteristics updates, Product lineup, changes and ordering information
Prelim 5	2007-09-12	Addition of the electrical characteristic examples and the LVD characteristics specifications, updates of the DC characteristics. Pin circuit type drawing modifications.
Prelim 6	2007-11-21	LVD typo correction. Update of the DC characteristics. Typos corrections.
Prelim 7	2007-12-04	Absolute maximum rating asterisks numbering corrected. Typos page 59: Hardware -> Hardware. IO map table regenerated. Typos corrections. IO circuit drawings modified. Renaming of the Main/Satellite Flash into Flash memory A/B. Memory map reworked.
Prelim 8	2008-02-04	■ Satellite Flash -> 32kB Data Flash ■ MB96345 added (under development) ■ MB96F348 TSA/HSA/TWA/HWA removed (outdated devices) ■ Block diagram and pin assignment corrected (existing resource pins) ■ Pin function table corrected ■ I/O circuit type diagrams corrected ■ Memory map cleaned up ■ "Flash sector configuration" replaced by corrected "User ROM Memory map for Flash devices", “ROM configuration” replaced by “User ROM Memory map for Mask ROM devices” ■ Parallel Flash programming pinning removed ■ IO map table regenerated: ❒ Port register: Naming style corrected ❒ Memory control registers renamed (Main/Sat -> A/B) ❒ addresses after 000BFFh removed ■ Absolute maximum ratings: Pd and Ta specified more precisely ■ oscillator input levels in oscillation mode with external clock added ■ Run and Sleep mode currents: 96/48MHz and 72/36MHz settings added ■ Run mode current spec in 48/24MHz mode corrected ■ Maximum CLKS1/2 frequency for all devices correctly specified ■ Maximum CLKP2 for MB96F34xY/R/Axx corrected ■ External bus timings: missing conditions added and readability improved ■ Alarm comparator spec updated (transition voltages defined) ■ MB96V300A removed ■ Ordering information updated ■ Typos and formatting corrected