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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

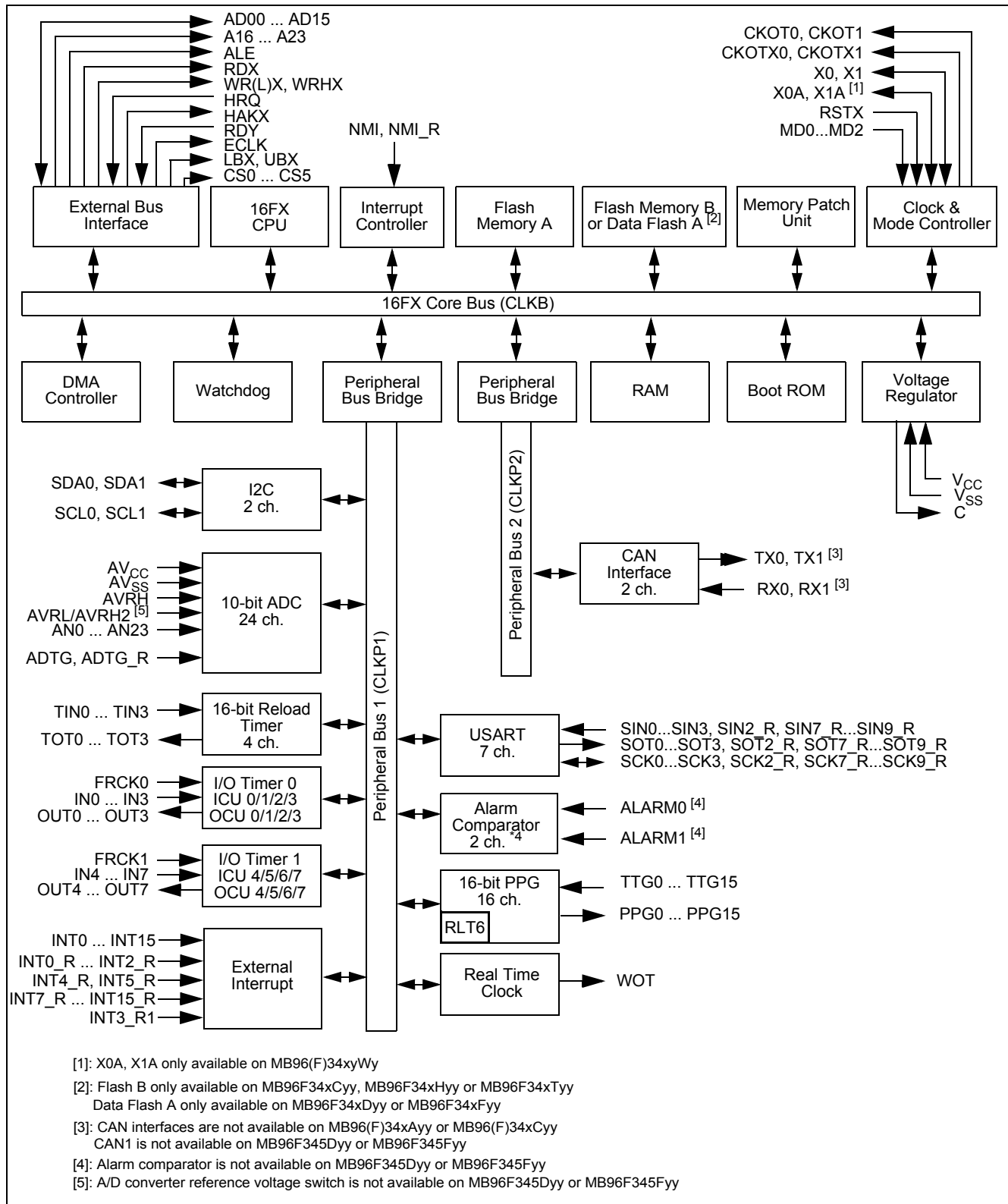
Details	
Product Status	Discontinued at Digi-Key
Core Processor	F ² MC-16FX
Core Size	16-Bit
Speed	56MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, LVR, POR, PWM, WDT
Number of I/O	82
Program Memory Size	544KB (544K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-fl.com/product-detail/infiniteon-technologies/mb96f348rsbpmc-gse2

Features	MB96V300B	MB96(F)34x
I ² C	2 channels	2 channels
A/D Converter	40 channels	24 channels
A/D Converter Reference Voltage switch	yes	yes (except MB96F345Dyy or MB96F345Fyy)
16-bit Reload Timer	6 channels + 1 channel (for PPG)	4 channels + 1 channel (for PPG)
16-bit Free-Running Timer	4 channels	2 channels
16-bit Output Compare	12 channels	8 channels
16-bit Input Capture	12 channels	8 channels
16-bit Programmable Pulse Generator	20 channels	16 channels
CAN Interface	5 channels	MB96(F)34xAyy or MB96(F)34xCyy: no MB96F345Dyy or MB96F345Fyy: 1 channel others: 2 channels
External Interrupts	16 channels	
Non-Maskable Interrupt	1 channel	
Real Time Clock	1	
I/O Ports	136	80 for part number with suffix "W", 82 for part number with suffix "S"
Alarm comparator	2 channels	MB96F345Dyy or MB96F345Fyy: no others: 2 channels
External bus interface	Yes	Yes (multiplexed address/data)
Chip select	6 signals	
Clock output function	2 channels	
Low voltage reset	Yes	
On-chip RC-oscillator	Yes	

[1]: These devices are under development and specification is preliminary. These products under development may change its specification without notice.

2. Block Diagram

Figure 1. Block diagram of MB96(F)34x



5. Pin Circuit Type

Table 2: Pin circuit types

FPT-100P-M20		FPT-100P-M22	
Pin no.	Circuit type ^[1]	Pin no.	Circuit type ^[1]
1-10	H	1-12	H
11,12	B ^[2]	13, 14	B ^[2]
11,12	H ^[3]	13, 14	H ^[3]
13,14	Supply	15,16	Supply
15	F	17	F
16,17	H	18,19	H
18-21	N	20-23	N
22-29	I	24-31	I
30	Supply	32	Supply
31-32	G	33-34	G
33	Supply	35	Supply
34 to 41	I	36 to 43	I
42	Supply	44	Supply
43 to 48	I	45 to 50	I
49 to 51	C	51 to 53	C
52	E	54	E
53 to 54	I	55 to 56	I
55 to 62	H	57 to 64	H
63, 64	Supply	65, 66	Supply
65 to 87	H	67 to 89	H
88,89	Supply	90, 91	Supply
90, 91	A	92, 93	A
92-100	H	94 to 100	H

[1]: Please refer to “[I/O Circuit Type](#)” for details on the I/O circuit types

[2]: Devices with suffix “W”

[3]: Devices without suffix “W”

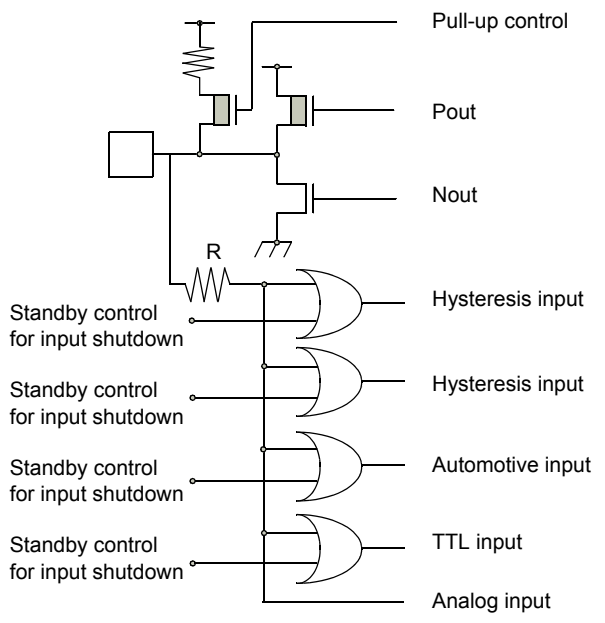
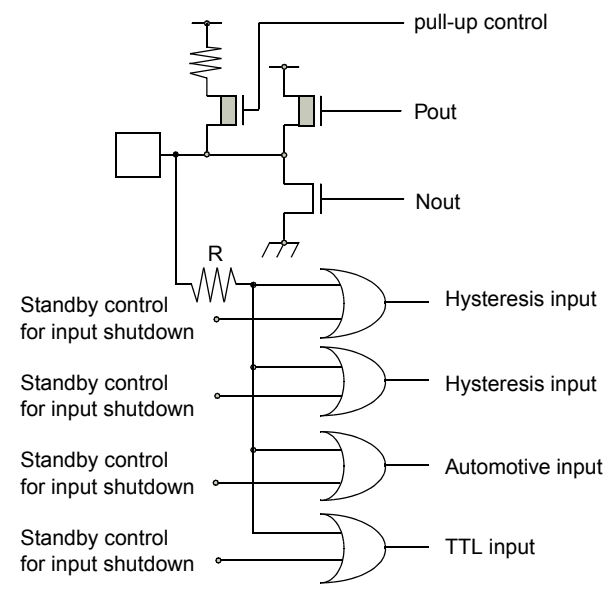
Type	Circuit	Remarks
I	 Pull-up control Pout Nout R Standby control for input shutdown Hysteresis input Hysteresis input Automotive input TTL input Analog input	■ CMOS level output (programmable $I_{OL} = 5\text{mA}$, $I_{OH} = -5\text{mA}$ and $I_{OL} = 2\text{mA}$, $I_{OH} = -2\text{mA}$) ■ 2 different CMOS hysteresis inputs with input shutdown function * ■ Automotive input with input shutdown function ■ TTL input with input shutdown function * ■ Programmable pull-up resistor: 50kΩ approx. ■ Analog input *MB96F345Dyy or MB96F345Fyy: Only Automotive input and CMOS hysteresis input (0.7/0.3) are supported
N	 pull-up control Pout Nout R Standby control for input shutdown Hysteresis input Hysteresis input Automotive input TTL input	■ CMOS level output ($I_{OL} = 3\text{mA}$, $I_{OH} = -3\text{mA}$) ■ 2 different CMOS hysteresis inputs with input shutdown function * ■ Automotive input with input shutdown function ■ TTL input with input shutdown function * ■ Programmable pull-up resistor: 50kΩ approx. *MB96F345Dyy or MB96F345Fyy: Only Automotive input and CMOS hysteresis input (0.7/0.3) are supported

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00002B _H	OCU0 - Compare Register			R/W
00002C _H	OCU1 - Compare Register		OCCP1	R/W
00002D _H	OCU1 - Compare Register			R/W
00002E _H	OCU2 - Output Compare Control Status	OCS2		R/W
00002F _H	OCU3 - Output Compare Control Status	OCS3		R/W
000030 _H	OCU2 - Compare Register		OCCP2	R/W
000031 _H	OCU2 - Compare Register			R/W
000032 _H	OCU3 - Compare Register		OCCP3	R/W
000033 _H	OCU3 - Compare Register			R/W
000034 _H	OCU4 - Output Compare Control Status	OCS4		R/W
000035 _H	OCU5 - Output Compare Control Status	OCS5		R/W
000036 _H	OCU4 - Compare Register		OCCP4	R/W
000037 _H	OCU4 - Compare Register			R/W
000038 _H	OCU5 - Compare Register		OCCP5	R/W
000039 _H	OCU5 - Compare Register			R/W
00003A _H	OCU6 - Output Compare Control Status	OCS6		R/W
00003B _H	OCU7 - Output Compare Control Status	OCS7		R/W
00003C _H	OCU6 - Compare Register		OCCP6	R/W
00003D _H	OCU6 - Compare Register			R/W
00003E _H	OCU7 - Compare Register		OCCP7	R/W
00003F _H	OCU7 - Compare Register			R/W
000040 _H	ICU0/ICU1 - Control Status Register	ICS01		R/W
000041 _H	ICU0/ICU1 - Edge register	ICE01		R/W
000042 _H	ICU0 - Capture Register Low	IPCPL0	IPCP0	R
000043 _H	ICU0 - Capture Register High	IPCPH0		R
000044 _H	ICU1 - Capture Register Low	IPCPL1	IPCP1	R
000045 _H	ICU1 - Capture Register High	IPCPH1		R
000046 _H	ICU2/ICU3 - Control Status Register	ICS23		R/W
000047 _H	ICU2/ICU3 - Edge register	ICE23		R/W
000048 _H	ICU2 - Capture Register Low	IPCPL2	IPCP2	R
000049 _H	ICU2 - Capture Register High	IPCPH2		R
00004A _H	ICU3 - Capture Register Low	IPCPL3	IPCP3	R

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000081 _H	PPG1 - Timer register			R
000082 _H	PPG1 - Period setting register		PCSR1	W
000083 _H	PPG1 - Period setting register			W
000084 _H	PPG1 - Duty cycle register		PDUT1	W
000085 _H	PPG1 - Duty cycle register			W
000086 _H	PPG1 - Control status register Low	PCNL1	PCN1	R/W
000087 _H	PPG1 - Control status register High	PCNH1		R/W
000088 _H	PPG2 - Timer register		PTMR2	R
000089 _H	PPG2 - Timer register			R
00008A _H	PPG2 - Period setting register		PCSR2	W
00008B _H	PPG2 - Period setting register			W
00008C _H	PPG2 - Duty cycle register		PDUT2	W
00008D _H	PPG2 - Duty cycle register			W
00008E _H	PPG2 - Control status register Low	PCNL2	PCN2	R/W
00008F _H	PPG2 - Control status register High	PCNH2		R/W
000090 _H	PPG3 - Timer register		PTMR3	R
000091 _H	PPG3 - Timer register			R
000092 _H	PPG3 - Period setting register		PCSR3	W
000093 _H	PPG3 - Period setting register			W
000094 _H	PPG3 - Duty cycle register		PDUT3	W
000095 _H	PPG3 - Duty cycle register			W
000096 _H	PPG3 - Control status register Low	PCNL3	PCN3	R/W
000097 _H	PPG3 - Control status register High	PCNH3		R/W
000098 _H	PPG7-PPG4 - General Control register 1 Low	GCN1L1	GCN11	R/W
000099 _H	PPG7-PPG4 - General Control register 1 High	GCN1H1		R/W
00009A _H	PPG7-PPG4 - General Control register 2 Low	GCN2L1	GCN21	R/W
00009B _H	PPG7-PPG4 - General Control register 2 High	GCN2H1		R/W
00009C _H	PPG4 - Timer register		PTMR4	R
00009D _H	PPG4 - Timer register			R
00009E _H	PPG4 - Period setting register		PCSR4	W
00009F _H	PPG4 - Period setting register			W
0000A0 _H	PPG4 - Duty cycle register		PDUT4	W

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000114 _H	DMA2 - I/O register address pointer low byte	IOAL2	IOA2	R/W
000115 _H	DMA2 - I/O register address pointer high byte	IOAH2		R/W
000116 _H	DMA2 - Data counter low byte	DCTL2	DCT2	R/W
000117 _H	DMA2 - Data counter high byte	DCTH2		R/W
000118 _H	DMA3 - Buffer address pointer low byte	BAPL3		R/W
000119 _H	DMA3 - Buffer address pointer middle byte	BAPM3		R/W
00011A _H	DMA3 - Buffer address pointer high byte	BAPH3		R/W
00011B _H	DMA3 - DMA control register	DMACS3		R/W
00011C _H	DMA3 - I/O register address pointer low byte	IOAL3	IOA3	R/W
00011D _H	DMA3 - I/O register address pointer high byte	IOAH3		R/W
00011E _H	DMA3 - Data counter low byte	DCTL3	DCT3	R/W
00011F _H	DMA3 - Data counter high byte	DCTH3		R/W
000120 _H	DMA4 - Buffer address pointer low byte	BAPL4		R/W
000121 _H	DMA4 - Buffer address pointer middle byte	BAPM4		R/W
000122 _H	DMA4 - Buffer address pointer high byte	BAPH4		R/W
000123 _H	DMA4 - DMA control register	DMACS4		R/W
000124 _H	DMA4 - I/O register address pointer low byte	IOAL4	IOA4	R/W
000125 _H	DMA4 - I/O register address pointer high byte	IOAH4		R/W
000126 _H	DMA4 - Data counter low byte	DCTL4	DCT4	R/W
000127 _H	DMA4 - Data counter high byte	DCTH4		R/W
000128 _H	DMA5 - Buffer address pointer low byte	BAPL5		R/W
000129 _H	DMA5 - Buffer address pointer middle byte	BAPM5		R/W
00012A _H	DMA5 - Buffer address pointer high byte	BAPH5		R/W
00012B _H	DMA5 - DMA control register	DMACS5		R/W
00012C _H	DMA5 - I/O register address pointer low byte	IOAL5	IOA5	R/W
00012D _H	DMA5 - I/O register address pointer high byte	IOAH5		R/W
00012E _H	DMA5 - Data counter low byte	DCTL5	DCT5	R/W
00012F _H	DMA5 - Data counter high byte	DCTH5		R/W
000130 _H -00017F _H	Reserved			-
000180 _H -00037F _H	CPU - General Purpose registers (RAM access)	GPR_RAM		R/W
000380 _H	DMA0 - Interrupt select	DISEL0		R/W
000381 _H	DMA1 - Interrupt select	DISEL1		R/W

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0004B3 _H -0004BB _H	Reserved			-
0004BC _H	I/O Port P00 - External Pin State Register	EPSR00		R
0004BD _H	I/O Port P01 - External Pin State Register	EPSR01		R
0004BE _H	I/O Port P02 - External Pin State Register	EPSR02		R
0004BF _H	I/O Port P03 - External Pin State Register	EPSR03		R
0004C0 _H	I/O Port P04 - External Pin State Register	EPSR04		R
0004C1 _H	I/O Port P05 - External Pin State Register	EPSR05		R
0004C2 _H	I/O Port P06 - External Pin State Register	EPSR06		R
0004C3 _H	I/O Port P07 - External Pin State Register	EPSR07		R
0004C4 _H	I/O Port P08 - External Pin State Register	EPSR08		R
0004C5 _H	I/O Port P09 - External Pin State Register	EPSR09		R
0004C6 _H	I/O Port P10 - External Pin State Register	EPSR10		R
0004C7 _H -0004CF _H	Reserved			-
0004D0 _H	ADC analog input enable register 0	ADER0		R/W
0004D1 _H	ADC analog input enable register 1	ADER1		R/W
0004D2 _H	ADC analog input enable register 2	ADER2		R/W
0004D3 _H	ADC analog input enable register 3	ADER3		R/W
0004D4 _H	ADC analog input enable register 4	ADER4		R/W
0004D5 _H	Reserved			-
0004D6 _H	Peripheral Resource Relocation Register 0	PRRR0		R/W
0004D7 _H	Peripheral Resource Relocation Register 1	PRRR1		R/W
0004D8 _H	Peripheral Resource Relocation Register 2	PRRR2		R/W
0004D9 _H	Peripheral Resource Relocation Register 3	PRRR3		R/W
0004DA _H	Peripheral Resource Relocation Register 4	PRRR4		R/W
0004DB _H	Peripheral Resource Relocation Register 5	PRRR5		R/W
0004DC _H	Peripheral Resource Relocation Register 6	PRRR6		R/W
0004DD _H	Peripheral Resource Relocation Register 7	PRRR7		R/W
0004DE _H	Peripheral Resource Relocation Register 8	PRRR8		R/W
0004DF _H	Peripheral Resource Relocation Register 9	PRRR9		R/W
0004E0 _H	RTC - Sub Second Register L	WTBRL0	WTBR0	R/W
0004E1 _H	RTC - Sub Second Register M	WTBRH0		R/W
0004E2 _H	RTC - Sub-Second Register H	WTBR1		R/W

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0004E3 _H	RTC - Second Register	WTSR		R/W
0004E4 _H	RTC - Minutes	WTMR		R/W
0004E5 _H	RTC - Hour	WTHR		R/W
0004E6 _H	RTC - Timer Control Extended Register	WTCER		R/W
0004E7 _H	RTC - Clock select register	WTCKSR		R/W
0004E8 _H	RTC - Timer Control Register Low	WTCRL	WTCR	R/W
0004E9 _H	RTC - Timer Control Register High	WTCRH		R/W
0004EA _H	CAL - Calibration unit Control register	CUCR		R/W
0004EB _H	Reserved			-
0004EC _H	CAL - Duration Timer Data Register Low	CUTDL	CUTD	R/W
0004ED _H	CAL - Duration Timer Data Register High	CUTDH		R/W
0004EE _H	CAL - Calibration Timer Register 2 Low	CUTR2L	CUTR2	R
0004EF _H	CAL - Calibration Timer Register 2 High	CUTR2H		R
0004F0 _H	CAL - Calibration Timer Register 1 Low	CUTR1L	CUTR1	R
0004F1 _H	CAL - Calibration Timer Register 1 High	CUTR1H		R
0004F2 _H -0004F9 _H	Reserved			-
0004FA _H	RLT - Timer input select (for Cascading)	TMISR		R/W
0004FB _H -00053D _H	Reserved			-
00053E _H	USART7 - Serial Mode Register	SMR7		R/W
00053F _H	USART7 - Serial Control Register	SCR7		R/W
000540 _H	USART7 - Serial TX Register	TDR7		W
000540 _H	USART7 - Serial RX Register	RDR7		R
000541 _H	USART7 - Serial Status Register	SSR7		R/W
000542 _H	USART7 - Ext. Control/Com. Register	ECCR7		R/W
000543 _H	USART7 - Ext. Status Com. Register	ESCR7		R/W
000544 _H	USART7 - Baud Rate Generator Register Low	BGRL7	BGR7	R/W
000545 _H	USART7 - Baud Rate Generator Register High	BGRH7		R/W
000546 _H	USART7 - Extended Serial Interrupt Register	ESIR7		R/W
000547 _H	Reserved			-
000548 _H	USART8 - Serial Mode Register	SMR8		R/W
000549 _H	USART8 - Serial Control Register	SCR8		R/W
00054A _H	USART8 - Serial TX Register	TDR8		W

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00054A _H	USART8 - Serial RX Register	RDR8		R
00054B _H	USART8 - Serial Status Register	SSR8		R/W
00054C _H	USART8 - Ext. Control/Com. Register	ECCR8		R/W
00054D _H	USART8 - Ext. Status Com. Register	ESCR8		R/W
00054E _H	USART8 - Baud Rate Generator Register Low	BGRL8	BGR8	R/W
00054F _H	USART8 - Baud Rate Generator Register High	BGRH8		R/W
000550 _H	USART8 - Extended Serial Interrupt Register	ESIR8		R/W
000551 _H	Reserved			-
000552 _H	USART9 - Serial Mode Register	SMR9		R/W
000553 _H	USART9 - Serial Control Register	SCR9		R/W
000554 _H	USART9 - Serial TX Register	TDR9		W
000554 _H	USART9 - Serial RX Register	RDR9		R
000555 _H	USART9 - Serial Status Register	SSR9		R/W
000556 _H	USART9 - Ext. Control/Com. Register	ECCR9		R/W
000557 _H	USART9 - Ext. Status Com. Register	ESCR9		R/W
000558 _H	USART9 - Baud Rate Generator Register Low	BGRL9	BGR9	R/W
000559 _H	USART9 - Baud Rate Generator Register High	BGRH9		R/W
00055A _H	USART9 - Extended Serial Interrupt Register	ESIR9		R/W
00055B _H -00055F _H	Reserved			-
000560 _H	ALARM0 - Control Status Register	ACSR0		R/W
000561 _H	ALARM0 - Extended Control Status Register	AECSR0		R/W
000562 _H	ALARM1 - Control Status Register	ACSR1		R/W
000563 _H	ALARM1 - Extended Control Status Register	AECSR1		R/W
000564 _H	PPG6 - Timer register		PTMR6	R
000565 _H	PPG6 - Timer register			R
000566 _H	PPG6 - Period setting register		PCSR6	W
000567 _H	PPG6 - Period setting register			W
000568 _H	PPG6 - Duty cycle register		PDUT6	W
000569 _H	PPG6 - Duty cycle register			W
00056A _H	PPG6 - Control status register Low	PCNL6	PCN6	R/W
00056B _H	PPG6 - Control status register High	PCNH6		R/W
00056C _H	PPG7 - Timer register		PTMR7	R

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000801 _H	CAN1 - Control register High (reserved)	CTRLRH1		R
000802 _H	CAN1 - Status register Low	STATRL1	STATR1	R/W
000803 _H	CAN1 - Status register High (reserved)	STATRH1		R
000804 _H	CAN1 - Error Counter Low (Transmit)	ERRCNTL1	ERRCNT1	R
000805 _H	CAN1 - Error Counter High (Receive)	ERRCNTH1		R
000806 _H	CAN1 - Bit Timing Register Low	BTRL1	BTR1	R/W
000807 _H	CAN1 - Bit Timing Register High	BTRH1		R/W
000808 _H	CAN1 - Interrupt Register Low	INTRL1	INTR1	R
000809 _H	CAN1 - Interrupt Register High	INTRH1		R
00080A _H	CAN1 - Test Register Low	TESTRL1	TESTR1	R/W
00080B _H	CAN1 - Test Register High (reserved)	TESTRH1		R
00080C _H	CAN1 - BRP Extension register Low	BRPERL1	BRPER1	R/W
00080D _H	CAN1 - BRP Extension register High (reserved)	BRPERH1		R
00080E _H -00080F _H	Reserved			-
000810 _H	CAN1 - IF1 Command request register Low	IF1CREQL1	IF1CREQ1	R/W
000811 _H	CAN1 - IF1 Command request register High	IF1CREQH1		R/W
000812 _H	CAN1 - IF1 Command Mask register Low	IF1CMSKL1	IF1CMSK1	R/W
000813 _H	CAN1 - IF1 Command Mask register High (reserved)	IF1CMSKH1		R
000814 _H	CAN1 - IF1 Mask 1 Register Low	IF1MSK1L1	IF1MSK11	R/W
000815 _H	CAN1 - IF1 Mask 1 Register High	IF1MSK1H1		R/W
000816 _H	CAN1 - IF1 Mask 2 Register Low	IF1MSK2L1	IF1MSK21	R/W
000817 _H	CAN1 - IF1 Mask 2 Register High	IF1MSK2H1		R/W
000818 _H	CAN1 - IF1 Arbitration 1 Register Low	IF1ARB1L1	IF1ARB11	R/W
000819 _H	CAN1 - IF1 Arbitration 1 Register High	IF1ARB1H1		R/W
00081A _H	CAN1 - IF1 Arbitration 2 Register Low	IF1ARB2L1	IF1ARB21	R/W
00081B _H	CAN1 - IF1 Arbitration 2 Register High	IF1ARB2H1		R/W
00081C _H	CAN1 - IF1 Message Control Register Low	IF1MCTRL1	IF1MCTR1	R/W
00081D _H	CAN1 - IF1 Message Control Register High	IF1MCTRH1		R/W
00081E _H	CAN1 - IF1 Data A1 Low	IF1DTA1L1	IF1DTA11	R/W
00081F _H	CAN1 - IF1 Data A1 High	IF1DTA1H1		R/W
000820 _H	CAN1 - IF1 Data A2 Low	IF1DTA2L1	IF1DTA21	R/W
000821 _H	CAN1 - IF1 Data A2 High	IF1DTA2H1		R/W

13. Handling Devices

Special care is required for the following when handling the device:

- Latch-up prevention
- Unused pins handling
- External clock usage
- Unused sub clock signal
- Notes on PLL clock mode operation
- Power supply pins (V_{CC}/V_{SS})
- Crystal oscillator circuit
- Turn on sequence of power supply to A/D converter and analog inputs
- Pin handling when not using the A/D converter
- Notes on energization
- Stabilization of power supply voltage
- Serial communication
- Handling of Data Flash

13.1 Latch-up prevention

CMOS IC chips may suffer latch-up under the following conditions:

- A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V_{CC} pins and V_{SS} pins.
- The AV_{CC} power supply is applied before the V_{CC} voltage.

Latch-up may increase the power supply current dramatically, causing thermal damages to the device.

For the same reason, extra care is required to not let the analog power-supply voltage (AV_{CC} , $AVRH$) exceed the digital power-supply voltage.

13.2 Unused pins handling

Unused input pins can be left open when the input is disabled (corresponding bit of Port Input Enable register $PIER = 0$).

Leaving unused input pins open when the input is enabled may result in misbehavior and possible permanent damage of the device. They must therefore be pulled up or pulled down through resistors. To prevent latch-up, those resistors should be more than 2 k Ω .

Unused bidirectional pins can be set either to the output state and be then left open, or to the input state with either input disabled or external pull-up/pull-down resistor as described above.

13.3 External clock usage

The permitted frequency range of an external clock depends on the oscillator type and configuration. See [AC Characteristics](#) for detailed modes and frequency limits. Single and opposite phase external clocks must be connected as follows:

($T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = 0\text{V}$)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Run modes ^[1]	I_{CCRCH}	RC Run mode with $CLKS1/2 = CLKB = CLKP1/2 = 2\text{MHz}$ (CLKMC, CLKPLL and CLKSC stopped)	+25°C	2.9	4	mA	Flash devices at 1 Flash wait state
			+125°C	3.5	6.5		
			+25°C	1.7	2.7	mA	MB96345/346 at 1 ROM wait state
			+125°C	2.3	4.7		
	I_{CCRCL}	RC Run mode with $CLKS1/2 = CLKB = CLKP1/2 = 100\text{kHz}$, SMCR:LPMS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)	+25°C	0.4	0.6	mA	MB96F346/F347/F348 at 1 Flash wait state
			+125°C	0.9	3.5		
			+25°C	0.18	0.3	mA	MB96F345 at 1 Flash wait state
			+125°C	0.68	3.3		
			+25°C	0.4	0.6	mA	MB96345/346 at 1 ROM wait state
			+125°C	0.9	2.4		
		RC Run mode with $CLKS1/2 = CLKB = CLKP1/2 = 100\text{kHz}$, SMCR:LPMS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode, no Flash programming/erasing allowed)	+25°C	0.15	0.25	mA	Flash devices at 1 Flash wait state
			+125°C	0.65	3.2		
			+25°C	0.15	0.25	mA	MB96345/346 at 1 ROM wait state
			+125°C	0.65	2.1		
	I_{CCSUB}	Sub Run mode with $CLKS1/2 = CLKB = CLKP1/2 = 32\text{kHz}$ (CLKMC, CLKPLL and CLKRC stopped, no Flash programming/erasing allowed)	+25°C	0.1	0.2	mA	Flash devices at 1 Flash wait state
			+125°C	0.6	3		
			+25°C	0.1	0.2	mA	MB96345/346 at 1 ROM wait state
			+125°C	0.6	2		

($T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = 0\text{V}$)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Sleep modes ^[1]	I_{CCSPLL}	PLL Sleep mode with $CLKS1/2 = 48\text{MHz}$, $CLKP1/2 = 24\text{MHz}$ (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	9	10.5	mA	Flash devices
			+125°C	9.7	13		
			+25°C	8	9.5	mA	MB96345/346
			+125°C	8.7	11.5		
		PLL Sleep mode with $CLKS1/2 =$ $CLKP1 = 56\text{MHz}$, $CLKP2 = 28\text{MHz}$ (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	14	15.5	mA	MB96F346/F347/F348
			+125°C	14.8	18		
			+25°C	13.5	15	mA	MB96345/346
			+125°C	14.3	17		
		PLL Sleep mode with $CLKS1/2 = 72\text{MHz}$, $CLKP1 = 36\text{MHz}$, $CLKP2 = 18\text{MHz}$ (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	10.5	12	mA	MB96F346/F347/F348Y/R/Ayy
			+125°C	11.3	14.5		
		PLL Sleep mode with $CLKS1/2 = 80\text{MHz}$, $CLKP1 = 40\text{MHz}$, $CLKP2 = 20\text{MHz}$ (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	TBD	TBD	mA	MB96F345
			+125°C	TBD	TBD		
		PLL Sleep mode with $CLKS1/2 = 96\text{MHz}$, $CLKP1 = 48\text{MHz}$, $CLKP2 = 24\text{MHz}$ (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	15	16.5	mA	MB96F348T/H/CyB/C
			+125°C	15.8	19		
			+25°C	14	15.5	mA	MB96345/346
			+125°C	14.8	17.5		
	$I_{CCSMAIN}$	Main Sleep mode with $CLKS1/2 =$ $CLKP1/2 = 4\text{MHz}$ (CLKPLL, CLKSC and CLKRC stopped)	+25°C	1.5	1.8	mA	Flash devices
			+125°C	2	4.5		
			+25°C	1.5	1.8	mA	MB96345/346
			+125°C	2	3.8		

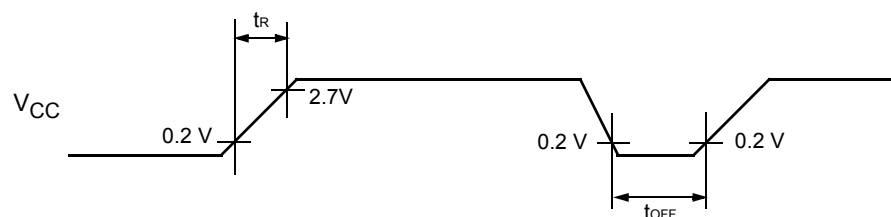
($T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = 0\text{V}$)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Timer modes ^[1]	I_{CCTRCL}	RC Timer mode with CLKRC = 100kHz, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)	+25°C	0.3	0.45	mA	MB96F346/F347/F348
			+125°C	0.8	3.2		
			+25°C	0.08	0.15	mA	MB96F345
			+125°C	0.58	2.95		
			+25°C	0.3	0.45	mA	MB96345/346
			+125°C	0.8	2.2		
		RC Timer mode with CLKRC = 100kHz, SMCR:LPMSS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode)	+25°C	0.05	0.1	mA	Flash devices
			+125°C	0.55	2.85		
			+25°C	0.05	0.1	mA	MB96345/346
			+125°C	0.55	1.85		
	I_{CCTSUB}	Sub Timer mode with CLKSC = 32kHz (CLKMC, CLKPLL and CLKRC stopped)	+25°C	0.03	0.1	mA	Flash devices
			+125°C	0.53	2.85		
			+25°C	0.03	0.1	mA	MB96345/346
			+125°C	0.53	1.85		
Power supply current in Stop Mode	I_{CCH}	VR CR:LPMB[2:0] = 110 _B (Core voltage at 1.8V)	+25°C	0.02	0.08	mA	Flash devices
			+125°C	0.52	2.8		
			+25°C	0.02	0.08	mA	MB96345/346
			+125°C	0.52	1.8		
		VR CR:LPMB[2:0] = 000 _B (Core voltage at 1.2V)	+25°C	0.015	0.06	mA	Flash devices
			+125°C	0.4	2.3		
			+25°C	0.015	0.06	mA	MB96345/346
			+125°C	0.4	1.4		
Power supply current for active Low Voltage detector	I_{CCLVD}	Low voltage detector enabled (RCR:LVDE = 1)	-	5	10	μA	MB96F345 Must be added to all current above
			+25°C	90	140	μA	Other devices Must be added to all current above
			+125°C	100	150		

14.4.4 Power On Reset timing

($T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = 0\text{V}$)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Power on rise time	t_R	V_{CC}	0.05	-	30	ms	
Power off time	t_{OFF}	V_{CC}	1	-	-	ms	



If the power supply is changed too rapidly, a power-on reset may occur.
 We recommend a smooth startup by restraining voltages when changing the power supply voltage during operation, as shown in the figure below.



14.4.7 Basic Timing

($T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $I_{O_{drive}} = 5\text{mA}$, $C_L = 50\text{pF}$)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
ECLK	t_{CYC}	ECLK	-	25	-	ns	
	t_{CHCL}			$t_{CYC}/2-5$	$t_{CYC}/2+5$		
	t_{CLCH}			$t_{CYC}/2-5$	$t_{CYC}/2+5$		
ECLK → UBX/ LBX / CSn time	t_{CHCBH}	CSn, UBX, LBX, ECLK	-	-20	20	ns	
	t_{CHCBL}			-20	20		
	t_{CLCBH}			-20	20		
	t_{CLCBL}			-20	20		
ECLK → ALE time	t_{CHLH}	ALE, ECLK	-	-10	10	ns	
	t_{CHLL}			-10	10		
	t_{CLLH}			-10	10		
	t_{CLLL}			-10	10		
ECLK → address valid time	t_{CHAV}	A[23:16], ECLK	-	-15	15	ns	
	t_{CLAV}			-15	15		
	t_{CLADV}	AD[15:0], ECLK	-	-15	15	ns	
	t_{CHADV}			-15	15		
ECLK → RDX /WRX time	t_{CHRWL}	RDX, WRX, WRLX, WRHX, ECLK	-	-10	10	ns	
	t_{CHRWL}			-10	10		
	t_{CLRWH}			-10	10		
	t_{CLRWL}			-10	10		

14.4.12 USART timing

WARNING: The values given below are for an I/O driving strength $IO_{drive} = 5mA$. If IO_{drive} is 2mA, all the maximum output timing described in the different tables must then be increased by 10ns.

($T_A = -40^{\circ}C$ to $125^{\circ}C$, $V_{CC} = 3.0V$ to $5.5V$, $V_{SS} = AV_{SS} = 0V$, $IO_{drive} = 5mA$, $C_L = 50pF$)

Parameter	Symbol	Pin	Condition	$V_{CC} = AV_{CC} = 4.5V$ to $5.5V$		$V_{CC} = AV_{CC} = 3.0V$ to $4.5V$		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYCI}	SCKn	Internal Shift Clock Mode	$4 t_{CLKP1}$	-	$4 t_{CLKP1}$	-	ns
SCK $\downarrow \rightarrow$ SOT delay time	t_{SLOVI}	SCKn, SOTn		-20	+20	-30	+30	ns
SOT $\rightarrow$ SCK $\uparrow$ delay time	t_{OVSHI}	SCKn, SOTn		$N * t_{CLKP1} - 20$ [1]	-	$N * t_{CLKP1} - 30$ [1]	-	ns
Valid SIN $\rightarrow$ SCK $\uparrow$	t_{IVSHI}	SCKn, SINn		$t_{CLKP1} + 45$	-	$t_{CLKP1} + 55$	-	ns
SCK $\uparrow \rightarrow$ Valid SIN hold time	t_{SHIXI}	SCKn, SINn		0	-	0	-	ns
Serial clock "L" pulse width	t_{LSHE}	SCKn	External Shift Clock Mode	$t_{CLKP1} + 10$	-	$t_{CLKP1} + 10$	-	ns
Serial clock "H" pulse width	t_{HSLE}	SCKn		$t_{CLKP1} + 10$	-	$t_{CLKP1} + 10$	-	ns
SCK $\downarrow \rightarrow$ SOT delay time	t_{SLOVE}	SCKn, SOTn		-	$2 t_{CLKP1} + 45$	-	$2 t_{CLKP1} + 55$	ns
Valid SIN $\rightarrow$ SCK $\uparrow$	t_{IVSHE}	SCKn, SINn		$t_{CLKP1}/2 + 10$	-	$t_{CLKP1}/2 + 10$	-	ns
SCK $\uparrow \rightarrow$ Valid SIN hold time	t_{SHIXE}	SCKn, SINn		$t_{CLKP1} + 10$	-	$t_{CLKP1} + 10$	-	ns
SCK fall time	t_{FE}	SCKn		-	20	-	20	ns
SCK rise time	t_{RE}	SCKn		-	20	-	20	ns

Notes:

- AC characteristic in CLK synchronized mode.
- C_L is the load capacity value of pins when testing.
- Depending on the used machine clock frequency, the maximum possible baud rate can be limited by some parameters. These parameters are shown in "MB96300 Super series HARDWARE MANUAL".
- t_{CLKP1} is the cycle time of the peripheral clock 1 (CLKP1), Unit : ns

[1]: Parameter N depends on t_{SCYCI} and can be calculated as follows:

- if $t_{SCYCI} = 2 * k * t_{CLKP1}$, then $N = k$, where k is an integer > 2
- if $t_{SCYCI} = (2 * k + 1) * t_{CLKP1}$, then $N = k + 1$, where k is an integer > 1

Examples:

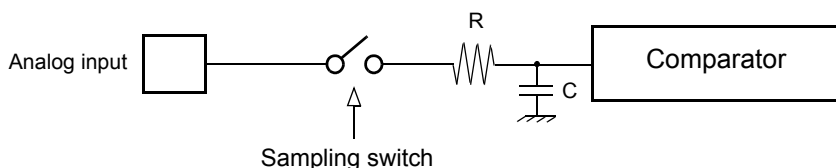
t_{SCYCI}	N
$4 * t_{CLKP1}$	2
$5 * t_{CLKP1}$	3
$7 * t_{CLKP1}$	4
...	...

14.5.2 Notes on A/D Converter Section

■ About the external impedance of the analog input and the sampling time of the A/D converter (with sample and hold circuit):

If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision.

Analog input circuit model:



Reference value:

C = 8.5 pF (Max)

To satisfy the A/D conversion precision standard, the relationship between the external impedance and minimum sampling time must be considered and then either the resistor value and operating frequency must be adjusted or the external impedance must be decreased so that the sampling time (T_{samp}) is longer than the minimum value. Usually, this value is set to 7τ , where $\tau = RC$. If the external input resistance (R_{ext}) connected to the analog input is included, the sampling time is expressed as follows:

$$T_{\text{samp}} [\text{min}] = 7 \times (R_{\text{ext}} + 2.6\text{k}\Omega) \times C \text{ for } 4.5 \leq AV_{\text{CC}} \leq 5.5$$

$$T_{\text{samp}} [\text{min}] = 7 \times (R_{\text{ext}} + 12.1\text{k}\Omega) \times C \text{ for } 3.0 \leq AV_{\text{CC}} \leq 4.5$$

If the sampling time cannot be sufficient, connect a capacitor of about 0.1 μF to the analog input pin.

■ About the error

The accuracy gets worse as $|AV_{\text{RH}} - AV_{\text{RL}}|$ becomes smaller.

14.6 Alarm Comparator

($T_A = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$, $V_{CC} = AV_{CC} = 3.0\text{V} - 5.5\text{V}$, $V_{SS} = AV_{SS} = 0\text{V}$)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Power supply current	I_{A5ALMF}	AV_{CC}	-	25	45	μA	Alarm comparator enabled in fast mode (one channel)
	I_{A5ALMS}		-	7	13	μA	Alarm comparator enabled in slow mode (one channel)
	I_{A5ALMH}		-	-	5	μA	Alarm comparator disabled
ALARM pin input current	I_{ALIN}	ALARM0, ALARM1	-1	-	+1	μA	$T_A = 25\text{ }^{\circ}\text{C}$
			-3	-	+3	μA	$T_A = 125\text{ }^{\circ}\text{C}$
ALARM pin input voltage range	V_{ALIN}		0	-	AV_{CC}	V	
External low threshold high->low transition	$V_{EVTL(H\rightarrow L)}$		$0.36 * AV_{CC} - 0.25$	$0.36 * AV_{CC} - 0.1$	-	V	INTREF = 0
External low threshold low->high transition	$V_{EVTL(L\rightarrow H)}$		-	$0.36 * AV_{CC} + 0.1$	$0.36 * AV_{CC} + 0.25$	V	
External high threshold high->low transition	$V_{EVTH(H\rightarrow L)}$		$0.78 * AV_{CC} - 0.25$	$0.78 * AV_{CC} - 0.1$	-	V	
External high threshold low->high transition	$V_{EVTH(L\rightarrow H)}$			$0.78 * AV_{CC} + 0.1$	$0.78 * AV_{CC} + 0.25$	V	
Internal low threshold high->low transition	$V_{IVTL(H\rightarrow L)}$		0.9	1.1	-	V	INTREF = 1
Internal low threshold low->high transition	$V_{IVTL(L\rightarrow H)}$		-	1.3	1.55	V	
Internal high threshold high->low transition	$V_{IVTH(H\rightarrow L)}$		2.2	2.4	-	V	
Internal high threshold low->high transition	$V_{IVTH(L\rightarrow H)}$		-	2.6	2.85	V	
Switching hysteresis	V_{HYS}		50	-	300	mV	
Comparison time	t_{COMPF}		-	0.1	1	μs	CMD = 1 (fast)
	t_{COMPS}		-	1	10	μs	CMD = 0 (slow)
Power-up stabilization time after enabling alarm comparator	t_{PD}		-	1	5	ms	Threshold levels specified above are not guaranteed within this time
Slow/Fast mode transition time	t_{CMD}		-	100	500	μs	