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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	F ² MC-16FX
Core Size	16-Bit
Speed	56MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, LVR, POR, PWM, WDT
Number of I/O	82
Program Memory Size	544KB (544K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-PQFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f348rsbpqc-gs-jaere2

2. Block Diagram

Figure 1. Block diagram of MB96(F)34x

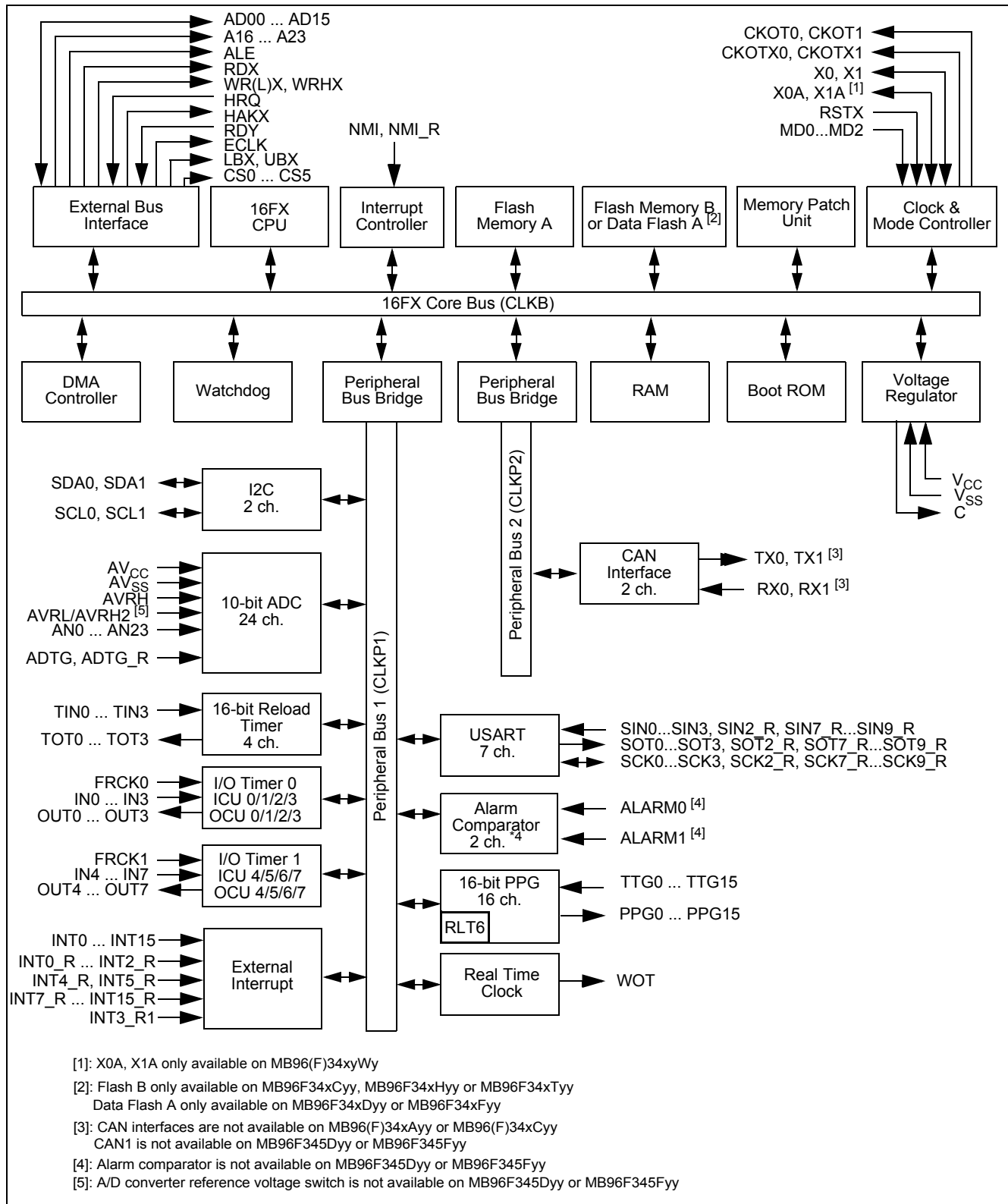


Table 1: Pin Function description

Pin name	Feature	Description
RDY	External bus	External bus interface external wait state request input
RSTX	Core	Reset input
RXn	CAN	CAN interface n RX input
SCKn	USART	USART n serial clock input/output
SCKn_R	USART	Relocated USART n serial clock input/output
SCLn	I ² C	I ² C interface n clock I/O input/output
SDAn	I ² C	I ² C interface n serial data I/O input/output
SINn	USART	USART n serial data input
SINn_R	USART	Relocated USART n serial data input
SOTn	USART	USART n serial data output
SOTn_R	USART	Relocated USART n serial data output
TINn	Reload Timer	Reload Timer n event input
TOTn	Reload Timer	Reload Timer n output
TTGn	PPG	Programmable Pulse Generator n trigger input
TXn	CAN	CAN interface n TX output
UBX	External bus	External Bus Interface Upper Byte select strobe output
V _{CC}	Supply	Power supply
V _{SS}	Supply	Power supply
WOT	RTC	Real Timer clock output
WRHX	External bus	External bus High byte write strobe output
WRLX/WRX	External bus	External bus Low byte / Word write strobe output
X0	Clock	Oscillator input
X0A	Clock	Subclock Oscillator input (only for devices with suffix "W")
X1	Clock	Oscillator output
X1A	Clock	Subclock Oscillator output (only for devices with suffix "W")

■ RAM Start/End and External Bus End Addresses

Devices	Bank 0 RAM size	Bank 1 RAM size	External Bus end address	RAMSTART0	RAMSTART1	RAMEND1
MB96(F)345	8KByte	-	00:21FF _H	00:6240 _H	-	-
MB96(F)346,MB96F347	16KByte	-	00:21FF _H	00:4240 _H	-	-
MB96F348	24KByte	-	00:21FF _H	00:2240 _H	-	-

11. I/O Map

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000000 _H	I/O Port P00 - Port Data Register	PDR00		R/W
000001 _H	I/O Port P01 - Port Data Register	PDR01		R/W
000002 _H	I/O Port P02 - Port Data Register	PDR02		R/W
000003 _H	I/O Port P03 - Port Data Register	PDR03		R/W
000004 _H	I/O Port P04 - Port Data Register	PDR04		R/W
000005 _H	I/O Port P05 - Port Data Register	PDR05		R/W
000006 _H	I/O Port P06 - Port Data Register	PDR06		R/W
000007 _H	I/O Port P07 - Port Data Register	PDR07		R/W
000008 _H	I/O Port P08 - Port Data Register	PDR08		R/W
000009 _H	I/O Port P09 - Port Data Register	PDR09		R/W
00000A _H	I/O Port P10 - Port Data Register	PDR10		R/W
00000B _H -000017 _H	Reserved			-
000018 _H	ADC0 - Control Status register Low	ADCSL	ADCS	R/W
000019 _H	ADC0 - Control Status register High	ADCSH		R/W
00001A _H	ADC0 - Data Register Low	ADCRL	ADCR	R
00001B _H	ADC0 - Data Register High	ADCRH		R
00001C _H	ADC0 - Setting Register		ADSR	R/W
00001D _H	ADC0 - Setting Register			R/W
00001E _H	ADC0 - Extended Configuration Register	ADECR		R/W
00001F _H	Reserved			-
000020 _H	FRT0 - Data register of free-running timer		TCDT0	R/W
000021 _H	FRT0 - Data register of free-running timer			R/W
000022 _H	FRT0 - Control status register of free-running timer Low	TCCSL0	TCCS0	R/W
000023 _H	FRT0 - Control status register of free-running timer High	TCCSH0		R/W
000024 _H	FRT1 - Data register of free-running timer		TCDT1	R/W
000025 _H	FRT1 - Data register of free-running timer			R/W
000026 _H	FRT1 - Control status register of free-running timer Low	TCCSL1	TCCS1	R/W
000027 _H	FRT1 - Control status register of free-running timer High	TCCSH1		R/W
000028 _H	OCU0 - Output Compare Control Status	OCS0		R/W
000029 _H	OCU1 - Output Compare Control Status	OCS1		R/W
00002A _H	OCU0 - Compare Register		OCCP0	R/W

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0000A1 _H	PPG4 - Duty cycle register			W
0000A2 _H	PPG4 - Control status register Low	PCNL4	PCN4	R/W
0000A3 _H	PPG4 - Control status register High	PCNH4		R/W
0000A4 _H	PPG5 - Timer register		PTMR5	R
0000A5 _H	PPG5 - Timer register			R
0000A6 _H	PPG5 - Period setting register		PCSR5	W
0000A7 _H	PPG5 - Period setting register			W
0000A8 _H	PPG5 - Duty cycle register		PDUT5	W
0000A9 _H	PPG5 - Duty cycle register			W
0000AA _H	PPG5 - Control status register Low	PCNL5	PCN5	R/W
0000AB _H	PPG5 - Control status register High	PCNH5		R/W
0000AC _H	I2C0 - Bus Status Register	IBSR0		R
0000AD _H	I2C0 - Bus Control Register	IBCR0		R/W
0000AE _H	I2C0 - Ten bit Slave address Register Low	ITBAL0	ITBA0	R/W
0000AF _H	I2C0 - Ten bit Slave address Register High	ITBAH0		R/W
0000B0 _H	I2C0 - Ten bit Address mask Register Low	ITMKL0	ITMK0	R/W
0000B1 _H	I2C0 - Ten bit Address mask Register High	ITMKH0		R/W
0000B2 _H	I2C0 - Seven bit Slave address Register	ISBA0		R/W
0000B3 _H	I2C0 - Seven bit Address mask Register	ISMK0		R/W
0000B4 _H	I2C0 - Data Register	IDAR0		R/W
0000B5 _H	I2C0 - Clock Control Register	ICCR0		R/W
0000B6 _H	I2C1 - Bus Status Register	IBSR1		R
0000B7 _H	I2C1 - Bus Control Register	IBCR1		R/W
0000B8 _H	I2C1 - Ten bit Slave address Register Low	ITBAL1	ITBA1	R/W
0000B9 _H	I2C1 - Ten bit Slave address Register High	ITBAH1		R/W
0000BA _H	I2C1 - Ten bit Address mask Register Low	ITMKL1	ITMK1	R/W
0000BB _H	I2C1 - Ten bit Address mask Register High	ITMKH1		R/W
0000BC _H	I2C1 - Seven bit Slave address Register	ISBA1		R/W
0000BD _H	I2C1 - Seven bit Address mask Register	ISMK1		R/W
0000BE _H	I2C1 - Data Register	IDAR1		R/W
0000BF _H	I2C1 - Clock Control Register	ICCR1		R/W
0000C0 _H	USART0 - Serial Mode Register	SMR0		R/W

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0003D9 _H	Memory Patch function - Patch data 4 High	PFDH4		R/W
0003DA _H	Memory Patch function - Patch data 5 Low	PFDL5	PFD5	R/W
0003DB _H	Memory Patch function - Patch data 5 High	PFDH5		R/W
0003DC _H	Memory Patch function - Patch data 6 Low	PFDL6	PFD6	R/W
0003DD _H	Memory Patch function - Patch data 6 High	PFDH6		R/W
0003DE _H	Memory Patch function - Patch data 7 Low	PFDL7	PFD7	R/W
0003DF _H	Memory Patch function - Patch data 7 High	PFDH7		R/W
0003E0 _H	Data Flash Control and Status register A	DFCSA		R/W
0003E1 _H	Data Flash Write command sequencer Control register A	DFWCA		R/W
0003E2 _H	Data Flash Write command sequencer Status register A	DFWSA		R/W
0003E3 _H -0003F0 _H	Reserved			-
0003F1 _H	Memory Control Status Register A	MCSRA		R/W
0003F2 _H	Memory Timing Configuration Register A Low	MTCRAL	MTCRA	R/W
0003F3 _H	Memory Timing Configuration Register A High	MTCRAH		R/W
0003F4 _H	Reserved			-
0003F5 _H	Memory Control Status Register B	MCSR B		R/W
0003F6 _H	Memory Timing Configuration Register B Low	MTCRBL	MTCRB	R/W
0003F7 _H	Memory Timing Configuration Register B High	MTCRBH		R/W
0003F8 _H	Flash Memory Write Control register 0	FMWC0		R/W
0003F9 _H	Flash Memory Write Control register 1	FMWC1		R/W
0003FA _H	Flash Memory Write Control register 2	FMWC2		R/W
0003FB _H	Flash Memory Write Control register 3	FMWC3		R/W
0003FC _H	Flash Memory Write Control register 4	FMWC4		R/W
0003FD _H	Flash Memory Write Control register 5	FMWC5		R/W
0003FE _H -0003FF _H	Reserved			-
000400 _H	Standby Mode control register	SMCR		R/W
000401 _H	Clock select register	CKSR		R/W
000402 _H	Clock Stabilization select register	CKSSR		R/W
000403 _H	Clock monitor register	CKMR		R
000404 _H	Clock Frequency control register Low	CKFCRL	CKFCR	R/W
000405 _H	Clock Frequency control register High	CKFCRH		R/W
000406 _H	PLL Control register Low	PLLCRL	PLLCR	R/W

Table 4: I/O map MB96(F)34x

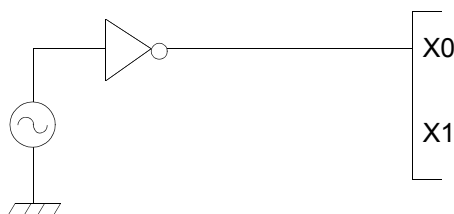
Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00058D _H	PPG10 - Duty cycle register			W
00058E _H	PPG10 - Control status register Low	PCNL10	PCN10	R/W
00058F _H	PPG10 - Control status register High	PCNH10		R/W
000590 _H	PPG11 - Timer register		PTMR11	R
000591 _H	PPG11 - Timer register			R
000592 _H	PPG11 - Period setting register		PCSR11	W
000593 _H	PPG11 - Period setting register			W
000594 _H	PPG11 - Duty cycle register		PDUT11	W
000595 _H	PPG11 - Duty cycle register			W
000596 _H	PPG11 - Control status register Low	PCNL11	PCN11	R/W
000597 _H	PPG11 - Control status register High	PCNH11		R/W
000598 _H	PPG15-PPG12 - General Control register 1 Low	GCN1L3	GCN13	R/W
000599 _H	PPG15-PPG12 - General Control register 1 High	GCN1H3		R/W
00059A _H	PPG15-PPG12 - General Control register 2 Low	GCN2L3	GCN23	R/W
00059B _H	PPG15-PPG12 - General Control register 2 High	GCN2H3		R/W
00059C _H	PPG12 - Timer register		PTMR12	R
00059D _H	PPG12 - Timer register			R
00059E _H	PPG12 - Period setting register		PCSR12	W
00059F _H	PPG12 - Period setting register			W
0005A0 _H	PPG12 - Duty cycle register		PDUT12	W
0005A1 _H	PPG12 - Duty cycle register			W
0005A2 _H	PPG12 - Control status register Low	PCNL12	PCN12	R/W
0005A3 _H	PPG12 - Control status register High	PCNH12		R/W
0005A4 _H	PPG13 - Timer register		PTMR13	R
0005A5 _H	PPG13 - Timer register			R
0005A6 _H	PPG13 - Period setting register		PCSR13	W
0005A7 _H	PPG13 - Period setting register			W
0005A8 _H	PPG13 - Duty cycle register		PDUT13	W
0005A9 _H	PPG13 - Duty cycle register			W
0005AA _H	PPG13 - Control status register Low	PCNL13	PCN13	R/W
0005AB _H	PPG13 - Control status register High	PCNH13		R/W
0005AC _H	PPG14 - Timer register		PTMR14	R

Table 5: Interrupt vector table MB96(F)34x

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
30	384 _H	EXTINT13	Yes	30	External Interrupt 13
31	380 _H	EXTINT14	Yes	31	External Interrupt 14
32	37C _H	EXTINT15	Yes	32	External Interrupt 15
33	378 _H	CAN0	No	33	CAN Controller 0 (except MB96(F)34xAyy or MB96(F)34xCyy)
34	374 _H	CAN1	No	34	CAN Controller 1 (except MB96(F)34xAyy, MB96(F)34xCyy, MB96F345Dyy or MB96F345Fyy)
35	370 _H	PPG0	Yes	35	Programmable Pulse Generator 0
36	36C _H	PPG1	Yes	36	Programmable Pulse Generator 1
37	368 _H	PPG2	Yes	37	Programmable Pulse Generator 2
38	364 _H	PPG3	Yes	38	Programmable Pulse Generator 3
39	360 _H	PPG4	Yes	39	Programmable Pulse Generator 4
40	35C _H	PPG5	Yes	40	Programmable Pulse Generator 5
41	358 _H	PPG6	Yes	41	Programmable Pulse Generator 6
42	354 _H	PPG7	Yes	42	Programmable Pulse Generator 7
43	350 _H	PPG8	Yes	43	Programmable Pulse Generator 8
44	34C _H	PPG9	Yes	44	Programmable Pulse Generator 9
45	348 _H	PPG10	Yes	45	Programmable Pulse Generator 10
46	344 _H	PPG11	Yes	46	Programmable Pulse Generator 11
47	340 _H	PPG12	Yes	47	Programmable Pulse Generator 12
48	33C _H	PPG13	Yes	48	Programmable Pulse Generator 13
49	338 _H	PPG14	Yes	49	Programmable Pulse Generator 14
50	334 _H	PPG15	Yes	50	Programmable Pulse Generator 15
51	330 _H	RLT0	Yes	51	Reload Timer 0
52	32C _H	RLT1	Yes	52	Reload Timer 1
53	328 _H	RLT2	Yes	53	Reload Timer 2
54	324 _H	RLT3	Yes	54	Reload Timer 3
55	320 _H	PPGRLT	Yes	55	Reload Timer 6 - dedicated for PPG
56	31C _H	ICU0	Yes	56	Input Capture Unit 0
57	318 _H	ICU1	Yes	57	Input Capture Unit 1
58	314 _H	ICU2	Yes	58	Input Capture Unit 2
59	310 _H	ICU3	Yes	59	Input Capture Unit 3

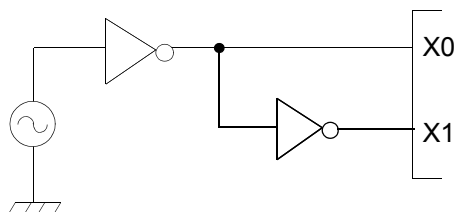
13.3.1 Single phase external clock

- When using a single phase external clock, X0 pin must be driven and X1 pin left open.



13.3.2 Opposite phase external clock

- When using an opposite phase external clock, X1 (X1A) must be supplied with a clock signal which has the opposite phase to the X0 (X0A) pins.



13.4 Unused sub clock signal

If the pins X0A and X1A are not connected to an oscillator, a pull-down resistor must be connected on the X0A pin and the X1A pin must be left open.

13.5 Notes on PLL clock mode operation

If the PLL clock mode is selected and no external oscillator is operating or no external clock is supplied, the microcontroller attempts to work with the free oscillating PLL. Performance of this operation, however, cannot be guaranteed.

13.6 Power supply pins (V_{CC}/V_{SS})

It is required that all V_{CC} -level as well as all V_{SS} -level power supply pins are at the same potential. If there is more than one V_{CC} or V_{SS} level, the device may operate incorrectly or be damaged even within the guaranteed operating range.

V_{CC} and V_{SS} must be connected to the device from the power supply with lowest possible impedance.

As a measure against power supply noise, it is required to connect a bypass capacitor of about 0.1 μF between V_{CC} and V_{SS} as close as possible to V_{CC} and V_{SS} pins.

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Permitted Power dissipation (Mask ROM devices) ^[4]	P_D	-	350	mW	$T_A=105^{\circ}\text{C}$
		-	360	mW	$T_A=125^{\circ}\text{C}$ ^[6]
Operating ambient temperature	T_A	0	+70	$^{\circ}\text{C}$	MB96V300B
		-40	+105		
		-40	+125		^[6]
Storage temperature	T_{STG}	-55	+150	$^{\circ}\text{C}$	

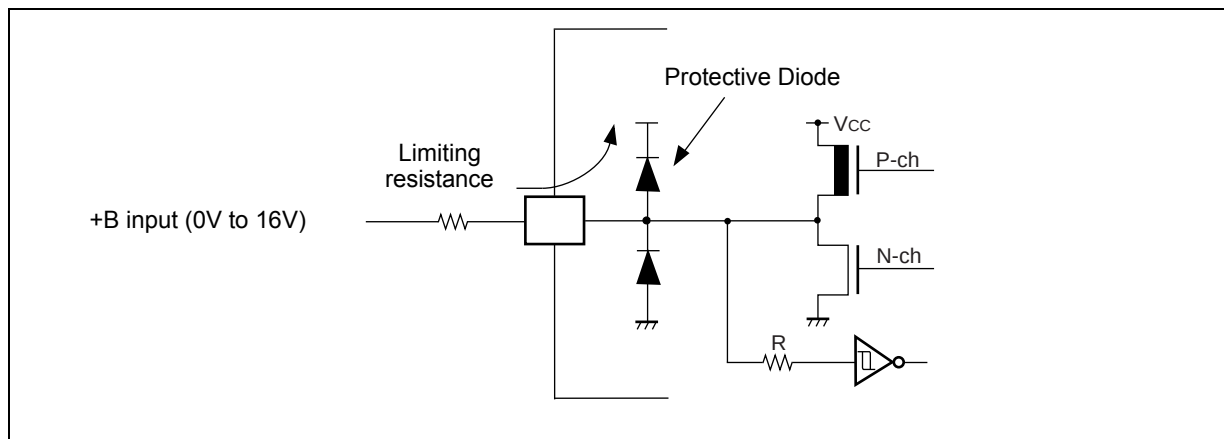
[1]: AV_{CC} and V_{CC} must be set to the same voltage. It is required that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} neither when the power is switched on.

[2]: V_I and V_O should not exceed $V_{CC} + 0.3\text{ V}$. V_I should also not exceed the specified ratings. However if the maximum current to/from a input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating. Input/output voltages of standard ports depend on V_{CC} .

[3]:

- Applicable to all general purpose I/O pins (Pnn_m)
- Use within recommended operating conditions.
- Use at DC voltage (current)
- The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the Power reset (except devices with persistent low voltage reset in internal vector mode).

Sample recommended circuits:



[4]: The maximum permitted power dissipation depends on the ambient temperature, the air flow velocity and the thermal conductance of the package on the PCB. The actual power dissipation depends on the customer application and can be calculated as follows:

$$P_D = P_{IO} + P_{INT}$$

$$P_{IO} = \sum (V_{OL} * I_{OL} + V_{OH} * I_{OH}) \text{ (IO load power dissipation, sum is performed on all IO ports)}$$

$$P_{INT} = V_{CC} * (I_{CC} + I_A) \text{ (internal power dissipation)}$$

I_{CC} is the total core current consumption into V_{CC} as described in the "DC characteristics" and depends on the selected operation mode and clock frequency and the usage of functions like Flash programming or the clock modulator. I_A is the analog current consumption into AV_{CC} .

[5]: Worst case value for a package mounted on single layer PCB at specified T_A without air flow.

[6]: Please contact Cypress for reliability limitations when using under these conditions.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed any of these ratings.

14.2 Recommended Operating Conditions

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}	3.0	-	5.5	V	
Smoothing capacitor at C pin	C_S	3.5	4.7 - 10	15	μF	Use a low inductance capacitor (for example X7R ceramic capacitor)

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

($T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = 0\text{V}$)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Run modes ^[1]	I_{CCPLL}	PLL Run mode with $CLKS1/2 = 48\text{MHz}$, $CLKB = CLKP1/2 = 24\text{MHz}$ (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	35	44	mA	Flash devices at 0 Flash wait states
			+125°C	36	47		
			+25°C	17	23	mA	MB96345/346 at 0 ROM wait states
			+125°C	18	25		
		PLL Run mode with $CLKS1/2 = CLKB = CLKP1 = 56\text{MHz}$, $CLKP2 = 28\text{MHz}$ (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	44	57	mA	MB96F346/F347/F348 at 2 Flash wait states
			+125°C	45	60		
			+25°C	25	35	mA	MB96345/346 at 2 ROM wait states
			+125°C	26	37		
		PLL Run mode with $CLKS1/2 = 72\text{MHz}$, $CLKB = CLKP1 = 36\text{MHz}$, $CLKP2 = 18\text{MHz}$ (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	38	50	mA	MB96F346/F347/F348Y/R/Ayy at 1 Flash wait state
			+125°C	39	53		
		PLL Run mode with $CLKS1/2 = 80\text{MHz}$, $CLKB = CLKP1 = 40\text{MHz}$, $CLKP2 = 20\text{MHz}$ (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	TBD	TBD	mA	MB96F345 at 1 Flash wait state
			+125°C	TBD	TBD		
		PLL Run mode with $CLKS1/2 = 96\text{MHz}$, $CLKB = CLKP1 = 48\text{MHz}$, $CLKP2 = 24\text{MHz}$ (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	49	62	mA	MB96F348T/H/CyB/C at 1 Flash wait state
			+125°C	50	65		
			+25°C	26	36	mA	MB96345/346 at 1 ROM wait state
			+125°C	27	38		
	I_{CCMAIN}	Main Run mode with $CLKS1/2 = CLKB = CLKP1/2 = 4\text{MHz}$ (CLKPLL, CLKSC and CLKRC stopped)	+25°C	4.5	5.5	mA	Flash devices at 1 Flash wait state
			+125°C	5.1	8.5		
			+25°C	2.5	3.5	mA	MB96345/346 at 1 ROM wait state
			+125°C	3.1	5.5		

($T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = 0\text{V}$)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Run modes ^[1]	I_{CCRCH}	RC Run mode with $CLKS1/2 = CLKB = CLKP1/2 = 2\text{MHz}$ (CLKMC, CLKPLL and CLKSC stopped)	+25°C	2.9	4	mA	Flash devices at 1 Flash wait state
			+125°C	3.5	6.5		
			+25°C	1.7	2.7	mA	MB96345/346 at 1 ROM wait state
			+125°C	2.3	4.7		
	I_{CCRCL}	RC Run mode with $CLKS1/2 = CLKB = CLKP1/2 = 100\text{kHz}$, SMCR:LPMS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)	+25°C	0.4	0.6	mA	MB96F346/F347/F348 at 1 Flash wait state
			+125°C	0.9	3.5		
			+25°C	0.18	0.3	mA	MB96F345 at 1 Flash wait state
			+125°C	0.68	3.3		
			+25°C	0.4	0.6	mA	MB96345/346 at 1 ROM wait state
			+125°C	0.9	2.4		
		RC Run mode with $CLKS1/2 = CLKB = CLKP1/2 = 100\text{kHz}$, SMCR:LPMS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode, no Flash programming/erasing allowed)	+25°C	0.15	0.25	mA	Flash devices at 1 Flash wait state
			+125°C	0.65	3.2		
			+25°C	0.15	0.25	mA	MB96345/346 at 1 ROM wait state
			+125°C	0.65	2.1		
	I_{CCSUB}	Sub Run mode with $CLKS1/2 = CLKB = CLKP1/2 = 32\text{kHz}$ (CLKMC, CLKPLL and CLKRC stopped, no Flash programming/erasing allowed)	+25°C	0.1	0.2	mA	Flash devices at 1 Flash wait state
			+125°C	0.6	3		
			+25°C	0.1	0.2	mA	MB96345/346 at 1 ROM wait state
			+125°C	0.6	2		

14.4.2 Internal Clock timing

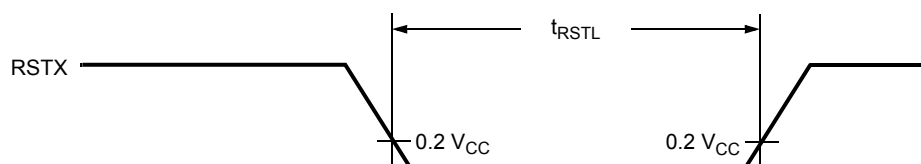
($T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = 0\text{V}$)

Parameter	Symbol	Core Voltage Settings				Unit	Remarks
		1.8V		1.9V			
		Min	Max	Min	Max		
Internal System clock frequency (CLKS1 and CLKS2)	f _{CLKS1} , f _{CLKS2}	0	92	0	96	MHz	Others than below
		0	86	0	96	MHz	MB96F348T/H/CxB/C
		0	72	0	80	MHz	MB96F345
		0	68	0	74	MHz	MB96F34xY/R/Axx
Internal CPU clock frequency (CLKB), internal peripheral clock frequency (CLKP1)	f _{CLKB} , f _{CLKP1}	0	52	0	56	MHz	Others than below
		0	36	0	40	MHz	MB96F345
Internal peripheral clock frequency (CLKP2)	f _{CLKP2}	0	28	0	32	MHz	Others than below
		0	26	0	28	MHz	MB96F34xY/R/Axx

14.4.3 External Reset timing

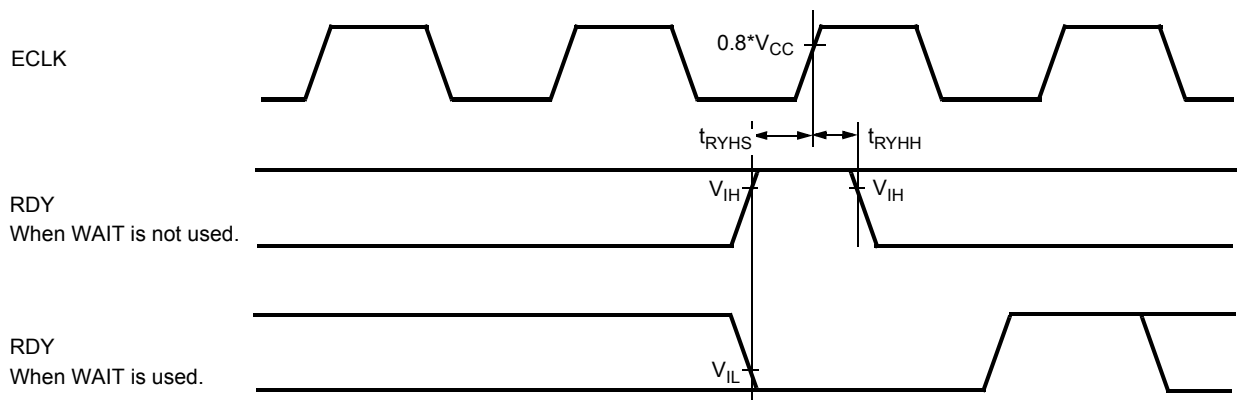
($T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = 0\text{V}$)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Reset input time	t_{RSTL}	RSTX	500	-	-	ns	



($T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 3.0$ to 4.5V , $V_{SS} = 0.0\text{V}$, $I_{Odrive} = 5\text{mA}$, $C_L = 50\text{pF}$)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
WRX pulse width	t_{WLWH}	WRX, WRXL, WRHX	-	$t_{CYC} - 8$	-	ns	w/o cycle extension
Valid data output $\Rightarrow$ WRX $\uparrow$ time	t_{DVWH}	WRX, WRLX, WRHX, AD[15:0]	-	$t_{CYC} - 25$	-	ns	w/o cycle extension
WRX $\uparrow \Rightarrow$ Data hold time	t_{WHDX}	WRX, WRLX, WRHX, AD[15:0]	-	$t_{CYC}/2 - 20$	-	ns	
WRX $\uparrow \Rightarrow$ Address valid time	t_{WHAX}	WRX, WRLX, WRHX, A[23:16]	-	$t_{CYC}/2 - 20$	-	ns	
WRX $\uparrow \Rightarrow$ ALE $\uparrow$ time	t_{WHLH}	WRX, WRLX, WRHX, ALE	EBM:ACE=1 and EACL:STS=1	$2t_{CYC} - 15$	-	ns	
			other EBM:ACE and EACL:STS setting	$t_{CYC} - 15$	-		
WRX $\downarrow \Rightarrow$ ECLK $\uparrow$ time	t_{WLCH}	WRX, WRLX, WRHX, ECLK	-	$t_{CYC}/2 - 15$	-	ns	
CSn $\Rightarrow$ WRX time	t_{CSLWL}	WRX, WRLX, WRHX, CSn	EACL:ACE=0	-	$3t_{CYC}/2 - 20$	ns	
			EACL:ACE=1	-	$5t_{CYC}/2 - 20$		
WRX $\Rightarrow$ CSn time	t_{WHCSH}	WRX, WRLX, WRHX, CSn	-	$t_{CYC}/2 - 20$	-	ns	



Refer to the Hardware Manual for detailed Timing Charts

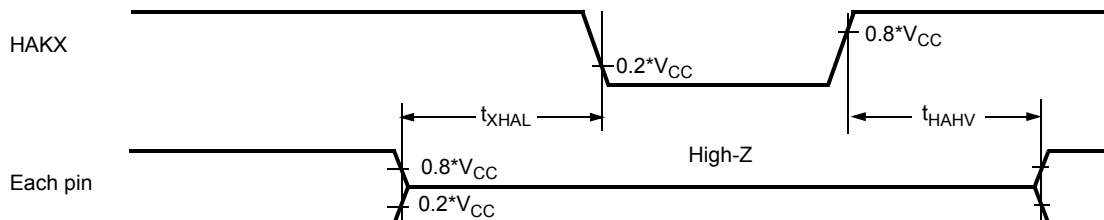
14.4.11 Hold Timing

($T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $I_{O\text{drive}} = 5\text{mA}$, $C_L = 50\text{pF}$)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min	Max		
Pin floating $\Rightarrow$ HAKX $\downarrow$ time	$t_{X\text{HAL}}$	HAKX	-	$t_{CYC} - 20$	$t_{CYC} + 20$	ns	
HAKX $\uparrow$ time $\Rightarrow$ Pin valid time	t_{HAHV}	HAKX		$t_{CYC} - 20$	$t_{CYC} + 20$	ns	

($T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 3.0$ to 4.5V , $V_{SS} = 0.0\text{ V}$, $I_{O\text{drive}} = 5\text{mA}$, $C_L = 50\text{pF}$)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min	Max		
Pin floating $\Rightarrow$ HAKX $\downarrow$ time	$t_{X\text{HAL}}$	HAKX	-	$t_{CYC} - 25$	$t_{CYC} + 25$	ns	
HAKX $\uparrow$ time $\Rightarrow$ Pin valid time	t_{HAHV}	HAKX		$t_{CYC} - 25$	$t_{CYC} + 25$	ns	



Refer to the Hardware Manual for detailed Timing Charts

14.4.13 I²C Timing

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

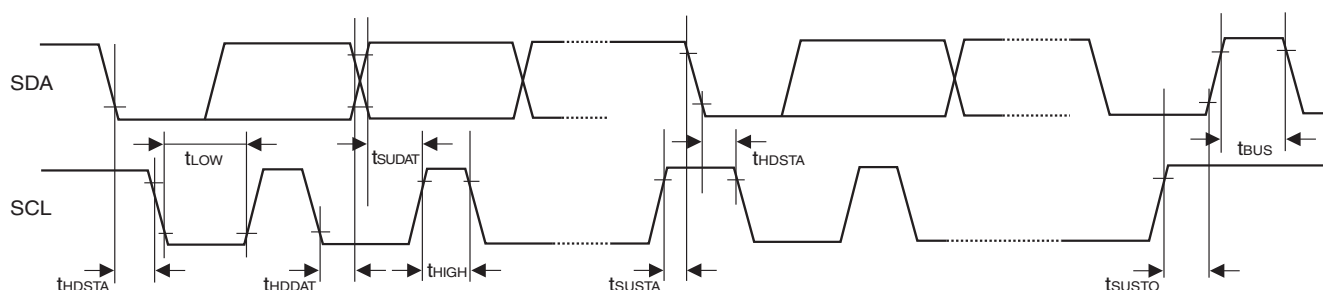
Parameter	Symbol	Condition	Standard-mode		Fast-mode ^[4]		Unit
			Min	Max	Min	Max	
SCL clock frequency	f _{SCL}	R = 1.7 kΩ, C = 50 pF ^[1]	0	100	0	400	kHz
Hold time (repeated) START condition SDA↓→SCL→	t _{HDSTA}		4.0	-	0.6	-	μs
"L" width of the SCL clock	t _{LOW}		4.7	-	1.3	-	μs
"H" width of the SCL clock	t _{HIGH}		4.0	-	0.6	-	μs
Set-up time for a repeated START condition SCL↓→SDA↑	t _{SUSTA}		4.7	-	0.6	-	μs
Data hold time SCL↑→SDA↓	t _{HDDAT}		0	3.45 ^[2]	0	0.9 ^[3]	μs
Data set-up time SDA↑↓→SCL↑	t _{SUDAT}		250	-	100	-	ns
Set-up time for STOP condition SCL↑→SDA↑	t _{SUSTO}		4.0	-	0.6	-	μs
Bus free time between a STOP and START condition	t _{BUS}		4.7	-	1.3	-	μs

[1] : R,C: Pull-up resistor and load capacitor of the SCL and SDA lines.

[2]: The maximum t_{HDDAT} have only to be met if the device does not stretch the "L" width (t_{LOW}) of the SCL signal.

[3] : A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement t_{SUDAT} ≥ 250 ns must then be met.

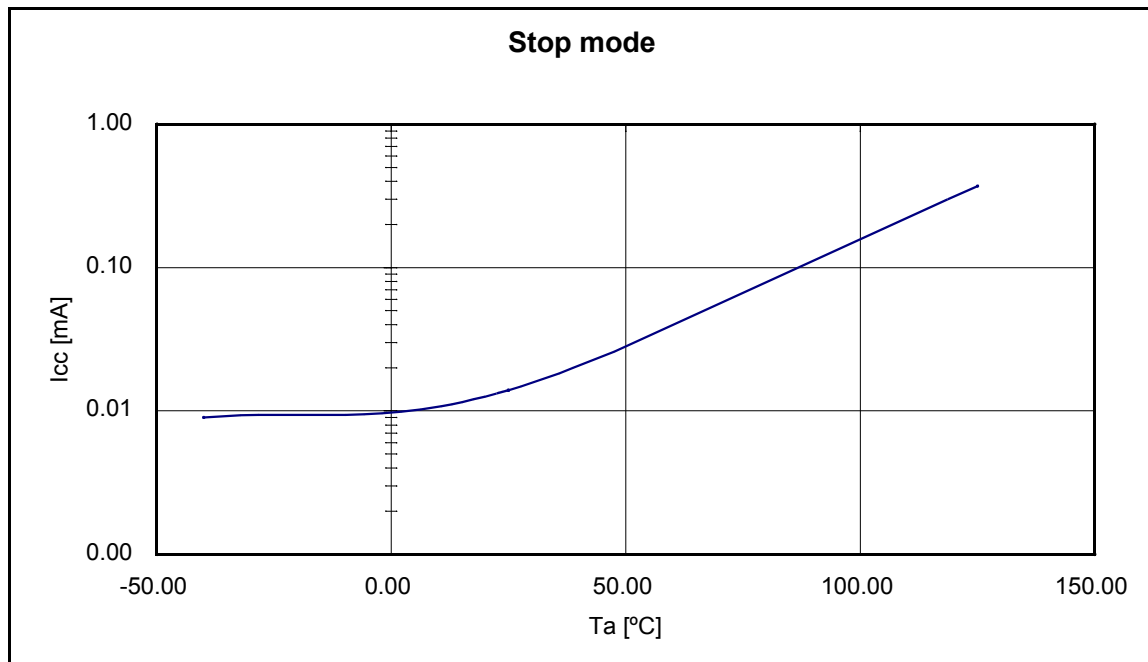
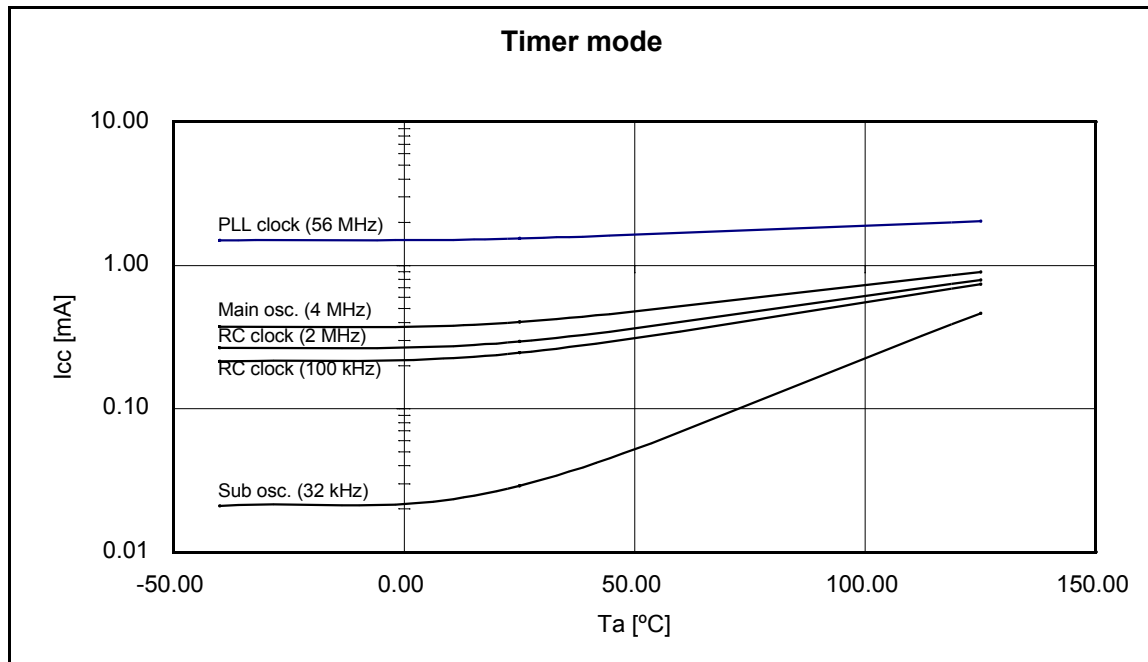
[4] : For use at over 100 kHz, set the peripheral clock 1 to at least 6 MHz.



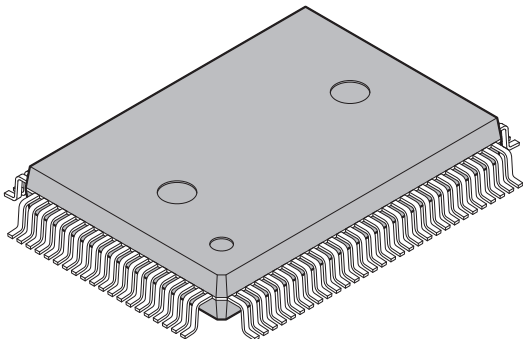
14.6 Alarm Comparator

($T_A = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$, $V_{CC} = AV_{CC} = 3.0\text{V} - 5.5\text{V}$, $V_{SS} = AV_{SS} = 0\text{V}$)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Power supply current	I_{A5ALMF}	AV_{CC}	-	25	45	μA	Alarm comparator enabled in fast mode (one channel)
	I_{A5ALMS}		-	7	13	μA	Alarm comparator enabled in slow mode (one channel)
	I_{A5ALMH}		-	-	5	μA	Alarm comparator disabled
ALARM pin input current	I_{ALIN}	ALARM0, ALARM1	-1	-	+1	μA	$T_A = 25\text{ }^{\circ}\text{C}$
			-3	-	+3	μA	$T_A = 125\text{ }^{\circ}\text{C}$
ALARM pin input voltage range	V_{ALIN}		0	-	AV_{CC}	V	
External low threshold high->low transition	$V_{EVT(L\rightarrow H)}$		$0.36 \cdot AV_{CC} - 0.25$	$0.36 \cdot AV_{CC} - 0.1$	-	V	INTREF = 0
External low threshold low->high transition	$V_{EVT(H\rightarrow L)}$		-	$0.36 \cdot AV_{CC} + 0.1$	$0.36 \cdot AV_{CC} + 0.25$	V	
External high threshold high->low transition	$V_{EVTH(L\rightarrow H)}$		$0.78 \cdot AV_{CC} - 0.25$	$0.78 \cdot AV_{CC} - 0.1$	-	V	
External high threshold low->high transition	$V_{EVTH(H\rightarrow L)}$		-	$0.78 \cdot AV_{CC} + 0.1$	$0.78 \cdot AV_{CC} + 0.25$	V	
Internal low threshold high->low transition	$V_{IVTL(H\rightarrow L)}$		0.9	1.1	-	V	INTREF = 1
Internal low threshold low->high transition	$V_{IVTL(L\rightarrow H)}$		-	1.3	1.55	V	
Internal high threshold high->low transition	$V_{IVTH(H\rightarrow L)}$		2.2	2.4	-	V	
Internal high threshold low->high transition	$V_{IVTH(L\rightarrow H)}$		-	2.6	2.85	V	
Switching hysteresis	V_{HYS}		50	-	300	mV	
Comparison time	t_{COMPF}		-	0.1	1	μs	CMD = 1 (fast)
	t_{COMPS}		-	1	10	μs	CMD = 0 (slow)
Power-up stabilization time after enabling alarm comparator	t_{PD}		-	1	5	ms	Threshold levels specified above are not guaranteed within this time
Slow/Fast mode transition time	t_{CMD}		-	100	500	μs	



17. Package Dimension MB96(F)34x QFP 100P

100-pin plastic QFP  (FPT-100P-M22)	Lead pitch	0.65 mm
	Package width × package length	14.00 mm × 20.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	3.35 mm MAX
	Code (Reference)	P-QFP100-14×20-0.65

