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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

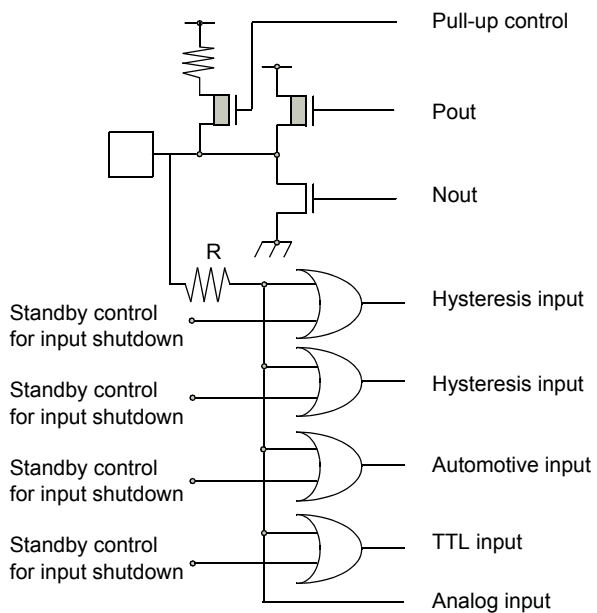
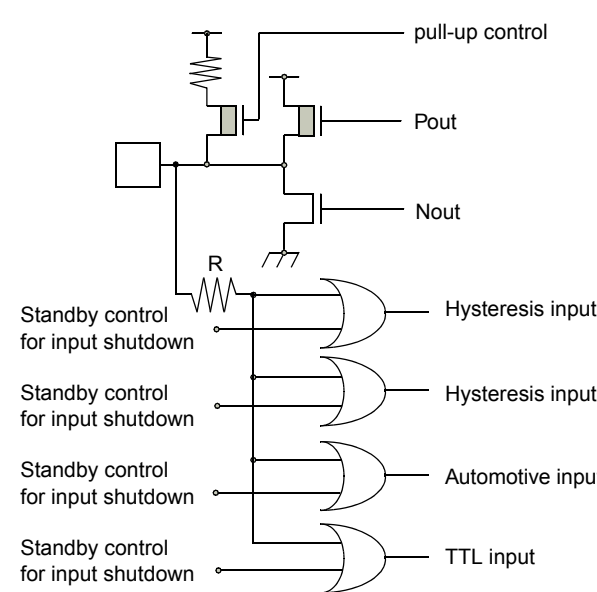
Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Discontinued at Digi-Key
Core Processor	F ² MC-16FX
Core Size	16-Bit
Speed	56MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, LVR, POR, PWM, WDT
Number of I/O	82
Program Memory Size	544KB (544K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-PQFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f348rsbpqc-gse2

Table 1: Pin Function description

Pin name	Feature	Description
RDY	External bus	External bus interface external wait state request input
RSTX	Core	Reset input
RXn	CAN	CAN interface n RX input
SCKn	USART	USART n serial clock input/output
SCKn_R	USART	Relocated USART n serial clock input/output
SCLn	I ² C	I ² C interface n clock I/O input/output
SDAn	I ² C	I ² C interface n serial data I/O input/output
SINn	USART	USART n serial data input
SINn_R	USART	Relocated USART n serial data input
SOTn	USART	USART n serial data output
SOTn_R	USART	Relocated USART n serial data output
TINn	Reload Timer	Reload Timer n event input
TOTn	Reload Timer	Reload Timer n output
TTGn	PPG	Programmable Pulse Generator n trigger input
TXn	CAN	CAN interface n TX output
UBX	External bus	External Bus Interface Upper Byte select strobe output
V _{CC}	Supply	Power supply
V _{SS}	Supply	Power supply
WOT	RTC	Real Timer clock output
WRHX	External bus	External bus High byte write strobe output
WRLX/WRX	External bus	External bus Low byte / Word write strobe output
X0	Clock	Oscillator input
X0A	Clock	Subclock Oscillator input (only for devices with suffix "W")
X1	Clock	Oscillator output
X1A	Clock	Subclock Oscillator output (only for devices with suffix "W")

Type	Circuit	Remarks
I	 Pull-up control Pout Nout R Standby control for input shutdown Hysteresis input Standby control for input shutdown Hysteresis input Standby control for input shutdown Automotive input Standby control for input shutdown TTL input Analog input	■ CMOS level output (programmable $I_{OL} = 5\text{mA}$, $I_{OH} = -5\text{mA}$ and $I_{OL} = 2\text{mA}$, $I_{OH} = -2\text{mA}$) ■ 2 different CMOS hysteresis inputs with input shutdown function * ■ Automotive input with input shutdown function ■ TTL input with input shutdown function * ■ Programmable pull-up resistor: 50kΩ approx. ■ Analog input *MB96F345Dyy or MB96F345Fyy: Only Automotive input and CMOS hysteresis input (0.7/0.3) are supported
N	 pull-up control Pout Nout R Standby control for input shutdown Hysteresis input Standby control for input shutdown Hysteresis input Standby control for input shutdown Automotive input Standby control for input shutdown TTL input	■ CMOS level output ($I_{OL} = 3\text{mA}$, $I_{OH} = -3\text{mA}$) ■ 2 different CMOS hysteresis inputs with input shutdown function * ■ Automotive input with input shutdown function ■ TTL input with input shutdown function * ■ Programmable pull-up resistor: 50kΩ approx. *MB96F345Dyy or MB96F345Fyy: Only Automotive input and CMOS hysteresis input (0.7/0.3) are supported

8. User ROM Memory Map For Flash Devices

MB96F345D MB96F345F					
Alternative mode CPU address	Flash memory mode address	Flash size 160kByte +64KByte Data Flash			
FF:FFFF _H FF:0000 _H	3F:FFFF _H 3F:0000 _H	S39 - 64K	Flash A		
FE:FFFF _H FE:0000 _H	3E:FFFF _H 3E:0000 _H	S38 - 64K			
FD:FFFF _H FD:0000 _H	3D:FFFF _H 3D:0000 _H	External bus			
FC:FFFF _H FC:0000 _H	3C:FFFF _H 3C:0000 _H				
FB:FFFF _H FB:0000 _H	3B:FFFF _H 3B:0000 _H				
FA:FFFF _H FA:0000 _H	3A:FFFF _H 3A:0000 _H				
F9:FFFF _H F9:0000 _H	39:FFFF _H 39:0000 _H				
F8:FFFF _H F8:0000 _H	38:FFFF _H 38:0000 _H				
F7:FFFF _H F7:0000 _H	37:FFFF _H 37:0000 _H				
F6:FFFF _H F6:0000 _H	36:FFFF _H 36:0000 _H				
F5:FFFF _H F5:0000 _H	35:FFFF _H 35:0000 _H				
F4:FFFF _H F4:0000 _H	34:FFFF _H 34:0000 _H				
F3:FFFF _H F3:0000 _H	33:FFFF _H 33:0000 _H				
F2:FFFF _H F2:0000 _H	32:FFFF _H 32:0000 _H				
F1:FFFF _H F1:0000 _H	31:FFFF _H 31:0000 _H				
F0:FFFF _H F0:0000 _H	30:FFFF _H 30:0000 _H				
E0:FFFF _H E0:0000 _H					
DF:FFFF _H DF:8000 _H				Reserved	
DF:7FFF _H DF:6000 _H	1F:7FFF _H 1F:6000 _H			SA3 - 8K	Flash A
DF:5FFF _H DF:4000 _H	1F:5FFF _H 1F:4000 _H			SA2 - 8K	
DF:3FFF _H DF:2000 _H	1F:3FFF _H 1F:2000 _H			SA1 - 8K	
DF:1FFF _H DF:0000 _H	1F:1FFF _H 1F:0000 _H			SA0 - 8K ^[1]	
DE:FFFF _H DE:0000 _H				Reserved	
0E:FFFF _H 0E:FF00 _H	(0E:FFFF _H) (0E:FF00 _H)			SDA0-256 ^[2]	Data Flash A
0E:FEFF _H 0E:0000 _H				Reserved	
0D:FFFF _H 0D:C000 _H	(0F:FFFF _H) (0F:C000 _H)	SDA4-16K	Data Flash A		
0D:BFFF _H 0D:8000 _H	(0F:BFFF _H) (0F:8000 _H)	SDA3-16K			
0D:7FFF _H 0D:4000 _H	(0F:7FFF _H) (0F:4000 _H)	SDA2-16K			
0D:3FFF _H 0D:0000 _H	(0F:3FFF _H) (0F:0000 _H)	SDA1-16K			
0C:FFFF _H 0C:0000 _H		Reserved			

[1]: Sector SA0 contains the ROM Configuration Block RCBA at CPU address DF:0000_H - DF:007F_H

[2]: Sector SDA0 contains the ROM Configuration Block RCBDA at CPU address DE:FF00_H - DE:FF2F_H

		MB96F346Y MB96F346R MB96F346A		MB96F347Y MB96F347R MB96F347A	
Alternative mode CPU address	Flash memory mode address	Flash size 288kByte		Flash size 416kByte	
FF:FFFF _H FF:0000 _H	3F:FFFF _H 3F:0000 _H	S39 - 64K		S39 - 64K	Flash A
FE:FFFF _H FE:0000 _H	3E:FFFF _H 3E:0000 _H	S38 - 64K		S38 - 64K	
FD:FFFF _H FD:0000 _H	3D:FFFF _H 3D:0000 _H	S37 - 64K		S37 - 64K	
FC:FFFF _H FC:0000 _H	3C:FFFF _H 3C:0000 _H	S36 - 64K		S36 - 64K	
FB:FFFF _H FB:0000 _H	3B:FFFF _H 3B:0000 _H	External bus		S35 - 64K	
FA:FFFF _H FA:0000 _H	3A:FFFF _H 3A:0000 _H			S34 - 64K	
F9:FFFF _H F9:0000 _H	39:FFFF _H 39:0000 _H		External bus		
F8:FFFF _H F8:0000 _H	38:FFFF _H 38:0000 _H				
F7:FFFF _H F7:0000 _H	37:FFFF _H 37:0000 _H				
F6:FFFF _H F6:0000 _H	36:FFFF _H 36:0000 _H				
F5:FFFF _H F5:0000 _H	35:FFFF _H 35:0000 _H				
F4:FFFF _H F4:0000 _H	34:FFFF _H 34:0000 _H				
F3:FFFF _H F3:0000 _H	33:FFFF _H 33:0000 _H				
F2:FFFF _H F2:0000 _H	32:FFFF _H 32:0000 _H				
F1:FFFF _H F1:0000 _H	31:FFFF _H 31:0000 _H				
F0:FFFF _H F0:0000 _H	30:FFFF _H 30:0000 _H				
E0:FFFF _H E0:0000 _H					
DF:FFFF _H DF:8000 _H		Reserved		Reserved	Flash A
DF:7FFF _H DF:6000 _H	1F:7FFF _H 1F:6000 _H	SA3 - 8K		SA3 - 8K	
DF:5FFF _H DF:4000 _H	1F:5FFF _H 1F:4000 _H	SA2 - 8K		SA2 - 8K	
DF:3FFF _H DF:2000 _H	1F:3FFF _H 1F:2000 _H	SA1 - 8K		SA1 - 8K	
DF:1FFF _H DF:0000 _H	1F:1FFF _H 1F:0000 _H	SA0 - 8K [1]		SA0 - 8K [1]	
DE:FFFF _H DE:0000 _H		Reserved		Reserved	

[1]: Sector SA0 contains the ROM Configuration Block RCBA at CPU address DF:0000_H - DF:007F_H

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000114 _H	DMA2 - I/O register address pointer low byte	IOAL2	IOA2	R/W
000115 _H	DMA2 - I/O register address pointer high byte	IOAH2		R/W
000116 _H	DMA2 - Data counter low byte	DCTL2	DCT2	R/W
000117 _H	DMA2 - Data counter high byte	DCTH2		R/W
000118 _H	DMA3 - Buffer address pointer low byte	BAPL3		R/W
000119 _H	DMA3 - Buffer address pointer middle byte	BAPM3		R/W
00011A _H	DMA3 - Buffer address pointer high byte	BAPH3		R/W
00011B _H	DMA3 - DMA control register	DMACS3		R/W
00011C _H	DMA3 - I/O register address pointer low byte	IOAL3	IOA3	R/W
00011D _H	DMA3 - I/O register address pointer high byte	IOAH3		R/W
00011E _H	DMA3 - Data counter low byte	DCTL3	DCT3	R/W
00011F _H	DMA3 - Data counter high byte	DCTH3		R/W
000120 _H	DMA4 - Buffer address pointer low byte	BAPL4		R/W
000121 _H	DMA4 - Buffer address pointer middle byte	BAPM4		R/W
000122 _H	DMA4 - Buffer address pointer high byte	BAPH4		R/W
000123 _H	DMA4 - DMA control register	DMACS4		R/W
000124 _H	DMA4 - I/O register address pointer low byte	IOAL4	IOA4	R/W
000125 _H	DMA4 - I/O register address pointer high byte	IOAH4		R/W
000126 _H	DMA4 - Data counter low byte	DCTL4	DCT4	R/W
000127 _H	DMA4 - Data counter high byte	DCTH4		R/W
000128 _H	DMA5 - Buffer address pointer low byte	BAPL5		R/W
000129 _H	DMA5 - Buffer address pointer middle byte	BAPM5		R/W
00012A _H	DMA5 - Buffer address pointer high byte	BAPH5		R/W
00012B _H	DMA5 - DMA control register	DMACS5		R/W
00012C _H	DMA5 - I/O register address pointer low byte	IOAL5	IOA5	R/W
00012D _H	DMA5 - I/O register address pointer high byte	IOAH5		R/W
00012E _H	DMA5 - Data counter low byte	DCTL5	DCT5	R/W
00012F _H	DMA5 - Data counter high byte	DCTH5		R/W
000130 _H -00017F _H	Reserved			-
000180 _H -00037F _H	CPU - General Purpose registers (RAM access)	GPR_RAM		R/W
000380 _H	DMA0 - Interrupt select	DISEL0		R/W
000381 _H	DMA1 - Interrupt select	DISEL1		R/W

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00058D _H	PPG10 - Duty cycle register			W
00058E _H	PPG10 - Control status register Low	PCNL10	PCN10	R/W
00058F _H	PPG10 - Control status register High	PCNH10		R/W
000590 _H	PPG11 - Timer register		PTMR11	R
000591 _H	PPG11 - Timer register			R
000592 _H	PPG11 - Period setting register		PCSR11	W
000593 _H	PPG11 - Period setting register			W
000594 _H	PPG11 - Duty cycle register		PDUT11	W
000595 _H	PPG11 - Duty cycle register			W
000596 _H	PPG11 - Control status register Low	PCNL11	PCN11	R/W
000597 _H	PPG11 - Control status register High	PCNH11		R/W
000598 _H	PPG15-PPG12 - General Control register 1 Low	GCN1L3	GCN13	R/W
000599 _H	PPG15-PPG12 - General Control register 1 High	GCN1H3		R/W
00059A _H	PPG15-PPG12 - General Control register 2 Low	GCN2L3	GCN23	R/W
00059B _H	PPG15-PPG12 - General Control register 2 High	GCN2H3		R/W
00059C _H	PPG12 - Timer register		PTMR12	R
00059D _H	PPG12 - Timer register			R
00059E _H	PPG12 - Period setting register		PCSR12	W
00059F _H	PPG12 - Period setting register			W
0005A0 _H	PPG12 - Duty cycle register		PDUT12	W
0005A1 _H	PPG12 - Duty cycle register			W
0005A2 _H	PPG12 - Control status register Low	PCNL12	PCN12	R/W
0005A3 _H	PPG12 - Control status register High	PCNH12		R/W
0005A4 _H	PPG13 - Timer register		PTMR13	R
0005A5 _H	PPG13 - Timer register			R
0005A6 _H	PPG13 - Period setting register		PCSR13	W
0005A7 _H	PPG13 - Period setting register			W
0005A8 _H	PPG13 - Duty cycle register		PDUT13	W
0005A9 _H	PPG13 - Duty cycle register			W
0005AA _H	PPG13 - Control status register Low	PCNL13	PCN13	R/W
0005AB _H	PPG13 - Control status register High	PCNH13		R/W
0005AC _H	PPG14 - Timer register		PTMR14	R

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0006EB _H	External Bus - Area configuration register 5 High	EACH5		R/W
0006EC _H	External Bus - Area select register 2	EAS2		R/W
0006ED _H	External Bus - Area select register 3	EAS3		R/W
0006EE _H	External Bus - Area select register 4	EAS4		R/W
0006EF _H	External Bus - Area select register 5	EAS5		R/W
0006F0 _H	External Bus - Mode register	EBM		R/W
0006F1 _H	External Bus - Clock and Function register	EBCF		R/W
0006F2 _H	External Bus - Address output enable register 0	EBAE0		R/W
0006F3 _H	External Bus - Address output enable register 1	EBAE1		R/W
0006F4 _H	External Bus - Address output enable register 2	EBAE2		R/W
0006F5 _H	External Bus - Control signal register	EBCS		R/W
0006F6 _H -0006FF _H	Reserved			-
000700 _H	CAN0 - Control register Low	CTRLRL0	CTRLR0	R/W
000701 _H	CAN0 - Control register High (reserved)	CTRLRH0		R
000702 _H	CAN0 - Status register Low	STATRL0	STATR0	R/W
000703 _H	CAN0 - Status register High (reserved)	STATRH0		R
000704 _H	CAN0 - Error Counter Low (Transmit)	ERRCNTL0	ERRCNT0	R
000705 _H	CAN0 - Error Counter High (Receive)	ERRCNTH0		R
000706 _H	CAN0 - Bit Timing Register Low	BTRL0	BTR0	R/W
000707 _H	CAN0 - Bit Timing Register High	BTRH0		R/W
000708 _H	CAN0 - Interrupt Register Low	INTRL0	INTR0	R
000709 _H	CAN0 - Interrupt Register High	INTRH0		R
00070A _H	CAN0 - Test Register Low	TESTRL0	TESTR0	R/W
00070B _H	CAN0 - Test Register High (reserved)	TESTRH0		R
00070C _H	CAN0 - BRP Extension register Low	BRPERL0	BRPER0	R/W
00070D _H	CAN0 - BRP Extension register High (reserved)	BRPERH0		R
00070E _H -00070F _H	Reserved			-
000710 _H	CAN0 - IF1 Command request register Low	IF1CREQL0	IF1CREQ0	R/W
000711 _H	CAN0 - IF1 Command request register High	IF1CREQH0		R/W
000712 _H	CAN0 - IF1 Command Mask register Low	IF1CMSKL0	IF1CMSK0	R/W
000713 _H	CAN0 - IF1 Command Mask register High (reserved)	IF1CMSKH0		R
000714 _H	CAN0 - IF1 Mask 1 Register Low	IF1MSK1L0	IF1MSK10	R/W

Table 5: Interrupt vector table MB96(F)34x

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
90	294 _H	LINT7	Yes	90	LIN USART 7 TX
91	290 _H	LINR8	Yes	91	LIN USART 8 RX
92	28C _H	LINT8	Yes	92	LIN USART 8 TX
93	288 _H	LINR9	Yes	93	LIN USART 9 RX
94	284 _H	LINT9	Yes	94	LIN USART 9 TX
95	280 _H	RTC0	No	95	Real Timer Clock
96	27C _H	CAL0	No	96	Clock Calibration Unit
97	278 _H	DFLASH_A	Yes	97	Data Flash A (only MB96F345Dyy, MB96F345Fyy)

13.7 Crystal oscillator and ceramic resonator circuit

Noise at X0, X1 pins or X0A, X1A pins might cause abnormal operation. It is required to provide bypass capacitors with shortest possible distance to X0, X1 pins and X0A, X1A pins, crystal oscillator (or ceramic resonator) and ground lines, and, to the utmost effort, that the lines of oscillation circuit do not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board art work surrounding X0, X1 pins and X0A, X1A pins with a ground area for stabilizing the operation.

It is highly recommended to evaluate the quartz/MCU or resonator/MCU system at the quartz or resonator manufacturer, especially when using low-Q resonators at higher frequencies.

13.8 Turn on sequence of power supply to A/D converter and analog inputs

It is required to turn the A/D converter power supply (AV_{CC} , $AVRH$, $AVRL$) and analog inputs (ANn) on after turning the digital power supply (V_{CC}) on.

It is also required to turn the digital power off after turning the A/D converter supply and analog inputs off. In this case, the voltage must not exceed $AVRH$ or AV_{CC} (turning the analog and digital power supplies simultaneously on or off is acceptable).

13.9 Pin handling when not using the A/D converter

It is required to connect the unused pins of the A/D converter as $AV_{CC} = V_{CC}$, $AV_{SS} = AVRH = AVRL = V_{SS}$.

13.10 Notes on Power-on

To prevent malfunction of the internal voltage regulator, supply voltage profile while turning the power supply on should be slower than 50 μ s from 0.2 V to 2.7 V.

13.11 Stabilization of power supply voltage

If the power supply voltage varies acutely even within the operation safety range of the V_{CC} power supply voltage, a malfunction may occur. The V_{CC} power supply voltage must therefore be stabilized. As stabilization guidelines, the power supply voltage must be stabilized in such a way that V_{CC} ripple fluctuations (peak to peak value) in the commercial frequencies (50 to 60 Hz) fall within 10% of the standard V_{CC} power supply voltage and the transient fluctuation rate becomes 0.1V/ μ s or less in instantaneous fluctuation for power supply switching.

13.12 Serial communication

There is a possibility to receive wrong data due to noise or other causes on the serial communication. Therefore, design a printed circuit board so as to avoid noise. Consider receiving of wrong data when designing the system. For example apply a checksum and retransmit the data if an error occurs.

13.13 Handling of Data Flash

The Data Flash requires different and additional control signals for parallel programming. Please check with your programming equipment maker for support of this interface.

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Permitted Power dissipation (Mask ROM devices) ^[4]	P_D	-	350	mW	$T_A=105^{\circ}\text{C}$
		-	360	mW	$T_A=125^{\circ}\text{C}$ [6]
Operating ambient temperature	T_A	0	+70	$^{\circ}\text{C}$	MB96V300B
		-40	+105		
		-40	+125		[6]
Storage temperature	T_{STG}	-55	+150	$^{\circ}\text{C}$	

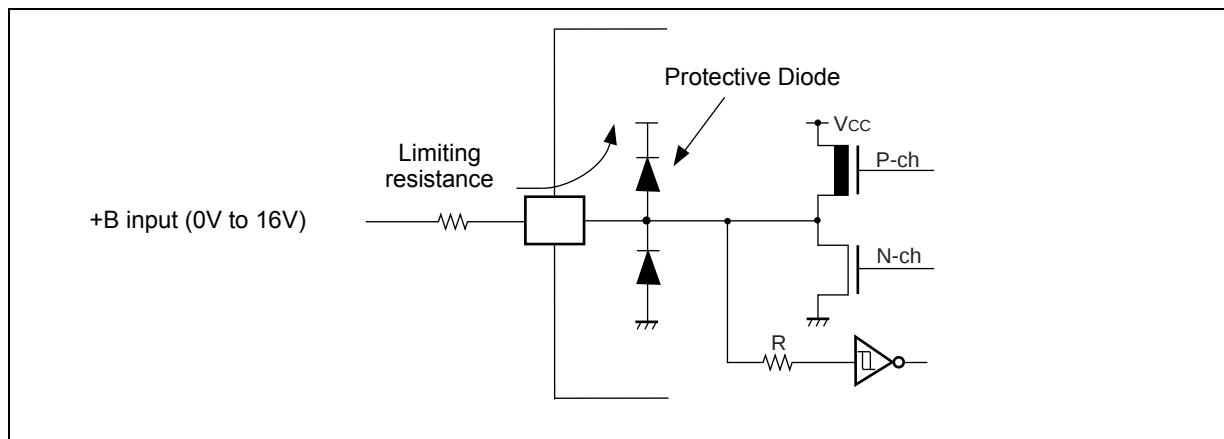
[1]: AV_{CC} and V_{CC} must be set to the same voltage. It is required that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} neither when the power is switched on.

[2]: V_I and V_O should not exceed $V_{CC} + 0.3\text{ V}$. V_I should also not exceed the specified ratings. However if the maximum current to/from a input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating. Input/output voltages of standard ports depend on V_{CC} .

[3]:

- Applicable to all general purpose I/O pins (Pnn_m)
- Use within recommended operating conditions.
- Use at DC voltage (current)
- The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the Power reset (except devices with persistent low voltage reset in internal vector mode).

Sample recommended circuits:



14.3 DC characteristics

($T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = 0\text{V}$)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input H voltage	V_{IH}	Port inputs Pnn_m	CMOS Hysteresis 0.8/0.2 input selected	$0.8 V_{CC}$	-	$V_{CC} + 0.3$	V	
			CMOS Hysteresis 0.7/0.3 input selected	$0.7 V_{CC}$	-	$V_{CC} + 0.3$	V	$V_{CC} \geq 4.5\text{V}$
			AUTOMOTIVE Hys- teresis input selected	$0.74 V_{CC}$	-	$V_{CC} + 0.3$	V	$V_{CC} < 4.5\text{V}$
			TTL input selected	2.0	-	$V_{CC} + 0.3$	V	
	V_{IHX0F}	X0	External clock in "Fast Clock Input mode"	$0.8 V_{CC}$	-	$V_{CC} + 0.3$	V	Not available in MB96F34xY/R/AxA
	V_{IHX0S}	X0,X1, X0A,X1A	External clock in "oscil- lation mode"	2.5	-	$V_{CC} + 0.3$	V	
	V_{IHR}	RSTX	-	$0.8 V_{CC}$	-	$V_{CC} + 0.3$	V	CMOS Hysteresis input
	V_{IHM}	MD2-MD0	-	$V_{CC} - 0.3$	-	$V_{CC} + 0.3$	V	
Input L voltage	V_{IL}	Port inputs Pnn_m	CMOS Hysteresis 0.8/0.2 input selected	$V_{SS} - 0.3$	-	$0.2 V_{CC}$	V	
			CMOS Hysteresis 0.7/0.3 input selected	$V_{SS} - 0.3$	-	$0.3 V_{CC}$	V	
			AUTOMOTIVE Hys- teresis input selected	$V_{SS} - 0.3$	-	$0.5 V_{CC}$	V	$V_{CC} \geq 4.5\text{V}$
			TTL input selected	$V_{SS} - 0.3$	-	0.8	V	$V_{CC} < 4.5\text{V}$
	V_{ILX0F}	X0	External clock in "Fast Clock Input mode"	$V_{SS} - 0.3$	-	$0.2 V_{CC}$	V	Not available in MB96F34xY/R/AxA
	V_{ILX0S}	X0,X1, X0A,X1A	External clock in "oscillation mode"	$V_{SS} - 0.3$	-	0.4	V	
	V_{ILR}	RSTX	-	$V_{SS} - 0.3$	-	$0.2 V_{CC}$	V	CMOS Hysteresis input
	V_{ILM}	MD2-MD0	-	$V_{SS} - 0.3$	-	$V_{SS} + 0.3$	V	
Output H voltage	V_{OH2}	Normal outputs	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $I_{OH} = -2\text{mA}$	$V_{CC} - 0.5$	-	-	V	Driving strength set to 2mA
			$3.0\text{V} \leq V_{CC} < 4.5\text{V}$ $I_{OH} = -1.6\text{mA}$					
	V_{OH5}	Normal outputs	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $I_{OH} = -5\text{mA}$	$V_{CC} - 0.5$	-	-	V	Driving strength set to 5mA
			$3.0\text{V} \leq V_{CC} < 4.5\text{V}$ $I_{OH} = -3\text{mA}$					
	V_{OH3}	3mA outputs	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $I_{OH} = -3\text{mA}$	$V_{CC} - 0.5$	-	-	V	
			$3.0\text{V} \leq V_{CC} < 4.5\text{V}$ $I_{OH} = -2\text{mA}$					

($T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = 0\text{V}$)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Sleep modes ^[1]	I_{CCSPLL}	PLL Sleep mode with $CLKS1/2 = 48\text{MHz}$, $CLKP1/2 = 24\text{MHz}$ (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	9	10.5	mA	Flash devices
			+125°C	9.7	13		
			+25°C	8	9.5	mA	MB96345/346
			+125°C	8.7	11.5		
		PLL Sleep mode with $CLKS1/2 =$ $CLKP1 = 56\text{MHz}$, $CLKP2 = 28\text{MHz}$ (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	14	15.5	mA	MB96F346/F347/F348
			+125°C	14.8	18		
			+25°C	13.5	15	mA	MB96345/346
			+125°C	14.3	17		
		PLL Sleep mode with $CLKS1/2 = 72\text{MHz}$, $CLKP1 = 36\text{MHz}$, $CLKP2 = 18\text{MHz}$ (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	10.5	12	mA	MB96F346/F347/F348Y/R/Ayy
			+125°C	11.3	14.5		
		PLL Sleep mode with $CLKS1/2 = 80\text{MHz}$, $CLKP1 = 40\text{MHz}$, $CLKP2 = 20\text{MHz}$ (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	TBD	TBD	mA	MB96F345
			+125°C	TBD	TBD		
		PLL Sleep mode with $CLKS1/2 = 96\text{MHz}$, $CLKP1 = 48\text{MHz}$, $CLKP2 = 24\text{MHz}$ (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	15	16.5	mA	MB96F348T/H/CyB/C
			+125°C	15.8	19		
			+25°C	14	15.5	mA	MB96345/346
			+125°C	14.8	17.5		
	I_{CCSMAN}	Main Sleep mode with $CLKS1/2 =$ $CLKP1/2 = 4\text{MHz}$ (CLKPLL, CLKSC and CLKRC stopped)	+25°C	1.5	1.8	mA	Flash devices
			+125°C	2	4.5		
			+25°C	1.5	1.8	mA	MB96345/346
			+125°C	2	3.8		

14.4.8 Bus Timing (Read)

($T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $I_{Odrive} = 5\text{mA}$, $C_L = 50\text{pF}$)

Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
ALE pulse width	t_{LHLL}	ALE	EACL:STS=0 and EACL:ACE=0	$t_{CYC}/2 - 5$	-	ns	
			EACL:STS=1	$t_{CYC} - 5$	-		
			EACL:STS=0 and EACL:ACE=1	$3t_{CYC}/2 - 5$	-		
Valid address $\Rightarrow$ ALE $\downarrow$ time	t_{AVLL}	ALE, A[23:16],	EACL:STS=0 and EACL:ACE=0	$t_{CYC} - 15$	-	ns	
			EACL:STS=1 and EACL:ACE=0	$3t_{CYC}/2 - 15$	-		
			EACL:STS=0 and EACL:ACE=1	$2t_{CYC} - 15$	-		
			EACL:STS=1 and EACL:ACE=1	$5t_{CYC}/2 - 15$	-		
	t_{ADVLL}	ALE,AD[15:0]	EACL:STS=0 and EACL:ACE=0	$t_{CYC}/2 - 15$	-	ns	
			EACL:STS=1 and EACL:ACE=0	$t_{CYC} - 15$	-		
			EACL:STS=0 and EACL:ACE=1	$3t_{CYC}/2 - 15$	-		
			EACL:STS=1 and EACL:ACE=1	$2t_{CYC} - 15$	-		
ALE $\downarrow \Rightarrow$ Address valid time	t_{LLAX}	ALE, AD[15:0]	EACL:STS=0	$t_{CYC}/2 - 15$	-	ns	
			EACL:STS=1	-15	-		
Valid address $\Rightarrow$ RDX $\downarrow$ time	t_{AVRL}	RDX, A[23:16]	EACL:ACE=0	$3t_{CYC}/2 - 15$	-	ns	
			EACL:ACE=1	$5t_{CYC}/2 - 15$	-		
	t_{ADVRL}	RDX, AD[15:0]	EACL:ACE=0	$t_{CYC} - 15$	-	ns	
			EACL:ACE=1	$2t_{CYC} - 15$	-		
Valid address $\Rightarrow$ Valid data input	t_{AVDV}	A[23:16], AD[15:0]	EACL:ACE=0	-	$3t_{CYC} - 55$	ns	w/o cycle extension
			EACL:ACE=1	-	$4t_{CYC} - 55$		
	$t_{ADV DV}$	AD[15:0]	EACL:ACE=0	-	$5t_{CYC}/2 - 55$	ns	w/o cycle extension
			EACL:ACE=1	-	$7t_{CYC}/2 - 55$		
RDX pulse width	t_{RLRH}	RDX	-	$3 t_{CYC}/2 - 5$	-	ns	w/o cycle extension
RDX $\downarrow \Rightarrow$ Valid data input	t_{RLDV}	RDX, AD[15:0]	-	-	$3 t_{CYC}/2 - 50$	ns	w/o cycle extension
RDX $\uparrow \Rightarrow$ Data hold time	t_{RHDX}	RDX, AD[15:0]	-	0	-	ns	
Address valid $\Rightarrow$ Data hold time	t_{AXDX}	A[23:16], AD[15:0]	-	0	-	ns	

($T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $I_{Odrive} = 5\text{mA}$, $C_L = 50\text{pF}$)

Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
RDX $\uparrow \Rightarrow$ ALE $\uparrow$ time	t_{RHLH}	RDX, ALE	EACL:STS=1 and EACL:ACE=1	$3t_{CYC}/2 - 10$	-	ns	
			other ECL:STS, EACL:ACE setting	$t_{CYC}/2 - 10$	-		
Valid address $\Rightarrow$ ECLK $\uparrow$ time	t_{AVCH}	A[23:16], ECLK	-	$t_{CYC} - 15$	-	ns	
	t_{ADVCH}	AD[15:0], ECLK		$t_{CYC}/2 - 15$	-		
RDX $\downarrow \Rightarrow$ ECLK $\uparrow$ time	t_{RLCH}	RDX, ECLK	-	$t_{CYC}/2 - 10$	-	ns	
ALE $\downarrow \Rightarrow$ RDX $\downarrow$ time	t_{LLRL}	ALE, RDX	EACL:STS=0	$t_{CYC}/2 - 10$	-	ns	
			EACL:STS=1	- 10	-		
ECLK $\uparrow \Rightarrow$ Valid data input	t_{CHDV}	AD[15:0], ECLK	-	-	$t_{CYC} - 50$	ns	

($T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 3.0$ to 4.5V , $V_{SS} = 0.0\text{ V}$, $I_{Odrive} = 5\text{mA}$, $C_L = 50\text{pF}$)

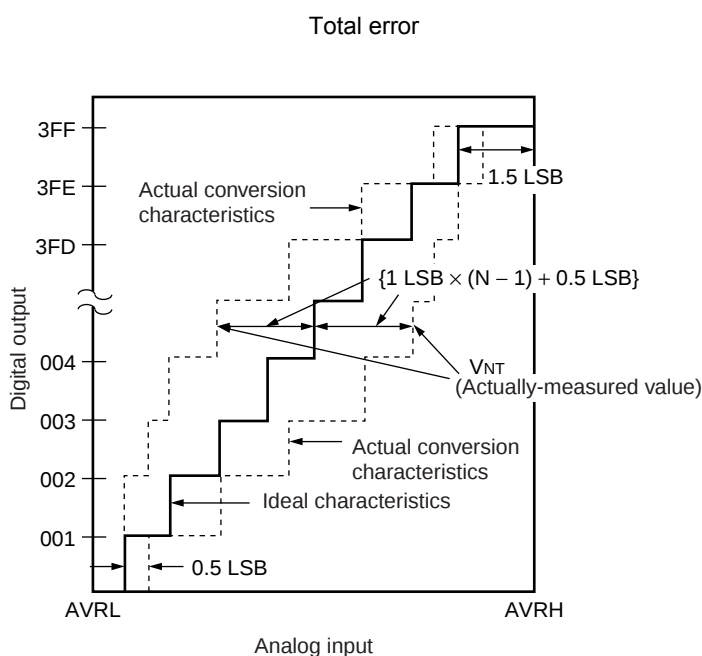
Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
ALE pulse width	t _{LHLL}	ALE	EACL:STS=0 and EACL:ACE=0	t _{CYC} /2 – 8	-	ns	
			EACL:STS=1	t _{CYC} – 8	-		
			EACL:STS=0 and EACL:ACE=1	3t _{CYC} /2 – 8	-		
Valid address ⇒ ALE ↓ time	t _{AVLL}	ALE, A[23:16],	EACL:STS=0 and EACL:ACE=0	t _{CYC} – 20	-	ns	
			EACL:STS=1 and EACL:ACE=0	3t _{CYC} /2 – 20	-		
			EACL:STS=0 and EACL:ACE=1	2t _{CYC} – 20	-		
			EACL:STS=1 and EACL:ACE=1	5t _{CYC} /2 – 20	-		
	t _{ADVLL}	ALE, AD[15:0]	EACL:STS=0 and EACL:ACE=0	t _{CYC} /2 – 20	-	ns	
			EACL:STS=1 and EACL:ACE=0	t _{CYC} – 20	-		
			EACL:STS=0 and EACL:ACE=1	3t _{CYC} /2 – 20	-		
			EACL:STS=1 and EACL:ACE=1	2t _{CYC} – 20	-		
ALE ↓ ⇒ Address valid time	t _{LLAX}	ALE, AD[15:0]	EACL:STS=0	t _{CYC} /2 – 20	-	ns	
			EACL:STS=1	-20	-		
Valid address ⇒ RDX ↓ time	t _{AVRL}	RDX, A[23:16]	EACL:ACE=0	3t _{CYC} /2 – 20	-	ns	
			EACL:ACE=1	5t _{CYC} /2 – 20	-		
	t _{ADVRL}	RDX, AD[15:0]	EACL:ACE=0	t _{CYC} – 20	-	ns	
			EACL:ACE=1	2t _{CYC} – 20	-		

($T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 3.0$ to 4.5V , $V_{SS} = 0.0\text{V}$, $I_{Odrive} = 5\text{mA}$, $C_L = 50\text{pF}$)

Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
Valid address $\Rightarrow$ Valid data input	t_{AVDV}	A[23:16], AD[15:0]	EACL:ACE=0	-	$3t_{CYC} - 60$	ns	w/o cycle extension
			EACL:ACE=1	-	$4t_{CYC} - 60$		
	$t_{ADV DV}$	AD[15:0]	EACL:ACE=0	-	$5t_{CYC}/2 - 60$	ns	w/o cycle extension
			EACL:ACE=1	-	$7t_{CYC}/2 - 60$		
RDX pulse width	t_{RLRH}	RDX	-	$3t_{CYC}/2 - 8$	-	ns	w/o cycle extension
RDX $\downarrow \Rightarrow$ Valid data input	t_{RLDV}	RDX, AD[15:0]	-	-	$3t_{CYC}/2 - 55$	ns	w/o cycle extension
RDX $\uparrow \Rightarrow$ Data hold time	t_{RHDX}	RDX, AD[15:0]	-	0	-	ns	
Address valid $\Rightarrow$ Data hold time	t_{AXDX}	A[23:16]	-	0	-	ns	
RDX $\uparrow \Rightarrow$ ALE $\uparrow$ time	t_{RHLH}	RDX, ALE	EACL:STS=1 and EACL:ACE=1	$3t_{CYC}/2 - 15$	-	ns	
			other ECL:STS, EA-CL:ACE setting	$t_{CYC}/2 - 15$	-		
Valid address $\Rightarrow$ ECLK $\uparrow$ time	t_{AVCH}	A[23:16], ECLK	-	$t_{CYC} - 20$	-	ns	
	t_{ADVCH}	AD[15:0], ECLK		$t_{CYC}/2 - 20$	-		
RDX $\downarrow \Rightarrow$ ECLK $\uparrow$ time	t_{RLCH}	RDX, ECLK	-	$t_{CYC}/2 - 15$	-	ns	
ALE $\downarrow \Rightarrow$ RDX $\downarrow$ time	t_{LLRL}	ALE, RDX	EACL:STS=0	$t_{CYC}/2 - 15$	-	ns	
			EACL:STS=1	- 15	-		
ECLK $\uparrow \Rightarrow$ Valid data input	t_{CHDV}	AD[15:0], ECLK	-	-	$t_{CYC} - 55$	ns	

14.5.1 Definition of A/D Converter Terms

- **Resolution:** Analog variation that is recognized by an A/D converter.
- **Total error:** Difference between the actual value and the ideal value. The total error includes zero transition error, full-scale transition error and nonlinearity error.
- **Nonlinearity error:** Deviation between a line across zero-transition line ("00 0000 0000" <--> "00 0000 0001") and full-scale transition line ("11 1111 1110" <--> "11 1111 1111") and actual conversion characteristics.
- **Differential nonlinearity error:** Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.
- **Zero reading voltage:** Input voltage which results in the minimum conversion value.
- **Full scale reading voltage:** Input voltage which results in the maximum conversion value.



$$\text{Total error of digital output "N"} = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + 0.5 \text{ LSB}\}}{1 \text{ LSB}} \quad [\text{LSB}]$$

$$1 \text{ LSB} = (\text{Ideal value}) \quad \frac{AVRH - AVRL}{1024} \quad [\text{V}]$$

N: A/D converter digital output value

$$V_{OT} (\text{Ideal value}) = AVRL + 0.5 \text{ LSB} \quad [\text{V}]$$

$$V_{FST} (\text{Ideal value}) = AVRH - 1.5 \text{ LSB} \quad [\text{V}]$$

V_{NT} : A voltage at which digital output transitions from (N - 1) to N.

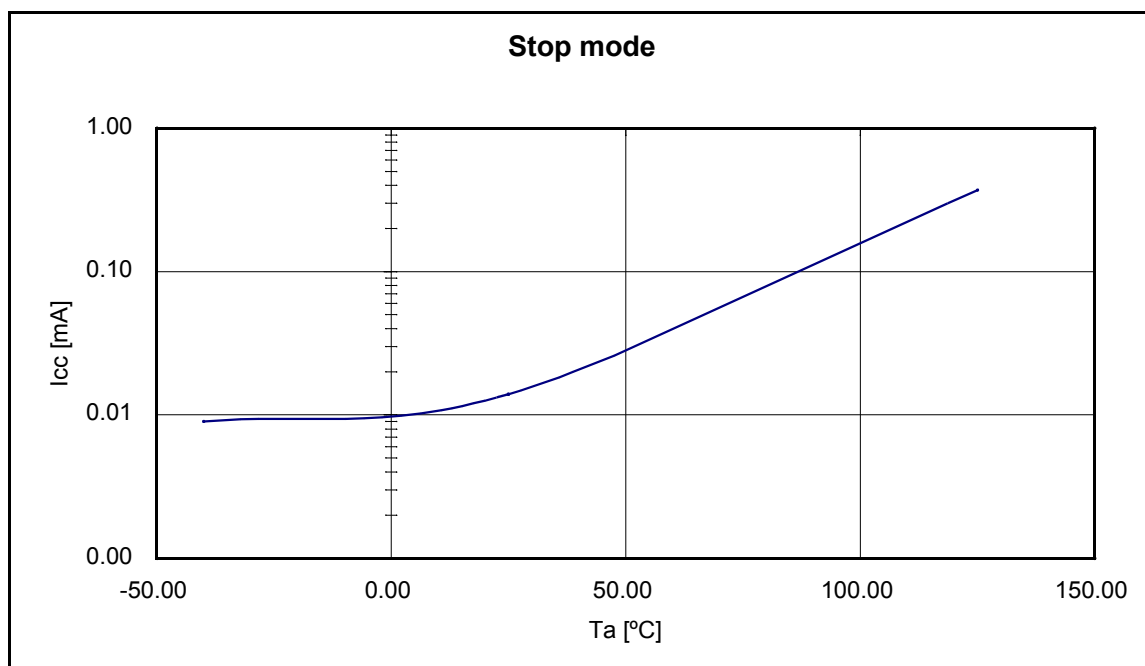
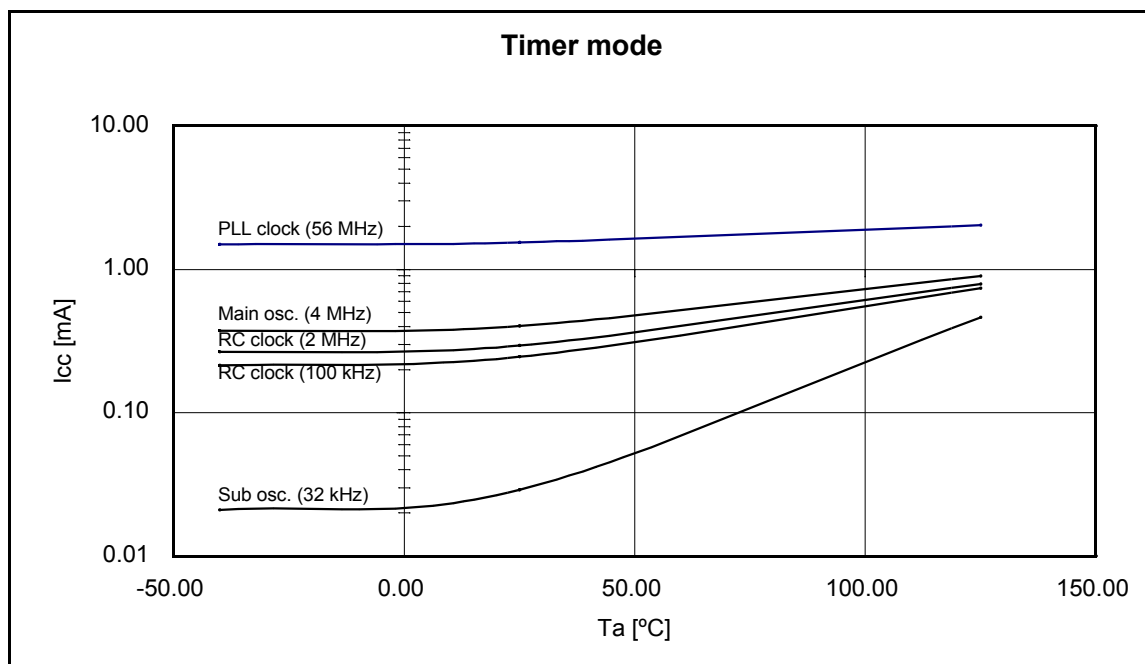


Table 6: Used settings

Mode	Selected Source Clock	Clock/Regulator Settings
Timer mode	PLL	CLKMC = 4 MHz, CLKPLL = 56 MHz (System clocks are stopped in this mode) Regulator in High Power Mode, Core Voltage = 1.9 V
	Main osc.	CLKMC = 4 MHz (System clocks are stopped in this mode) Regulator in High Power Mode, Core Voltage = 1.8 V
	RC clock fast	CLKRC = 2 MHz (System clocks are stopped in this mode) Regulator in High Power Mode, Core Voltage = 1.8 V
	RC clock slow	CLKRC = 100 kHz (System clocks are stopped in this mode) Regulator in High Power Mode, Core Voltage = 1.8 V
	Sub osc.	CLKSC = 100 kHz (System clocks are stopped in this mode) Regulator in Low Power Mode A, Core Voltage = 1.8 V
Stop mode	stopped	(All clocks are stopped in this mode) Regulator in Low Power Mode B, Core Voltage = 1.8 V

18. Ordering Information

18.1 MCU with CAN Controller

Part number	Flash/ROM	Subclock	Persistent Low Voltage Reset	Package
MB96345YSA PQC-GSE2 ^[1]	ROM (160KB)	No	Yes	100 pin Plastic QFP (FPT-100P-M22)
MB96345RSA PQC-GSE2 ^[1]			No	
MB96345YWA PQC-GSE2 ^[1]		Yes	Yes	
MB96345RWA PQC-GSE2 ^[1]			No	
MB96345YSA PMC-GSE2 ^[1]		No	Yes	100 pin Plastic LQFP (FPT-100P-M20)
MB96345RSA PMC-GSE2 ^[1]			No	
MB96345YWA PMC-GSE2 ^[1]		Yes	Yes	
MB96345RWA PMC-GSE2 ^[1]			No	
MB96346YSA PQC-GSE2 ^[1]	ROM (288KB)	No	Yes	100 pin Plastic QFP (FPT-100P-M22)
MB96346RSA PQC-GSE2 ^[1]			No	
MB96346YWA PQC-GSE2 ^[1]		Yes	Yes	
MB96346RWA PQC-GSE2 ^[1]			No	
MB96346YSA PMC-GSE2 ^[1]		No	Yes	100 pin Plastic LQFP (FPT-100P-M20)
MB96346RSA PMC-GSE2 ^[1]			No	
MB96346YWA PMC-GSE2 ^[1]		Yes	Yes	
MB96346RWA PMC-GSE2 ^[1]			No	
MB96F345FSA PQC-GSE2 ^[1]	Flash A (160KB) Data Flash A (64KB)	No	Yes	100 pin Plastic QFP (FPT-100P-M22)
MB96F345DSA PQC-GSE2 ^[1]			No	
MB96F345FWA PQC-GSE2 ^[1]		Yes	Yes	
MB96F345DWA PQC-GSE2 ^[1]			No	
MB96F345FSA PMC-GSE2 ^[1]		No	Yes	100 pin Plastic LQFP (FPT-100P-M20)
MB96F345DSA PMC-GSE2 ^[1]			No	
MB96F345FWA PMC-GSE2 ^[1]		Yes	Yes	
MB96F345DWA PMC-GSE2 ^[1]			No	
MB96F346YSB PQC-GSE2	Flash A (288KB)	No	Yes	100 pin Plastic QFP (FPT-100P-M22)
MB96F346RSB PQC-GSE2			No	
MB96F346YWB PQC-GSE2		Yes	Yes	
MB96F346RWB PQC-GSE2			No	
MB96F346YSB PMC-GSE2		No	Yes	100 pin Plastic LQFP (FPT-100P-M20)
MB96F346RSB PMC-GSE2			No	
MB96F346YWB PMC-GSE2		Yes	Yes	
MB96F346RWB PMC-GSE2			No	

18.1 MCU with CAN Controller

Part number	Flash/ROM	Subclock	Persistent Low Voltage Reset	Package
MB96F347YSB PQC-GSE2	Flash A (416KB)	No	Yes	100 pin Plastic QFP (FPT-100P-M22)
MB96F347RSB PQC-GSE2			No	
MB96F347YWB PQC-GSE2		Yes	Yes	
MB96F347RWB PQC-GSE2			No	
MB96F347YSB PMC-GSE2		No	Yes	100 pin Plastic LQFP (FPT-100P-M20)
MB96F347RSB PMC-GSE2			No	
MB96F347YWB PMC-GSE2		Yes	Yes	
MB96F347RWB PMC-GSE2			No	
MB96F348YSB PQC-GSE2	Flash A (544KB)	No	Yes	100 pin Plastic QFP (FPT-100P-M22)
MB96F348RSB PQC-GSE2			No	
MB96F348YWB PQC-GSE2		Yes	Yes	
MB96F348RWB PQC-GSE2			No	
MB96F348YSB PMC-GSE2		No	Yes	100 pin Plastic LQFP (FPT-100P-M20)
MB96F348RSB PMC-GSE2			No	
MB96F348YWB PMC-GSE2		Yes	Yes	
MB96F348RWB PMC-GSE2			No	
MB96F348TSC PQC-GSE2	Flash A (544KB) Flash B (32KB)	No	Yes	100 pin Plastic QFP (FPT-100P-M22)
MB96F348HSC PQC-GSE2			No	
MB96F348TWC PQC-GSE2		Yes	Yes	
MB96F348HWC PQC-GSE2			No	
MB96F348TSC PMC-GSE2		No	Yes	100 pin Plastic LQFP (FPT-100P-M20)
MB96F348HSC PMC-GSE2			No	
MB96F348TWC PMC-GSE2		Yes	Yes	
MB96F348HWC PMC-GSE2			No	
MB96V300BRB-ES(for evaluation)	Emulated by ext. RAM	Yes	No	416 pin Plastic BGA (BGA-416P-M02)