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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	56MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, LVR, POR, PWM, WDT
Number of I/O	80
Program Memory Size	576KB (576K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f348twbpmc-ge2

1. Product Lineup

Features		MB96V300B	MB96(F)34x
Product type		Evaluation sample	Flash product: MB96F34x Mask ROM product: MB9634x
Product options			
YS		NA	Low voltage reset persistently on / Single clock
RS			Low voltage reset can be disabled / Single clock
YW			Low voltage reset persistently on / Dual clock
RW			Low voltage reset can be disabled / Dual clock
TS			indep. 32KB Flash / Low voltage reset persistently on / Single clock
HS			indep. 32KB Flash / Low voltage reset can be disabled / Single clock
TW			indep. 32KB Flash / Low voltage reset persistently on / Dual clock
HW			indep. 32KB Flash / Low voltage reset can be disabled / Dual clock
FS			64KB Data Flash / Low voltage reset persistently on / Single clock
DS			64KB Data Flash / Low voltage reset can be disabled / Single clock
FW			64KB Data Flash / Low voltage reset persistently on / Dual clock
DW			64KB Data Flash / Low voltage reset can be disabled / Dual clock
AS			No CAN / Low voltage reset can be disabled / Single clock devices
CS			No CAN / indep. 32KB Flash / Low voltage reset can be disabled / Single clock
AW			No CAN / Low voltage reset can be disabled / Dual clock
CW			No CAN / indep. 32KB Flash / Low voltage reset can be disabled / Dual clock
Flash/ROM	RAM		
160KB	8KB	ROM/Flash memory emulation by external RAM, 92KB internal RAM	MB96345Y [1], MB96345R [1]
224KB [Flash A: 160KB, Data Flash A: 64KB]	8KB		MB96F345F [1], MB96F345D [1]
288KB	16KB		MB96F346Y, MB96346Y [1], MB96F346R, MB96346R [1], MB96F346A
416KB	16KB		MB96F347Y, MB96F347R, MB96F347A
544KB	24KB		MB96F348Y, MB96F348R, MB96F348A
576KB [Flash A: 544KB, Flash B: 32KB]	24KB		MB96F348T, MB96F348H, MB96F348C
Package		BGA416	FPT-100P-M20 FPT-100P-M22
DMA		16 channels	6 channels
USART		10 channels	7 channels

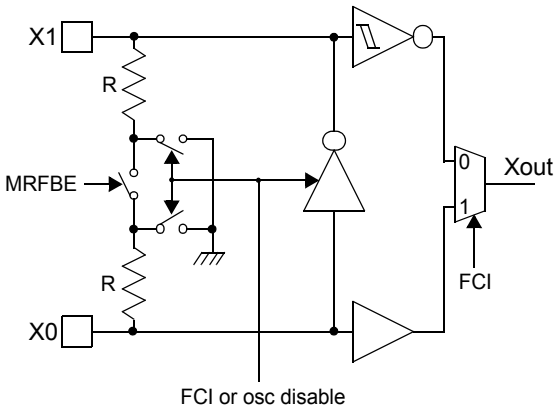
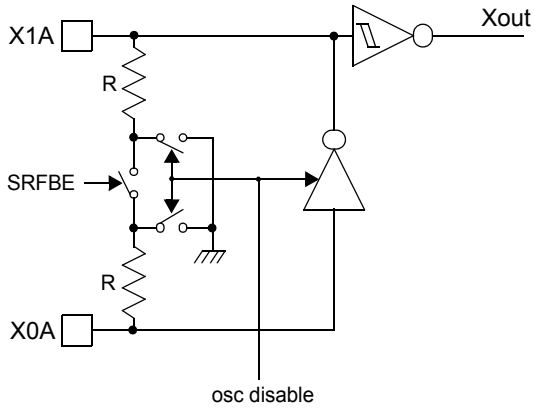
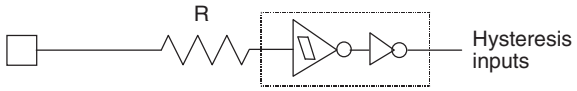
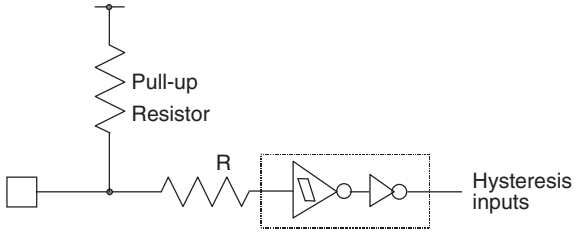
5. Pin Circuit Type

Table 2: Pin circuit types

FPT-100P-M20		FPT-100P-M22	
Pin no.	Circuit type [1]	Pin no.	Circuit type [1]
1-10	H	1-12	H
11,12	B [2]	13, 14	B [2]
11,12	H [3]	13, 14	H [3]
13,14	Supply	15,16	Supply
15	F	17	F
16,17	H	18,19	H
18-21	N	20-23	N
22-29	I	24-31	I
30	Supply	32	Supply
31-32	G	33-34	G
33	Supply	35	Supply
34 to 41	I	36 to 43	I
42	Supply	44	Supply
43 to 48	I	45 to 50	I
49 to 51	C	51 to 53	C
52	E	54	E
53 to 54	I	55 to 56	I
55 to 62	H	57 to 64	H
63, 64	Supply	65, 66	Supply
65 to 87	H	67 to 89	H
88,89	Supply	90, 91	Supply
90, 91	A	92, 93	A
92-100	H	94 to 100	H

[1]: Please refer to “ I/O Circuit Type” for details on the I/O circuit types
[2]: Devices with suffix ”W”
[3]: Devices without suffix ”W”

6. I/O Circuit Type

Type	Circuit	Remarks
A		High-speed oscillation circuit: ■ Programmable between oscillation mode (external crystal or resonator connected to X0/X1 pins) and Fast external Clock Input (FCI) mode (external clock connected to X0 pin) ■ Programmable feedback resistor = approx. 2 * 0.5 MΩ. Feedback resistor is grounded in the center when the oscillator is disabled or in FCI mode
B		Low-speed oscillation circuit: ■ Programmable feedback resistor = approx. 2 * 5 MΩ. Feedback resistor is grounded in the center when the oscillator is disabled
C		■ Mask ROM and EVA device:CMOS Hysteresis input pin ■ Flash device:CMOS input pin
E		■ CMOS Hysteresis input pin ■ Pull-up resistor value: approx. 50 kΩ

Alternative mode CPU address	Flash memory mode address	MB96F346Y MB96F346R MB96F346A Flash size 288kByte	MB96F347Y MB96F347R MB96F347A Flash size 416kByte	
FF:FFFF$_H$ FF:0000$_H$	3F:FFFF$_H$ 3F:0000$_H$	S39 - 64K	S39 - 64K	Flash A
FE:FFFF$_H$ FE:0000$_H$	3E:FFFF$_H$ 3E:0000$_H$	S38 - 64K	S38 - 64K	
FD:FFFF$_H$ FD:0000$_H$	3D:FFFF$_H$ 3D:0000$_H$	S37 - 64K	S37 - 64K	
FC:FFFF$_H$ FC:0000$_H$	3C:FFFF$_H$ 3C:0000$_H$	S36 - 64K	S36 - 64K	
FB:FFFF$_H$ FB:0000$_H$	3B:FFFF$_H$ 3B:0000$_H$	External bus	S35 - 64K	
FA:FFFF$_H$ FA:0000$_H$	3A:FFFF$_H$ 3A:0000$_H$		S34 - 64K	
F9:FFFF$_H$ F9:0000$_H$	39:FFFF$_H$ 39:0000$_H$		External bus	
F8:FFFF$_H$ F8:0000$_H$	38:FFFF$_H$ 38:0000$_H$			
F7:FFFF$_H$ F7:0000$_H$	37:FFFF$_H$ 37:0000$_H$			
F6:FFFF$_H$ F6:0000$_H$	36:FFFF$_H$ 36:0000$_H$			
F5:FFFF$_H$ F5:0000$_H$	35:FFFF$_H$ 35:0000$_H$			
F4:FFFF$_H$ F4:0000$_H$	34:FFFF$_H$ 34:0000$_H$			
F3:FFFF$_H$ F3:0000$_H$	33:FFFF$_H$ 33:0000$_H$			
F2:FFFF$_H$ F2:0000$_H$	32:FFFF$_H$ 32:0000$_H$			
F1:FFFF$_H$ F1:0000$_H$	31:FFFF$_H$ 31:0000$_H$			
F0:FFFF$_H$ F0:0000$_H$	30:FFFF$_H$ 30:0000$_H$			
E0:FFFF$_H$ E0:0000$_H$				
DF:FFFF$_H$ DF:8000$_H$		Reserved	Reserved	
DF:7FFF$_H$ DF:6000$_H$	1F:7FFF$_H$ 1F:6000$_H$	SA3 - 8K	SA3 - 8K	Flash A
DF:5FFF$_H$ DF:4000$_H$	1F:5FFF$_H$ 1F:4000$_H$	SA2 - 8K	SA2 - 8K	
DF:3FFF$_H$ DF:2000$_H$	1F:3FFF$_H$ 1F:2000$_H$	SA1 - 8K	SA1 - 8K	
DF:1FFF$_H$ DF:0000$_H$	1F:1FFF$_H$ 1F:0000$_H$	SA0 - 8K [1]	SA0 - 8K [1]	
DE:FFFF$_H$ DE:0000$_H$		Reserved	Reserved	

[1]: Sector SA0 contains the ROM Configuration Block RCBA at CPU address DF:0000$_H$ - DF:007F$_H$

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000081_H	PPG1 - Timer register			R
000082_H	PPG1 - Period setting register		PCSR1	W
000083_H	PPG1 - Period setting register			W
000084_H	PPG1 - Duty cycle register		PDUT1	W
000085_H	PPG1 - Duty cycle register			W
000086_H	PPG1 - Control status register Low	PCNL1	PCN1	R/W
000087_H	PPG1 - Control status register High	PCNH1		R/W
000088_H	PPG2 - Timer register		PTMR2	R
000089_H	PPG2 - Timer register			R
$00008A_H$	PPG2 - Period setting register		PCSR2	W
$00008B_H$	PPG2 - Period setting register			W
$00008C_H$	PPG2 - Duty cycle register		PDUT2	W
$00008D_H$	PPG2 - Duty cycle register			W
$00008E_H$	PPG2 - Control status register Low	PCNL2	PCN2	R/W
$00008F_H$	PPG2 - Control status register High	PCNH2		R/W
000090_H	PPG3 - Timer register		PTMR3	R
000091_H	PPG3 - Timer register			R
000092_H	PPG3 - Period setting register		PCSR3	W
000093_H	PPG3 - Period setting register			W
000094_H	PPG3 - Duty cycle register		PDUT3	W
000095_H	PPG3 - Duty cycle register			W
000096_H	PPG3 - Control status register Low	PCNL3	PCN3	R/W
000097_H	PPG3 - Control status register High	PCNH3		R/W
000098_H	PPG7-PPG4 - General Control register 1 Low	GCN1L1	GCN11	R/W
000099_H	PPG7-PPG4 - General Control register 1 High	GCN1H1		R/W
$00009A_H$	PPG7-PPG4 - General Control register 2 Low	GCN2L1	GCN21	R/W
$00009B_H$	PPG7-PPG4 - General Control register 2 High	GCN2H1		R/W
$00009C_H$	PPG4 - Timer register		PTMR4	R
$00009D_H$	PPG4 - Timer register			R
$00009E_H$	PPG4 - Period setting register		PCSR4	W
$00009F_H$	PPG4 - Period setting register			W
$0000A0_H$	PPG4 - Duty cycle register		PDUT4	W

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$0003B9_H$	Memory Patch function - Patch address 0 middle	PFAM0		R/W
$0003BA_H$	Memory Patch function - Patch address 0 high	PFAH0		R/W
$0003BB_H$	Memory Patch function - Patch address 1 low	PFAL1		R/W
$0003BC_H$	Memory Patch function - Patch address 1 middle	PFAM1		R/W
$0003BD_H$	Memory Patch function - Patch address 1 high	PFAH1		R/W
$0003BE_H$	Memory Patch function - Patch address 2 low	PFAL2		R/W
$0003BF_H$	Memory Patch function - Patch address 2 middle	PFAM2		R/W
$0003C0_H$	Memory Patch function - Patch address 2 high	PFAH2		R/W
$0003C1_H$	Memory Patch function - Patch address 3 low	PFAL3		R/W
$0003C2_H$	Memory Patch function - Patch address 3 middle	PFAM3		R/W
$0003C3_H$	Memory Patch function - Patch address 3 high	PFAH3		R/W
$0003C4_H$	Memory Patch function - Patch address 4 low	PFAL4		R/W
$0003C5_H$	Memory Patch function - Patch address 4 middle	PFAM4		R/W
$0003C6_H$	Memory Patch function - Patch address 4 high	PFAH4		R/W
$0003C7_H$	Memory Patch function - Patch address 5 low	PFAL5		R/W
$0003C8_H$	Memory Patch function - Patch address 5 middle	PFAM5		R/W
$0003C9_H$	Memory Patch function - Patch address 5 high	PFAH5		R/W
$0003CA_H$	Memory Patch function - Patch address 6 low	PFAL6		R/W
$0003CB_H$	Memory Patch function - Patch address 6 middle	PFAM6		R/W
$0003CC_H$	Memory Patch function - Patch address 6 high	PFAH6		R/W
$0003CD_H$	Memory Patch function - Patch address 7 low	PFAL7		R/W
$0003CE_H$	Memory Patch function - Patch address 7 middle	PFAM7		R/W
$0003CF_H$	Memory Patch function - Patch address 7 high	PFAH7		R/W
$0003D0_H$	Memory Patch function - Patch data 0 Low	PFDL0	PFD0	R/W
$0003D1_H$	Memory Patch function - Patch data 0 High	PFDH0		R/W
$0003D2_H$	Memory Patch function - Patch data 1 Low	PFDL1	PFD1	R/W
$0003D3_H$	Memory Patch function - Patch data 1 High	PFDH1		R/W
$0003D4_H$	Memory Patch function - Patch data 2 Low	PFDL2	PFD2	R/W
$0003D5_H$	Memory Patch function - Patch data 2 High	PFDH2		R/W
$0003D6_H$	Memory Patch function - Patch data 3 Low	PFDL3	PFD3	R/W
$0003D7_H$	Memory Patch function - Patch data 3 High	PFDH3		R/W
$0003D8_H$	Memory Patch function - Patch data 4 Low	PFDL4	PFD4	R/W

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$00043B_H$-000443_H	Reserved			-
000444_H	I/O Port P00 - Port Input Enable Register	PIER00		R/W
000445_H	I/O Port P01 - Port Input Enable Register	PIER01		R/W
000446_H	I/O Port P02 - Port Input Enable Register	PIER02		R/W
000447_H	I/O Port P03 - Port Input Enable Register	PIER03		R/W
000448_H	I/O Port P04 - Port Input Enable Register	PIER04		R/W
000449_H	I/O Port P05 - Port Input Enable Register	PIER05		R/W
$00044A_H$	I/O Port P06 - Port Input Enable Register	PIER06		R/W
$00044B_H$	I/O Port P07 - Port Input Enable Register	PIER07		R/W
$00044C_H$	I/O Port P08 - Port Input Enable Register	PIER08		R/W
$00044D_H$	I/O Port P09 - Port Input Enable Register	PIER09		R/W
$00044E_H$	I/O Port P10 - Port Input Enable Register	PIER10		R/W
$00044F_H$-000457_H	Reserved			-
000458_H	I/O Port P00 - Port Input Level Register	PILR00		R/W
000459_H	I/O Port P01 - Port Input Level Register	PILR01		R/W
$00045A_H$	I/O Port P02 - Port Input Level Register	PILR02		R/W
$00045B_H$	I/O Port P03 - Port Input Level Register	PILR03		R/W
$00045C_H$	I/O Port P04 - Port Input Level Register	PILR04		R/W
$00045D_H$	I/O Port P05 - Port Input Level Register	PILR05		R/W
$00045E_H$	I/O Port P06 - Port Input Level Register	PILR06		R/W
$00045F_H$	I/O Port P07 - Port Input Level Register	PILR07		R/W
000460_H	I/O Port P08 - Port Input Level Register	PILR08		R/W
000461_H	I/O Port P09 - Port Input Level Register	PILR09		R/W
000462_H	I/O Port P10 - Port Input Level Register	PILR10		R/W
000463_H-$00046B_H$	Reserved			-
$00046C_H$	I/O Port P00 - Extended Port Input Level Register	EPILR00		R/W
$00046D_H$	I/O Port P01 - Extended Port Input Level Register	EPILR01		R/W
$00046E_H$	I/O Port P02 - Extended Port Input Level Register	EPILR02		R/W
$00046F_H$	I/O Port P03 - Extended Port Input Level Register	EPILR03		R/W
000470_H	I/O Port P04 - Extended Port Input Level Register	EPILR04		R/W
000471_H	I/O Port P05 - Extended Port Input Level Register	EPILR05		R/W
000472_H	I/O Port P06 - Extended Port Input Level Register	EPILR06		R/W

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$0005AD_H$	PPG14 - Timer register			R
$0005AE_H$	PPG14 - Period setting register		PCSR14	W
$0005AF_H$	PPG14 - Period setting register			W
$0005B0_H$	PPG14 - Duty cycle register		PDUT14	W
$0005B1_H$	PPG14 - Duty cycle register			W
$0005B2_H$	PPG14 - Control status register Low	PCNL14	PCN14	R/W
$0005B3_H$	PPG14 - Control status register High	PCNH14		R/W
$0005B4_H$	PPG15 - Timer register		PTMR15	R
$0005B5_H$	PPG15 - Timer register			R
$0005B6_H$	PPG15 - Period setting register		PCSR15	W
$0005B7_H$	PPG15 - Period setting register			W
$0005B8_H$	PPG15 - Duty cycle register		PDUT15	W
$0005B9_H$	PPG15 - Duty cycle register			W
$0005BA_H$	PPG15 - Control status register Low	PCNL15	PCN15	R/W
$0005BB_H$	PPG15 - Control status register High	PCNH15		R/W
$0005BC_H$-$00065F_H$	Reserved			-
000660_H	Peripheral Resource Relocation Register 10	PRRR10		R/W
000661_H	Peripheral Resource Relocation Register 11	PRRR11		R/W
000662_H	Peripheral Resource Relocation Register 12	PRRR12		R/W
000663_H	Peripheral Resource Relocation Register 13	PRRR13		W
000664_H-$0006DF_H$	Reserved			-
$0006E0_H$	External Bus - Area configuration register 0 Low	EACL0	EAC0	R/W
$0006E1_H$	External Bus - Area configuration register 0 High	EACH0		R/W
$0006E2_H$	External Bus - Area configuration register 1 Low	EACL1	EAC1	R/W
$0006E3_H$	External Bus - Area configuration register 1 High	EACH1		R/W
$0006E4_H$	External Bus - Area configuration register 2 Low	EACL2	EAC2	R/W
$0006E5_H$	External Bus - Area configuration register 2 High	EACH2		R/W
$0006E6_H$	External Bus - Area configuration register 3 Low	EACL3	EAC3	R/W
$0006E7_H$	External Bus - Area configuration register 3 High	EACH3		R/W
$0006E8_H$	External Bus - Area configuration register 4 Low	EACL4	EAC4	R/W
$0006E9_H$	External Bus - Area configuration register 4 High	EACH4		R/W
$0006EA_H$	External Bus - Area configuration register 5 Low	EACL5	EAC5	R/W

Table 4: I/O map MB96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000715_H	CAN0 - IF1 Mask 1 Register High	IF1MSK1H0		R/W
000716_H	CAN0 - IF1 Mask 2 Register Low	IF1MSK2L0	IF1MSK20	R/W
000717_H	CAN0 - IF1 Mask 2 Register High	IF1MSK2H0		R/W
000718_H	CAN0 - IF1 Arbitration 1 Register Low	IF1ARB1L0	IF1ARB10	R/W
000719_H	CAN0 - IF1 Arbitration 1 Register High	IF1ARB1H0		R/W
$00071A_H$	CAN0 - IF1 Arbitration 2 Register Low	IF1ARB2L0	IF1ARB20	R/W
$00071B_H$	CAN0 - IF1 Arbitration 2 Register High	IF1ARB2H0		R/W
$00071C_H$	CAN0 - IF1 Message Control Register Low	IF1MCTRL0	IF1MCTR0	R/W
$00071D_H$	CAN0 - IF1 Message Control Register High	IF1MCTRH0		R/W
$00071E_H$	CAN0 - IF1 Data A1 Low	IF1DTA1L0	IF1DTA10	R/W
$00071F_H$	CAN0 - IF1 Data A1 High	IF1DTA1H0		R/W
000720_H	CAN0 - IF1 Data A2 Low	IF1DTA2L0	IF1DTA20	R/W
000721_H	CAN0 - IF1 Data A2 High	IF1DTA2H0		R/W
000722_H	CAN0 - IF1 Data B1 Low	IF1DTB1L0	IF1DTB10	R/W
000723_H	CAN0 - IF1 Data B1 High	IF1DTB1H0		R/W
000724_H	CAN0 - IF1 Data B2 Low	IF1DTB2L0	IF1DTB20	R/W
000725_H	CAN0 - IF1 Data B2 High	IF1DTB2H0		R/W
000726_H-$00073F_H$	Reserved			-
000740_H	CAN0 - IF2 Command request register Low	IF2CREQL0	IF2CREQ0	R/W
000741_H	CAN0 - IF2 Command request register High	IF2CREQH0		R/W
000742_H	CAN0 - IF2 Command Mask register Low	IF2CMSKL0	IF2CMSK0	R/W
000743_H	CAN0 - IF2 Command Mask register High (reserved)	IF2CMSKH0		R
000744_H	CAN0 - IF2 Mask 1 Register Low	IF2MSK1L0	IF2MSK10	R/W
000745_H	CAN0 - IF2 Mask 1 Register High	IF2MSK1H0		R/W
000746_H	CAN0 - IF2 Mask 2 Register Low	IF2MSK2L0	IF2MSK20	R/W
000747_H	CAN0 - IF2 Mask 2 Register High	IF2MSK2H0		R/W
000748_H	CAN0 - IF2 Arbitration 1 Register Low	IF2ARB1L0	IF2ARB10	R/W
000749_H	CAN0 - IF2 Arbitration 1 Register High	IF2ARB1H0		R/W
$00074A_H$	CAN0 - IF2 Arbitration 2 Register Low	IF2ARB2L0	IF2ARB20	R/W
$00074B_H$	CAN0 - IF2 Arbitration 2 Register High	IF2ARB2H0		R/W
$00074C_H$	CAN0 - IF2 Message Control Register Low	IF2MCTRL0	IF2MCTR0	R/W
$00074D_H$	CAN0 - IF2 Message Control Register High	IF2MCTRH0		R/W

13. Handling Devices

Special care is required for the following when handling the device:

- Latch-up prevention
- Unused pins handling
- External clock usage
- Unused sub clock signal
- Notes on PLL clock mode operation
- Power supply pins (V_{CC}/V_{SS})
- Crystal oscillator circuit
- Turn on sequence of power supply to A/D converter and analog inputs
- Pin handling when not using the A/D converter
- Notes on energization
- Stabilization of power supply voltage
- Serial communication
- Handling of Data Flash

13.1 Latch-up prevention

CMOS IC chips may suffer latch-up under the following conditions:

- A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V_{CC} pins and V_{SS} pins.
- The AV_{CC} power supply is applied before the V_{CC} voltage.

Latch-up may increase the power supply current dramatically, causing thermal damages to the device.

For the same reason, extra care is required to not let the analog power-supply voltage (AV_{CC}, AVRH) exceed the digital power-supply voltage.

13.2 Unused pins handling

Unused input pins can be left open when the input is disabled (corresponding bit of Port Input Enable register PIER = 0).

Leaving unused input pins open when the input is enabled may result in misbehavior and possible permanent damage of the device. They must therefore be pulled up or pulled down through resistors. To prevent latch-up, those resistors should be more than 2 kΩ.

Unused bidirectional pins can be set either to the output state and be then left open, or to the input state with either input disabled or external pull-up/pull-down resistor as described above.

13.3 External clock usage

The permitted frequency range of an external clock depends on the oscillator type and configuration. See AC Characteristics for detailed modes and frequency limits. Single and opposite phase external clocks must be connected as follows:

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Permitted Power dissipation (Mask ROM devices) [4]	P_D	-	350	mW	T_A=105°C
		-	360	mW	T_A=125°C [6]
Operating ambient temperature	T_A	0	+70	°C	MB96V300B
		-40	+105		
		-40	+125		[6]
Storage temperature	T_{STG}	-55	+150	°C	

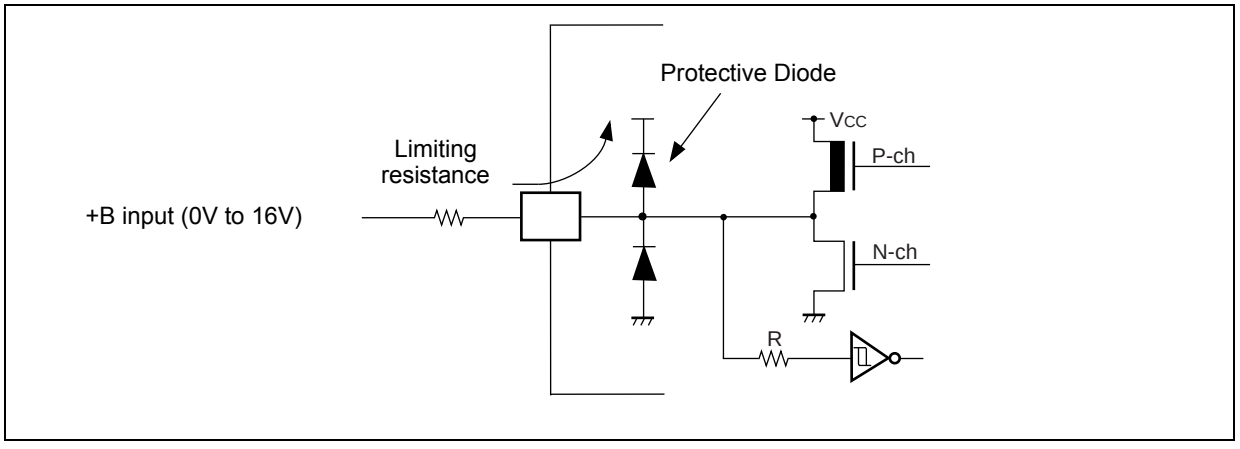
[1]: AV_{CC} and V_{CC} must be set to the same voltage. It is required that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} neither when the power is switched on.

[2]: V_I and V_O should not exceed V_{CC} + 0.3 V. V_I should also not exceed the specified ratings. However if the maximum current to/from a input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating. Input/output voltages of standard ports depend on V_{CC}.

[3]:

- Applicable to all general purpose I/O pins (Pnn_m)
- Use within recommended operating conditions.
- Use at DC voltage (current)
- The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the Power reset (except devices with persistent low voltage reset in internal vector mode).

Sample recommended circuits:

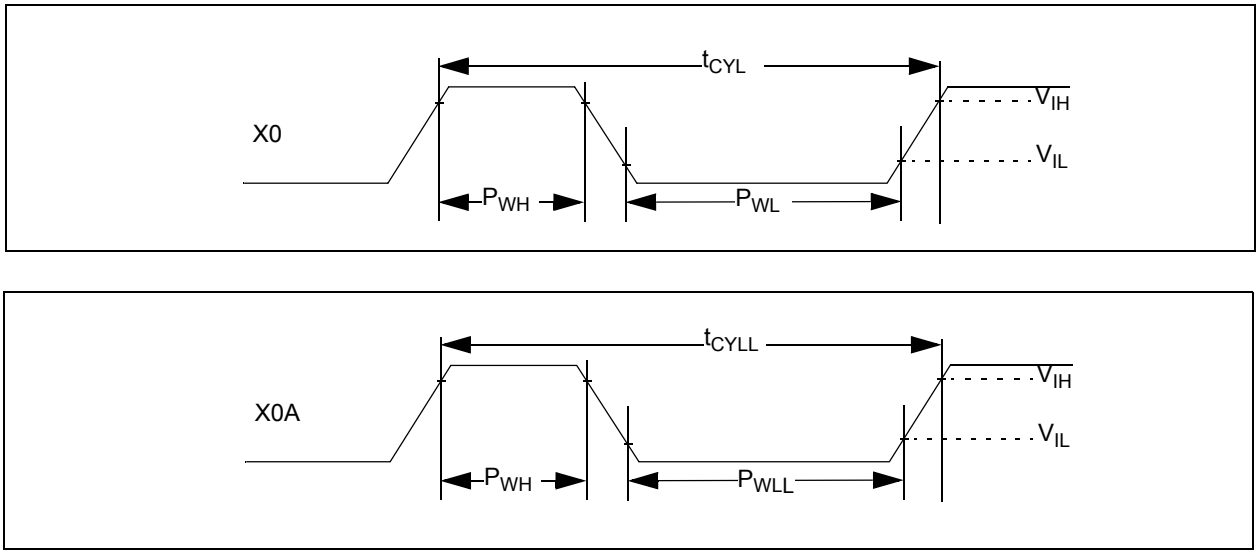


14.4 AC Characteristics

14.4.1 Source Clock timing

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

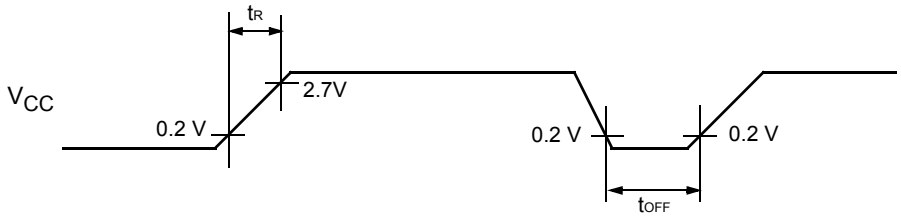
Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_C	X0, X1	3	-	16	MHz	When using a crystal oscillator, PLL off
			0	-	16	MHz	When using an opposite phase external clock, PLL off
			3.5	-	16	MHz	When using a crystal oscillator or opposite phase external clock, PLL on
Clock frequency	f_{FCI}	X0	0	-	56	MHz	When using a single phase external clock in “Fast Clock Input mode” (not available in MB96F34xY/R/AxA), PLL off
			3.5	-	56	MHz	When using a single phase external clock in “Fast Clock Input mode” (not available in MB96F34xY/R/AxA), PLL on
Clock frequency	f_{CL}	X0A, X1A	32	32.768	100	kHz	When using an oscillation circuit
			0	-	100	kHz	When using an opposite phase external clock
		X0A	0	-	50	kHz	When using a single phase external clock
Clock frequency	f_{CR}	-	50	100	200	kHz	When using slow frequency of RC oscillator
			1	2	4	MHz	When using fast frequency of RC oscillator
PLL Clock frequency	f_{CLKVCO}	-	64	-	200	MHz	Permitted VCO output frequency of PLL (CLKVCO)
PLL Phase Jitter	T_{PSKEW}	-	-	-	± 5	ns	For CLKMC (PLL input clock) ≥ 4MHz
Input clock pulse width	P_{WH}, P_{WL}	X0,X1	8	-	-	ns	Duty ratio is about 30% to 70%
Input clock pulse width	P_{WHL}, P_{WLL}	X0A,X1A	5	-	-	µs	



14.4.4 Power On Reset timing

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Power on rise time	t_R	Vcc	0.05	-	30	ms	
Power off time	t_{OFF}	Vcc	1	-	-	ms	



If the power supply is changed too rapidly, a power-on reset may occur.
We recommend a smooth startup by restraining voltages when changing the power supply voltage during operation, as shown in the figure below.

14.4.12 USART timing

WARNING: The values given below are for an I/O driving strength IO_{drive} = 5mA. If IO_{drive} is 2mA, all the maximum output timing described in the different tables must then be increased by 10ns.

(T_A = -40°C to 125°C, V_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Condition	V_{CC} = AV_{CC}= 4.5V to 5.5V		V_{CC} = AV_{CC}= 3.0V to 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYCI}	SCKn	Internal Shift Clock Mode	4 t_{CLKP1}	-	4 t_{CLKP1}	-	ns
SCK ↓→ SOT delay time	t_{SLOVI}	SCKn, SOTn		-20	+20	-30	+30	ns
SOT → SCK ↑ delay time	t_{OVSHI}	SCKn, SOTn		N*t_{CLKP1} - 20 [1]	-	N*t_{CLKP1} - 30 [1]	-	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCKn, SINn		t_{CLKP1} + 45	-	t_{CLKP1} + 55	-	ns
SCK ↑→ Valid SIN hold time	t_{SHIXI}	SCKn, SINn		0	-	0	-	ns
Serial clock “L” pulse width	t_{SLSHE}	SCKn	External Shift Clock Mode	t_{CLKP1} + 10	-	t_{CLKP1} + 10	-	ns
Serial clock “H” pulse width	t_{SHSLE}	SCKn		t_{CLKP1} + 10	-	t_{CLKP1} + 10	-	ns
SCK ↓→ SOT delay time	t_{SLOVE}	SCKn, SOTn		-	2 t_{CLKP1} + 45	-	2 t_{CLKP1} + 55	ns
Valid SIN → SCK ↑	t_{IVSHE}	SCKn, SINn		t_{CLKP1}/2 + 10	-	t_{CLKP1}/2 + 10	-	ns
SCK ↑→ Valid SIN hold time	t_{SHIXE}	SCKn, SINn		t_{CLKP1} + 10	-	t_{CLKP1} + 10	-	ns
SCK fall time	t_{FE}	SCKn		-	20	-	20	ns
SCK rise time	t_{RE}	SCKn		-	20	-	20	ns

Notes:

- AC characteristic in CLK synchronized mode.
- C_L is the load capacity value of pins when testing.
- Depending on the used machine clock frequency, the maximum possible baud rate can be limited by some parameters. These parameters are shown in “MB96300 Super series HARDWARE MANUAL”.
- t_{CLKP1} is the cycle time of the peripheral clock 1 (CLKP1), Unit : ns

[1]: Parameter N depends on t_{SCYCI} and can be calculated as follows:

- if t_{SCYCI} = 2*k*t_{CLKP1}, then N = k, where k is an integer > 2
- if t_{SCYCI} = (2*k+1)*t_{CLKP1}, then N = k+1, where k is an integer > 1

Examples:

t_{SCYCI}	N
4*t_{CLKP1}	2
5*t_{CLKP1},	3
7*t_{CLKP1},	4
...	...

14.4.13 I²C Timing

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V,V_{SS} = AV_{SS} =0V)

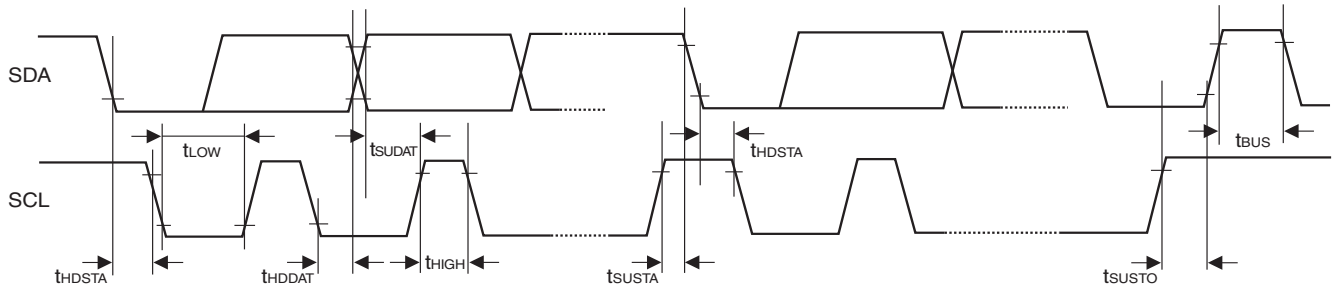
Parameter	Symbol	Condition	Standard-mode		Fast-mode[4]		Unit
			Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	R = 1.7 kΩ, C = 50 pF[1]	0	100	0	400	kHz
Hold time (repeated) START condition SDA↓→SCL¬	t_{HDSTA}		4.0	-	0.6	-	µs
"L" width of the SCL clock	t_{LOW}		4.7	-	1.3	-	µs
"H" width of the SCL clock	t_{HIGH}		4.0	-	0.6	-	µs
Set-up time for a repeated START condition SCL↓→SDA↑	t_{SUSTA}		4.7	-	0.6	-	µs
Data hold timeSCL↑→SDA↑↓	t_{HDDAT}		0	3.45[2]	0	0.9[3]	µs
Data set-up timeSDA↑↓→SCL↑	t_{SUDAT}		250	-	100	-	ns
Set-up time for STOP conditionSCL↑→SDA↑	t_{SUSTO}		4.0	-	0.6	-	µs
Bus free time between a STOP and START condition	t_{BUS}		4.7	-	1.3	-	µs

[1] : R,C: Pull-up resistor and load capacitor of the SCL and SDA lines.

[2]: The maximum t_{HDDAT} have only to be met if the device does not stretch the "L" width (t_{LOW}) of the SCL signal.

[3] : A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement t_{SUDAT}≥ 250 ns must then be met.

[4] : For use at over 100 kHz, set the peripheral clock 1 to at least 6 MHz.



14.7 Low Voltage Detector Characteristics

(T_A = -40 °C to +125 °C, V_{cc} = AV_{cc} = 3.0V - 5.5V, V_{ss} = AV_{ss} = 0V)

Parameter	Symbol	Value [1]		Value [2]		Unit	Remarks
		Min	Max	Min	Max		
Stabilization time	$T_{LVDSTAB}$	-	75	-	110	µs	After power-up or change of detection level
Level 0	V_{DL0}	2.7	2.9	2.65	2.95	V	CILCR:LVL[3:0]="0000"
Level 1	V_{DL1}	2.9	3.1	2.85	3.2	V	CILCR:LVL[3:0]="0001"
Level 2	V_{DL2}	3.1	3.3	3.05	3.4	V	CILCR:LVL[3:0]="0010"
Level 3	V_{DL3}	3.5	3.75	3.45	3.85	V	CILCR:LVL[3:0]="0011"
Level 4	V_{DL4}	3.6	3.85	3.55	3.95	V	CILCR:LVL[3:0]="0100"
Level 5	V_{DL5}	3.7	3.95	3.65	4.1	V	CILCR:LVL[3:0]="0101"
Level 6	V_{DL6}	3.8	4.05	3.75	4.2	V	CILCR:LVL[3:0]="0110"
Level 7	V_{DL7}	3.9	4.15	3.85	4.3	V	CILCR:LVL[3:0]="0111"
Level 8	V_{DL8}	4.0	4.25	3.95	4.4	V	CILCR:LVL[3:0]="1000"
Level 9	V_{DL9}	4.1	4.35	4.05	4.5	V	CILCR:LVL[3:0]="1001"
Level 10	V_{DL10}	not used		not used			
Level 11	V_{DL11}	not used		not used			
Level 12	V_{DL12}	not used		not used			
Level 13	V_{DL13}	not used		not used			
Level 14	V_{DL14}	not used		not used			
Level 15	V_{DL15}	not used		not used			

[1]: valid for all devices except devices listed under "[2]"

[2]: valid for: MB96F345

CILCR:LVL[3:0] are the low voltage detector level select bits of the CILCR register.

Levels 10 to 15 are not used in this device.

For correct detection, the slope of the voltage level must satisfy $\left|\frac{dV}{dt}\right| \leq 0.004\frac{V}{\mu s}$.

Faster variations are regarded as noise and may not be detected.

The functional operation of the MCU is guaranteed down to the minimum low voltage detection level of Vcc = 2.7V. The electrical characteristics however are only valid in the specified range (usually down to 3.0V).

14.7.1 Low Voltage Detector Operation

In the following figure, the occurrence of a low voltage condition is illustrated. For a detailed description of the reset and startup behavior, please refer to the corresponding hardware manual chapter.

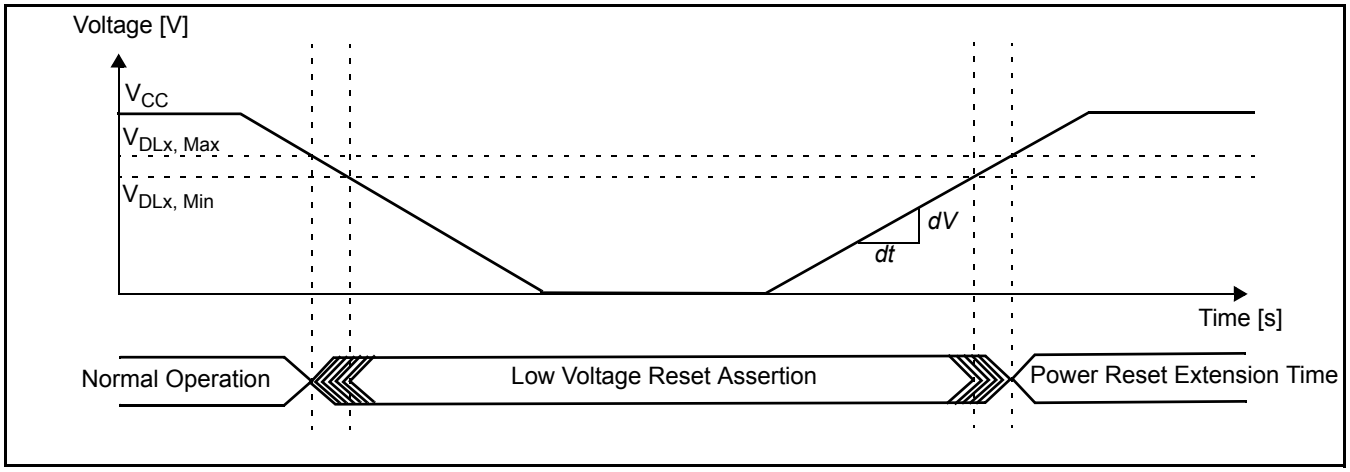


Table 6: Used settings

Mode	Selected Source Clock	Clock/Regulator Settings
Run mode	PLL	CLKS1 = CLKS2 = CLKB = CLKP1 = 56 MHz CLKP2 = 28 MHz Regulator in High Power Mode Core Voltage = 1.9 V
	Main osc.	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 4 MHz Regulator in High Power Mode Core Voltage = 1.8 V
	RC clock fast	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 2 MHz Regulator in High Power Mode Core Voltage = 1.8 V
	RC clock slow	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 100 kHz Regulator in High Power Mode Core Voltage = 1.8 V
	Sub osc.	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 32 kHz Regulator in Low Power Mode A Core Voltage = 1.8 V
Sleep mode	PLL	CLKS1 = CLKS2 = CLKP1 = 56 MHz CLKP2 = 28 MHz (CLKB is stopped in this mode) Regulator in High Power Mode Core Voltage = 1.9 V
	Main osc.	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 4 MHz (CLKB is stopped in this mode) Regulator in High Power Mode Core Voltage = 1.8 V
	RC clock fast	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 2 MHz (CLKB is stopped in this mode) Regulator in High Power Mode Core Voltage = 1.8 V
	RC clock slow	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 100 kHz (CLKB is stopped in this mode) Regulator in High Power Mode Core Voltage = 1.8 V
	Sub osc.	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 32 kHz (CLKB is stopped in this mode) Regulator in Low Power Mode A Core Voltage = 1.8 V

Table 6: Used settings

Mode	Selected Source Clock	Clock/Regulator Settings
Timer mode	PLL	CLKMC = 4 MHz, CLKPLL = 56 MHz (System clocks are stopped in this mode) Regulator in High Power Mode, Core Voltage = 1.9 V
	Main osc.	CLKMC = 4 MHz (System clocks are stopped in this mode) Regulator in High Power Mode, Core Voltage = 1.8 V
	RC clock fast	CLKRC = 2 MHz (System clocks are stopped in this mode) Regulator in High Power Mode, Core Voltage = 1.8 V
	RC clock slow	CLKRC = 100 kHz (System clocks are stopped in this mode) Regulator in High Power Mode, Core Voltage = 1.8 V
	Sub osc.	CLKSC = 100 kHz (System clocks are stopped in this mode) Regulator in Low Power Mode A, Core Voltage = 1.8 V
Stop mode	stopped	(All clocks are stopped in this mode) Regulator in Low Power Mode B, Core Voltage = 1.8 V

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