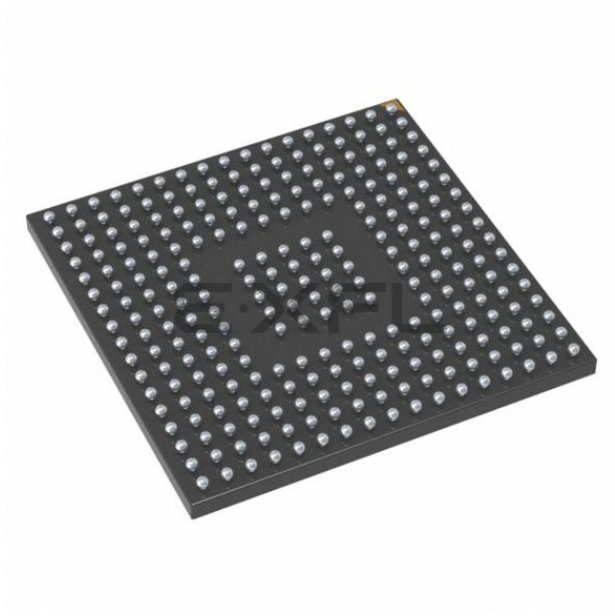

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	216MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	140
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	201-UFBGA
Supplier Device Package	176+25UFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f732iek6

2.2 STM32F733xx versus STM32F732xx LQFP144/LQFP176 packages:

Figure 3. Compatible board design for LQFP144 package

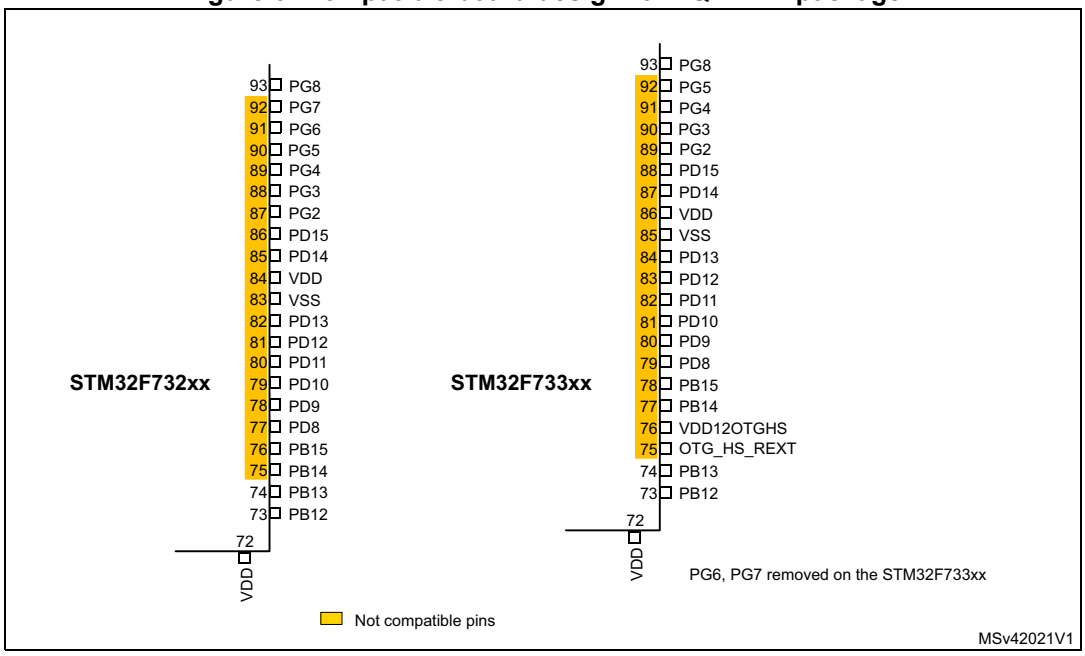


Figure 4. Compatible board design for LQFP176 package

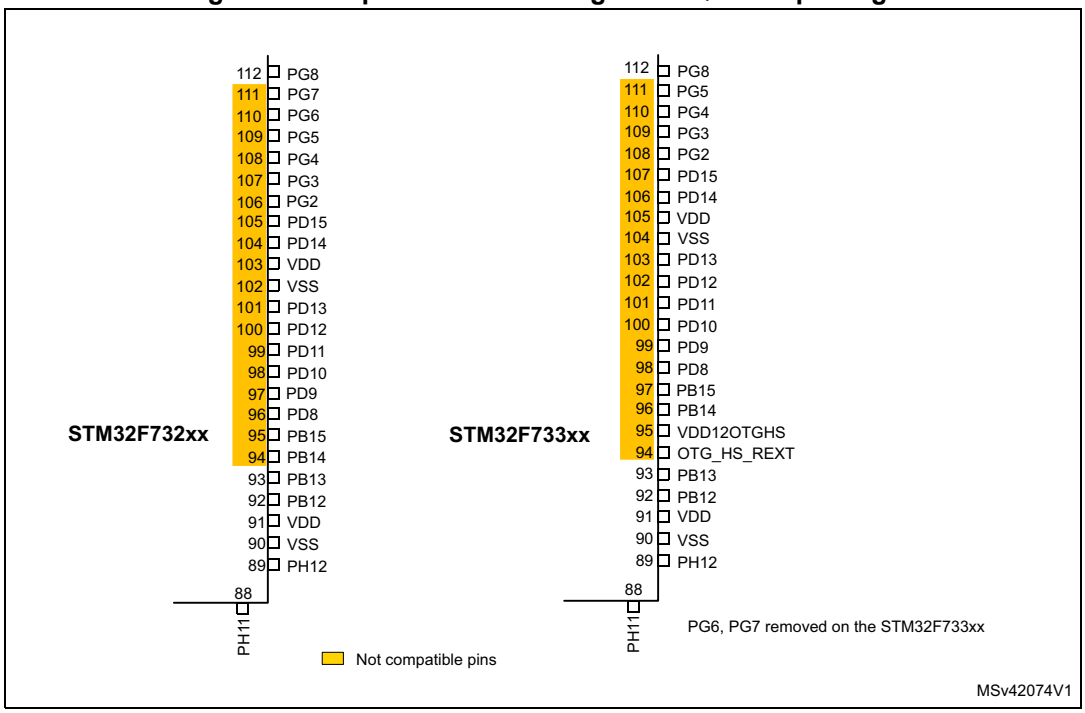
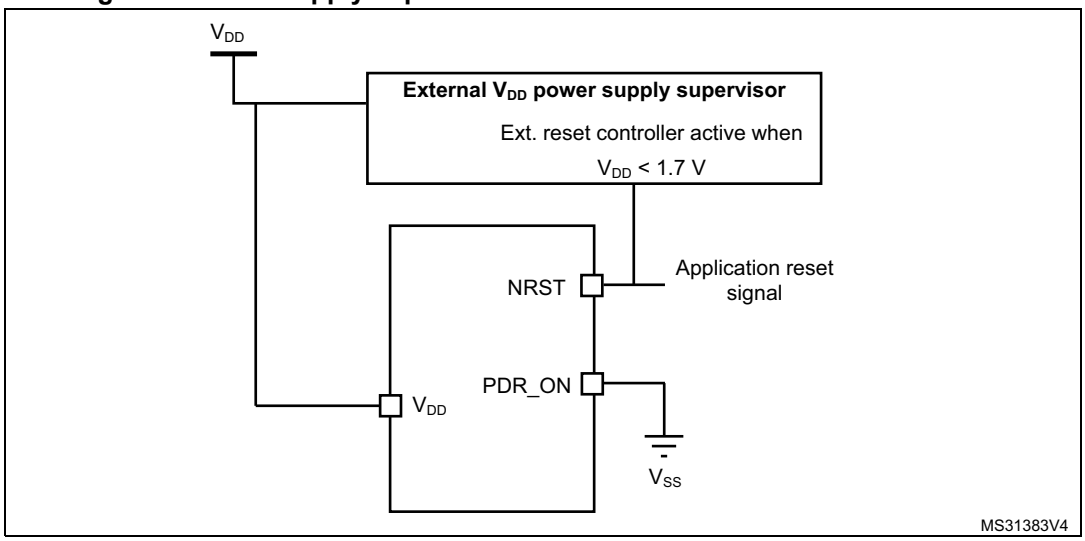


Figure 5 shows the general block diagram of the device family.

Figure 9. Power supply supervisor interconnection with internal reset OFF



The V_{DD} specified threshold, below which the device must be maintained under reset, is 1.7 V (see *Figure 10*).

A comprehensive set of power-saving mode allows to design low-power applications.

When the internal reset is OFF, the following integrated features are no more supported:

- The integrated power-on reset (POR) / power-down reset (PDR) circuitry is disabled
- The brownout reset (BOR) circuitry must be disabled
- The embedded programmable voltage detector (PVD) is disabled
- V_{BAT} functionality is no more available and V_{BAT} pin should be connected to V_{DD}.

All packages, except for the LQFP100, allow to disable the internal reset through the PDR_ON signal when connected to V_{SS}.

Figure 10. PDR_ON control with internal reset OFF

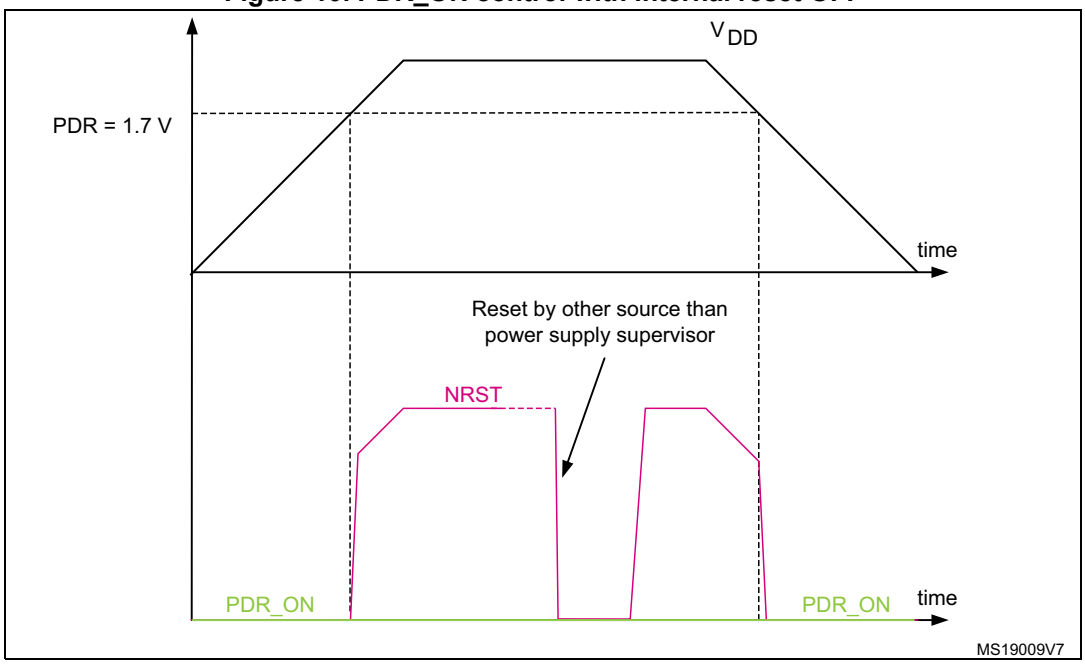
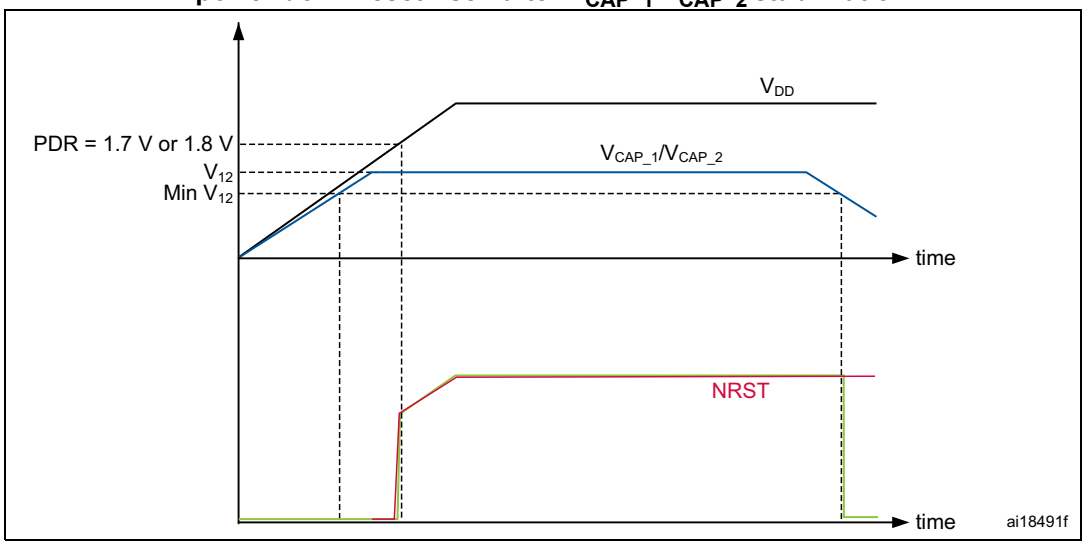
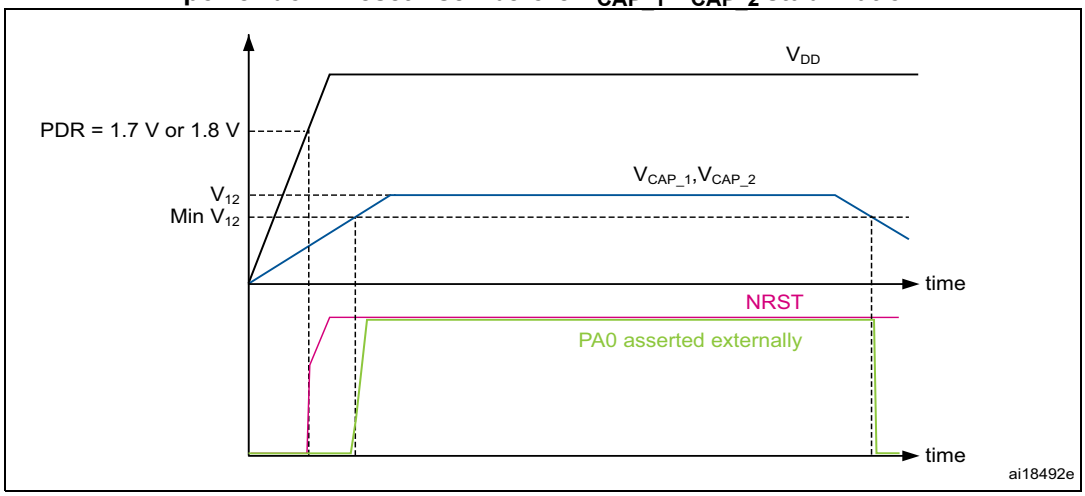


Figure 12. Startup in regulator OFF: slow V_{DD} slope - power-down reset risen after V_{CAP_1}/V_{CAP_2} stabilization



1. This figure is valid whatever the internal reset mode (ON or OFF).

Figure 13. Startup in regulator OFF mode: fast V_{DD} slope - power-down reset risen before V_{CAP_1}/V_{CAP_2} stabilization



1. This figure is valid whatever the internal reset mode (ON or OFF).

3.20.4 Low-power timer (LPTIM1)

The low-power timer has an independent clock and is running also in Stop mode if it is clocked by LSE, LSI or an external clock. It is able to wakeup the devices from Stop mode.

This low-power timer supports the following features:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous / one-shot mode
- Selectable software / hardware input trigger
- Selectable clock source:
- Internal clock source: LSE, LSI, HSI or APB clock
- External clock source over LPTIM input (working even with no internal clock source running, used by the Pulse Counter Application)
- Programmable digital glitch filter
- Encoder mode

3.20.5 Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes.

3.20.6 Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.20.7 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard downcounter. It features:

- A 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

- Internal FS OTG PHY support
- **For the STM32F732xx devices:** External HS or HS OTG operation supporting ULPI in SDR mode. The OTG PHY is connected to the microcontroller ULPI port through 12 signals. It can be clocked using the 60 MHz output.
- **For the STM32F733xx devices:** Internal HS OTG PHY support.
- Internal USB DMA
- HNP/SNP/IP inside (no need for any external resistor)
- For OTG/Host modes, a power switch is needed in case bus-powered devices are connected

Universal Serial Bus controller on-the-go High-Speed PHY controller (USBPHYC) only on STM32F733xx devices.

The USB HS PHY controller:

- Sets the PHYPLL1/2 values for the PHY HS
- Sets the other controls on the PHY HS
- Controls and monitors the USB PHY's LDO

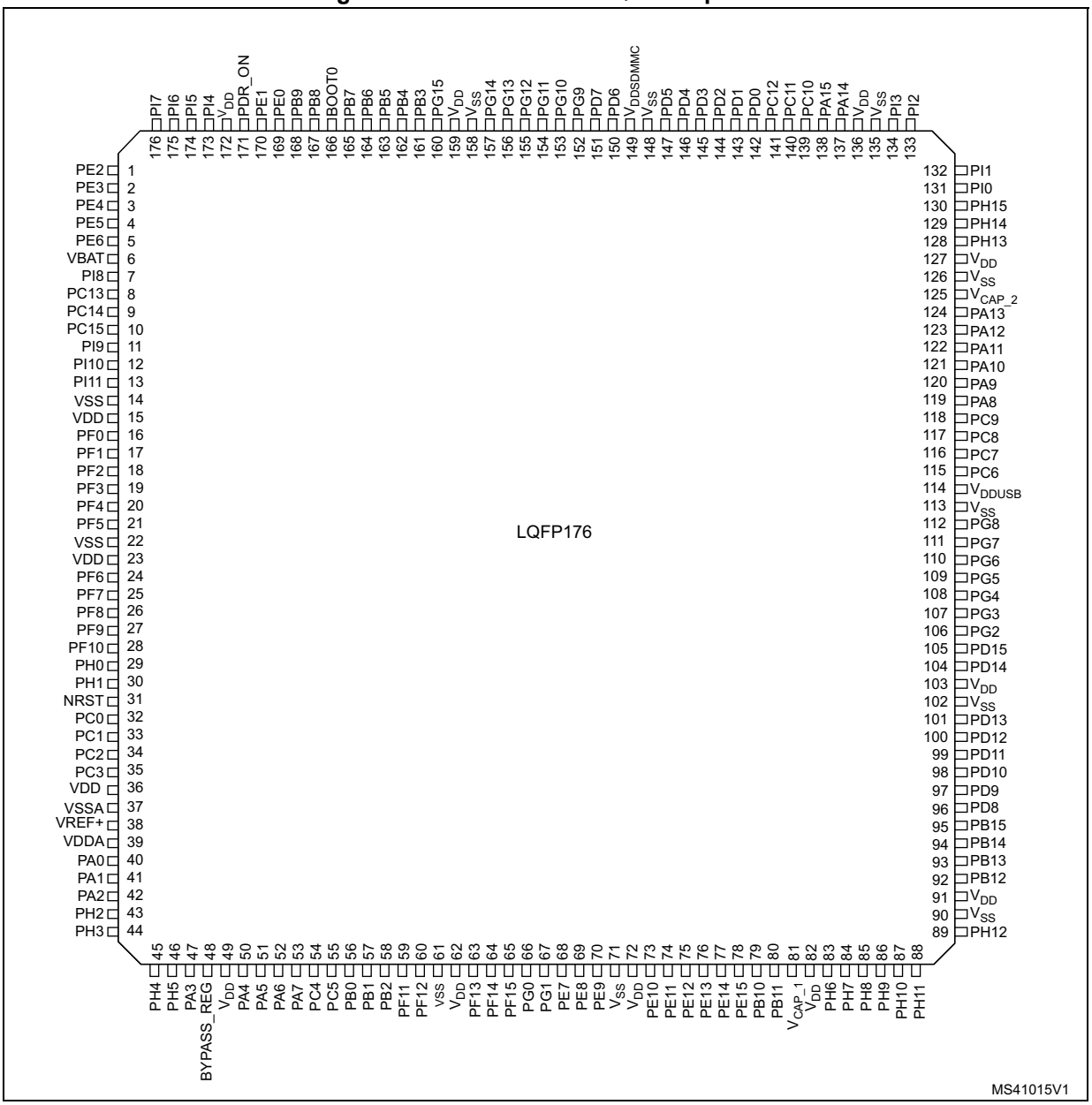
3.31 Random number generator (RNG)

All the devices embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit.

3.32 Advanced encryption standard hardware accelerator (AES)

The devices embed an AES hardware accelerator which can be used to both encipher and decipher data using AES algorithm.

Figure 20. STM32F732xx LQFP176 pinout



1. The above figure shows the package top view.

Table 10. STM32F732xx and STM32F733xx pin and ball definition (continued)

Pin Number										Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F732xx					STM32F733xx										
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
-	-	89	K14	108	-	K14	J10	91	110	PG4	I/O	FT	-	FMC_A14/FMC_BA0, EVENTOUT	-
-	-	90	K13	109	-	K13	H12	92	111	PG5	I/O	FT	-	FMC_A15/FMC_BA1, EVENTOUT	-
-	-	91	J15	110	-	-	-	-	-	PG6	I/O	FT	-	EVENTOUT	-
-	-	92	J14	111	-	-	-	-	-	PG7	I/O	FT	-	USART6_CK, FMC_INT, EVENTOUT	-
-	-	93	H14	112	-	H14	G11	93	112	PG8	I/O	FT	-	USART6_RTS, FMC_SDCLK, EVENTOUT	-
-	-	94	G12	113	-	G12	-	94	113	VSS	S	-	-	-	-
-	-	-	-	-	-	-	F10	-	-	VDD	-	-	-	-	-
-	-	95	H13	114	K1	H13	C11	95	114	VDDUSB	S	-	-	-	-
37	63	96	H15	115	E1	H15	G12	96	115	PC6	I/O	FT	-	TIM3_CH1, TIM8_CH1, I2S2_MCK, USART6_TX, SDMMC2_D6, SDMMC1_D6, EVENTOUT	-
38	64	97	G15	116	D4	G15	F12	97	116	PC7	I/O	FT	-	TIM3_CH2, TIM8_CH2, I2S3_MCK, USART6_RX, SDMMC2_D7, SDMMC1_D7, EVENTOUT	-

Table 11. FMC pin definition

Pin name	NOR/PSRAM/SRAM	NOR/PSRAM Mux	NAND16	SDRAM
PF0	A0	-	-	A0
PF1	A1	-	-	A1
PF2	A2	-	-	A2
PF3	A3	-	-	A3
PF4	A4	-	-	A4
PF5	A5	-	-	A5
PF12	A6	-	-	A6
PF13	A7	-	-	A7
PF14	A8	-	-	A8
PF15	A9	-	-	A9
PG0	A10	-	-	A10
PG1	A11	-	-	A11
PG2	A12	-	-	A12
PG3	A13	-	-	-
PG4	A14	-	-	BA0
PG5	A15	-	-	BA1
PD11	A16	A16	CLE	-
PD12	A17	A17	ALE	-
PD13	A18	A18	-	-
PE3	A19	A19	-	-
PE4	A20	A20	-	-
PE5	A21	A21	-	-
PE6	A22	A22	-	-
PE2	A23	A23	-	-
PG13	A24	A24	-	-
PG14	A25	A25	-	-
PD14	D0	DA0	D0	D0
PD15	D1	DA1	D1	D1
PD0	D2	DA2	D2	D2
PD1	D3	DA3	D3	D3
PE7	D4	DA4	D4	D4
PE8	D5	DA5	D5	D5
PE9	D6	DA6	D6	D6

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load).
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash memory access time is adjusted both to f_{HCLK} frequency and V_{DD} range (see *Table 17: Limitations depending on the operating power supply range*).
- When the regulator is ON, the voltage scaling and over-drive mode are adjusted to f_{HCLK} frequency as follows:
  - Scale 3 for $f_{HCLK} \leq 144$ MHz
  - Scale 2 for 144 MHz < $f_{HCLK} \leq 168$ MHz
  - Scale 1 for 168 MHz < $f_{HCLK} \leq 216$ MHz. The over-drive is only ON at 216 MHz.
- When the regulator is OFF, the V12 is provided externally as described in *Table 16: General operating conditions*:
- The system clock is HCLK, $f_{PCLK1} = f_{HCLK}/4$, and $f_{PCLK2} = f_{HCLK}/2$.
- External clock frequency is 25 MHz and PLL is ON when f_{HCLK} is higher than 25 MHz.
- The typical current consumption values are obtained for 1.7 V ≤ V_{DD} ≤ 3.6 V voltage range and for T_A= 25 °C unless otherwise specified.
- The maximum values are obtained for 1.7 V ≤ V_{DD} ≤ 3.6 V voltage range and a maximum ambient temperature (T_A) unless otherwise specified.
- For the voltage range 1.7 V ≤ V_{DD} ≤ 3.6 V, the maximum frequency is 180 MHz.

Table 24. Typical and maximum current consumption in Run mode, code with data processing running from ITCM RAM, regulator ON

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)			Unit
					T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in RUN mode	All peripherals enabled(2)(3)	216	156	170(4)	180(4)	200	mA
			200	144	154	164.6	183	
			180	127	134(4)	143(4)	158(4)	
			168	113	119	127.4	141	
			144	86	96	112.6	126	
			60	41	44	52.8	65	
			25	22	24	33.5	45	
		All peripherals disabled(3)	216	99	110(4)	119.6(4)	138.5	
			200	92	102	113.1	132	
			180	81	90(4)	96.7(4)	125(4)	
			168	72	78	86.5	100.1	
			144	55	61	77.1	90.8	
			60	24	25	38.5	50.3	
			25	12	13	26.3	38.1	

1. Guaranteed by characterization results.

1. Guaranteed by characterization results.
2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.

Table 31. Typical and maximum current consumptions in Stop mode

Symbol	Parameter	Conditions	Typ	Max(1)			Unit
				V_{DD} = 3.6 V			
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
$I_{DD\_STOP\_NM}$ (normal mode)	Supply current in Stop mode, main regulator in Run mode	Flash memory in Stop mode, all oscillators OFF, no IWDG	0.45	2	12	22	mA
		Flash memory in Deep power down mode, all oscillators OFF	0.4	2	12	22	
	Supply current in Stop mode, main regulator in Low-power mode	Flash memory in Stop mode, all oscillators OFF, no IWDG	0.32	1.5	10	18	
		Flash memory in Deep power down mode, all oscillators OFF, no IWDG	0.27	1.5	10	18	
$I_{DD\_STOP\_UDM}$ (under-drive mode)	Supply current in Stop mode, main regulator in Low voltage and under-drive modes	Regulator in Run mode, Flash memory in Deep power down mode, all oscillators OFF, no IWDG	0.15	0.8	5	7	
		Regulator in Low-power mode, Flash memory in Deep power down mode, all oscillators OFF, no IWDG	0.1	0.7	4	7	

1. Data based on characterization, tested in production.

pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

Where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DD} is the MCU supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT}$

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

Table 34. Switching output I/O current consumption(1)

Symbol	Parameter	Conditions	I/O toggling frequency (fsw) MHz	Typ V_{DD} = 3.3 V	Typ V_{DD} = 1.8 V	Unit
I_{DDIO}	I/O switching Current	C_{EXT} = 0 pF $C = C_{INT} + C_S + C_{EXT}$	2	0.1	0.1	mA
			8	0.4	0.2	
			25	1.1	0.7	
			50	2.4	1.3	
			60	3.1	1.6	
			84	4.3	2.4	
			90	4.9	2.6	
			100	5.4	2.8	
			108	5.6	-	
		C_{EXT} = 10 pF $C = C_{INT} + C_S + C_{EXT}$	2	0.2	0.1	
			8	0.6	0.3	
			25	1.8	1.1	
			50	3.1	2.3	
			60	4.6	3.4	
			84	9.7	3.6	
			90	10.12	5.2	
			100	14.92	5.4	
			108	18.11	-	

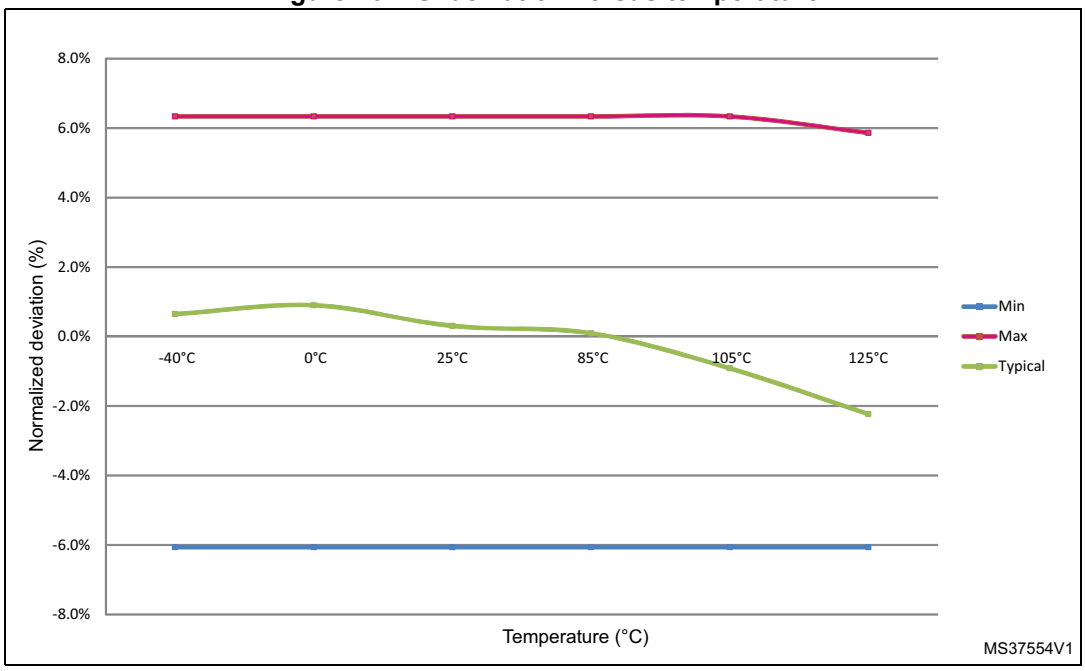
Low-speed internal (LSI) RC oscillator

Table 43. LSI oscillator characteristics (1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}(2)	Frequency	17	32	47	kHz
$t_{su(LSI)}$(3)	LSI oscillator startup time	-	15	40	µs
$I_{DD(LSI)}$(3)	LSI oscillator power consumption	-	0.4	0.6	µA

1. V_{DD} = 3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by characterization results.
3. Guaranteed by design.

Figure 40. LSI deviation versus temperature



6.3.11 PLL characteristics

The parameters given in *Table 44* and *Table 45* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 16*.

Table 44. Main PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock(1)	-	0.95(2)	1	2.10	MHz
f_{PLL_OUT}	PLL multiplier output clock	-	24	-	216	
f_{PLL48_OUT}	48 MHz PLL multiplier output clock	-	-	48	75	
f_{VCO_OUT}	PLL VCO output	-	100	-	432	

Table 61. I/O static characteristics (continued)

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
R_{PU}	Weak pull-up equivalent resistor(6)	All pins except for PA10/PB12 (OTG_FS_ID ,OTG_HS_ID)	$V_{IN} = V_{SS}$	30	40	50	kΩ
		PA10/PB12 (OTG_FS_ID ,OTG_HS_ID)		7	10	14	
R_{PD}	Weak pull-down equivalent resistor(7)	All pins except for PA10/PB12 (OTG_FS_ID ,OTG_HS_ID)	$V_{IN} = V_{DD}$	30	40	50	
		PA10/PB12 (OTG_FS_ID ,OTG_HS_ID)		7	10	14	
C_{IO}(8)	I/O pin capacitance		-	-	5	-	pF

1. Guaranteed by design.
2. Tested in production.
3. With a minimum of 200 mV.
4. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins, Refer to *Table 60: I/O current injection susceptibility*
5. To sustain a voltage higher than VDD +0.3 V, the internal pull-up/pull-down resistors must be disabled. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins.Refer to *Table 60: I/O current injection susceptibility*
6. Pull-up resistors are designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimum (~10% order).
7. Pull-down resistors are designed with a true resistance in series with a switchable NMOS. This NMOS contribution to the series resistance is minimum (~10% order).
8. Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization results.

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements for FT I/Os is shown in *Figure 43*.

Table 67. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{ADC}	ADC clock frequency	V_{DDA} = 1.7(1) to 2.4 V	0.6	15	18	MHz
		V_{DDA} = 2.4 to 3.6 V	0.6	30	36	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 30 MHz, 12-bit resolution	-	-	1764	kHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range(3)	-	0 (V_{SSA} or V_{REF-} tied to ground)	-	V_{REF+}	V
R_{AIN}(2)	External input impedance	See *Equation 1* for details	-	-	50	kΩ
R_{ADC}(2)(4)	Sampling switch resistance	-	1.5	-	6	kΩ
C_{ADC}(2)	Internal sample and hold capacitor	-	-	4	7	pF
t_{lat}(2)	Injection trigger conversion latency	f_{ADC} = 30 MHz	-	-	0.100	µs
		-	-	-	3(5)	$1/f_{ADC}$
t_{latr}(2)	Regular trigger conversion latency	f_{ADC} = 30 MHz	-	-	0.067	µs
		-	-	-	2(5)	$1/f_{ADC}$
t_S(2)	Sampling time	f_{ADC} = 30 MHz	0.100	-	16	µs
		-	3	-	480	$1/f_{ADC}$
t_{STAB}(2)	Power-up time	-	-	2	3	µs
t_{CONV}(2)	Total conversion time (including sampling time)	f_{ADC} = 30 MHz 12-bit resolution	0.50	-	16.40	µs
		f_{ADC} = 30 MHz 10-bit resolution	0.43	-	16.34	µs
		f_{ADC} = 30 MHz 8-bit resolution	0.37	-	16.27	µs
		f_{ADC} = 30 MHz 6-bit resolution	0.30	-	16.20	µs
		9 to 492 (t_S for sampling +n-bit resolution for successive approximation)				$1/f_{ADC}$
f_S(2)	Sampling rate (f_{ADC} = 36 MHz, and t_S = 3 ADC cycles)	12-bit resolution Single ADC	-	-	2.4	Msps
		12-bit resolution Interleave Dual ADC mode	-	-	4.5	Msps
		12-bit resolution Interleave Triple ADC mode	-	-	7.2	Msps

I²S interface characteristics

Unless otherwise specified, the parameters given in *Table 82* for the I²S interface are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 16*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.20: I/O port characteristics* for more details on the input/output alternate function characteristics (CK, SD, WS).

Table 82. I²S dynamic characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I2S Main clock output	-	256 x 8K	256xFs(2)	MHz
f_{CK}	I2S clock frequency	Master data: 32 bits	-	64xFs	MHz
		Slave data: 32 bits	-	64xFs	
D_{CK}	I2S clock frequency duty cycle	Slave receiver	30	70	%
$t_{v(WS)}$	WS valid time	Master mode	-	3	ns
$t_{h(WS)}$	WS hold time	Master mode	0	-	
$t_{su(WS)}$	WS setup time	Slave mode	5	-	
$t_{h(WS)}$	WS hold time	Slave mode	2	-	
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	2.5	-	
$t_{su(SD\_SR)}$		Slave receiver	2.5	-	
$t_{h(SD\_MR)}$	Data input hold time	Master receiver	3.5	-	
$t_{h(SD\_SR)}$		Slave receiver	2	-	
$t_{v(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	12	
$t_{v(SD\_MT)}$		Master transmitter (after enable edge)	-	3	
$t_{h(SD\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	5	-	
$t_{h(SD\_MT)}$		Master transmitter (after enable edge)	0	-	

1. Guaranteed by characterization results.
2. 256xFs maximum is 49.152 MHz (APB1 Maximum frequency).

Note: Refer to RM0385 reference manual I2S section for more details on the sampling frequency (F_S).

*f_{MCK}, f_{CK}, and D_{CK} values reflect only the digital peripheral behavior. The values of these parameters might be slightly impacted by the source clock precision. D_{CK} depends mainly on the value of ODD bit. The digital contribution leads to a minimum value of (I2SDIV/(2*I2SDIV+ODD) and a maximum value of (I2SDIV+ODD)/(2*I2SDIV+ODD). F_S maximum value is supported for each mode/condition.*

Figure 76. SDIO high-speed mode

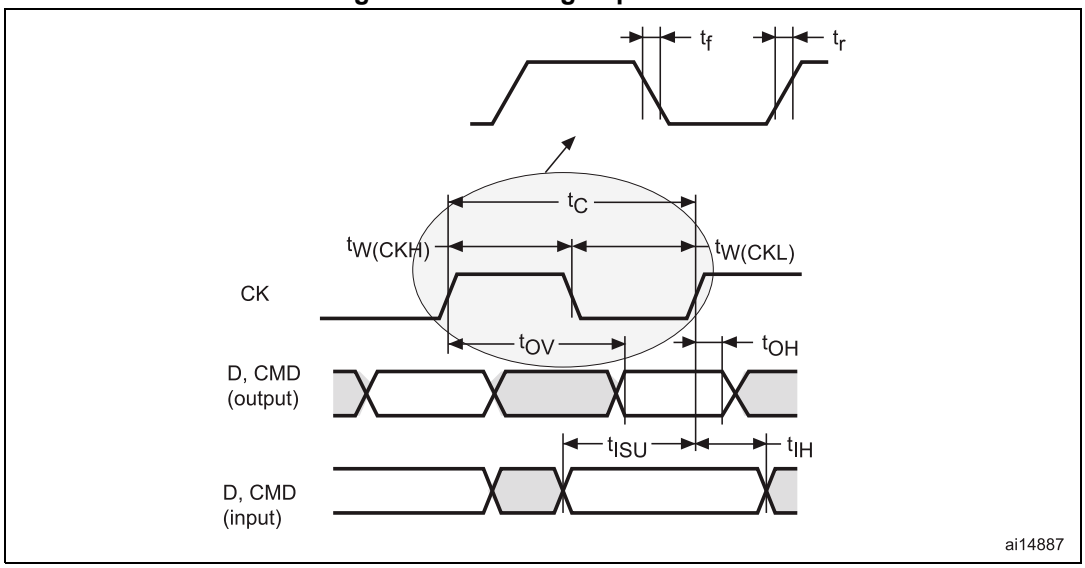


Figure 77. SD default mode

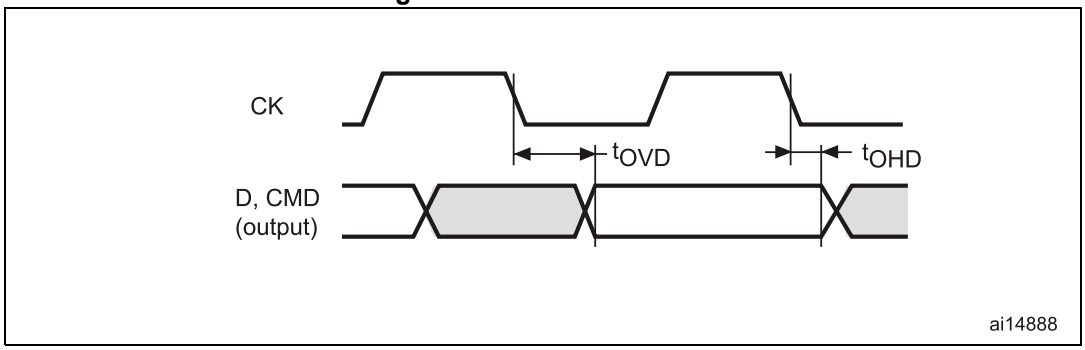
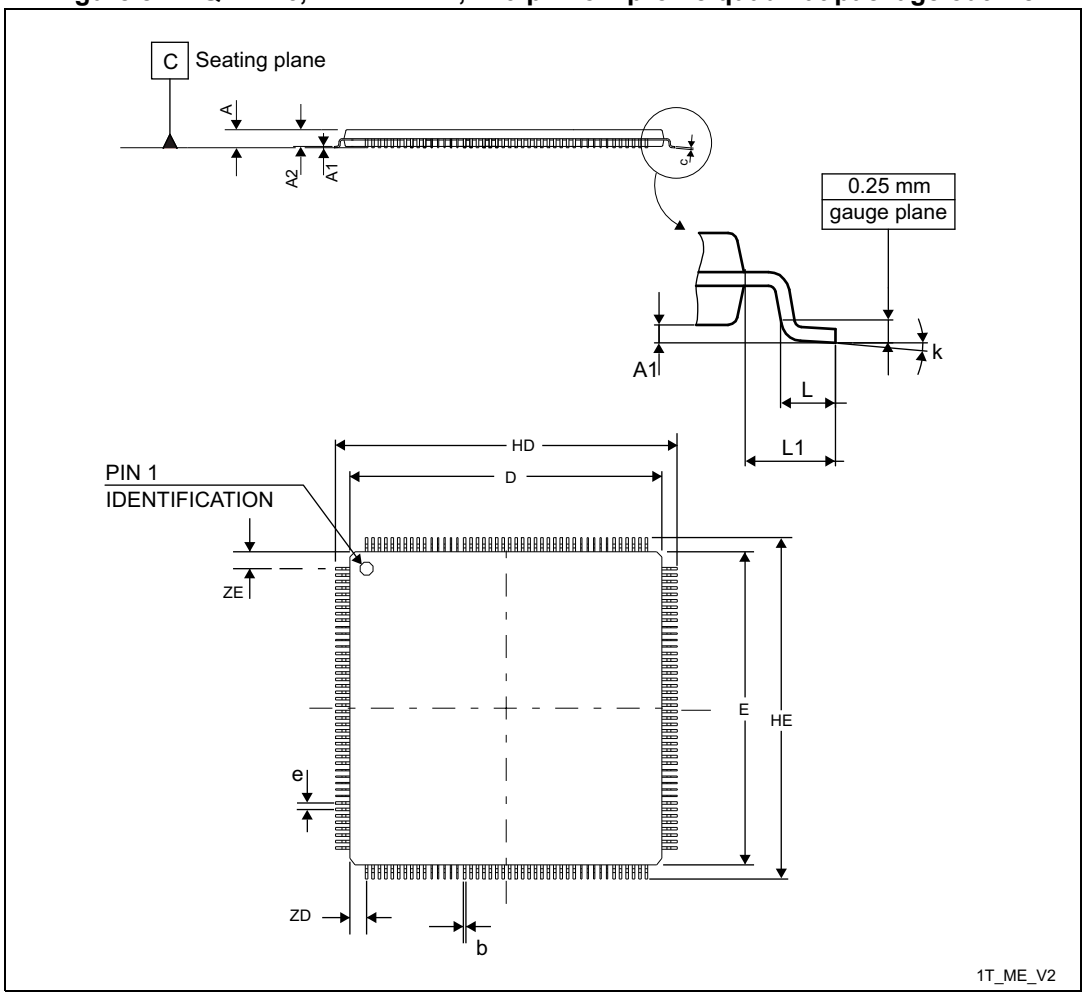


Table 113. Dynamic characteristics: SD / MMC characteristics, V_{DD}=2.7V to 3.6V(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	50	MHz
-	SDMMC_CK/fPCLK2 frequency ratio	-	-	-	8/3	-
$t_{W(CKL)}$	Clock low time	fpp =50 MHz	9	10	-	ns
$t_{W(CKH)}$	Clock high time	fpp =50 MHz	9	10	-	
CMD, D inputs (referenced to CK) in MMC and SD HS mode						
t_{ISU}	Input setup time HS	fpp =50 MHz	1	-	-	ns
t_{IH}	Input hold time HS	fpp =50 MHz	3	-	-	
CMD, D outputs (referenced to CK) in MMC and SD HS mode						
t_{OV}	Output valid time HS	fpp =50 MHz	-	11	12	ns
t_{OH}	Output hold time HS	fpp =50 MHz	9	-	-	

7.4 LQFP176 24 x 24 mm low-profile quad flat package information

Figure 87. LQFP176, 24 x 24 mm, 176-pin low-profile quad flat package outline



1. Drawing is not to scale.

Table 118. LQFP176, 24 x 24 mm, 176-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	-	1.450	0.0531	-	0.0060
b	0.170	-	0.270	0.0067	-	0.0106
C	0.090	-	0.200	0.0035	-	0.0079
D	23.900	-	24.100	0.9409	-	0.9488

Table 118. LQFP176, 24 x 24 mm, 176-pin low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E	23.900	-	24.100	0.9409	-	0.9488
e	-	0.500	-	-	0.0197	-
HD	25.900	-	26.100	1.0200	-	1.0276
HE	25.900	-	26.100	1.0200	-	1.0276
L	0.450	-	0.750	0.0177	-	0.0295
L1	-	1.000	-	-	0.0394	-
ZD	-	1.250	-	-	0.0492	-
ZE	-	1.250	-	-	0.0492	-
ccc	-	-	0.080	-	-	0.0031
k	0 °	-	7 °	0 °	-	7 °

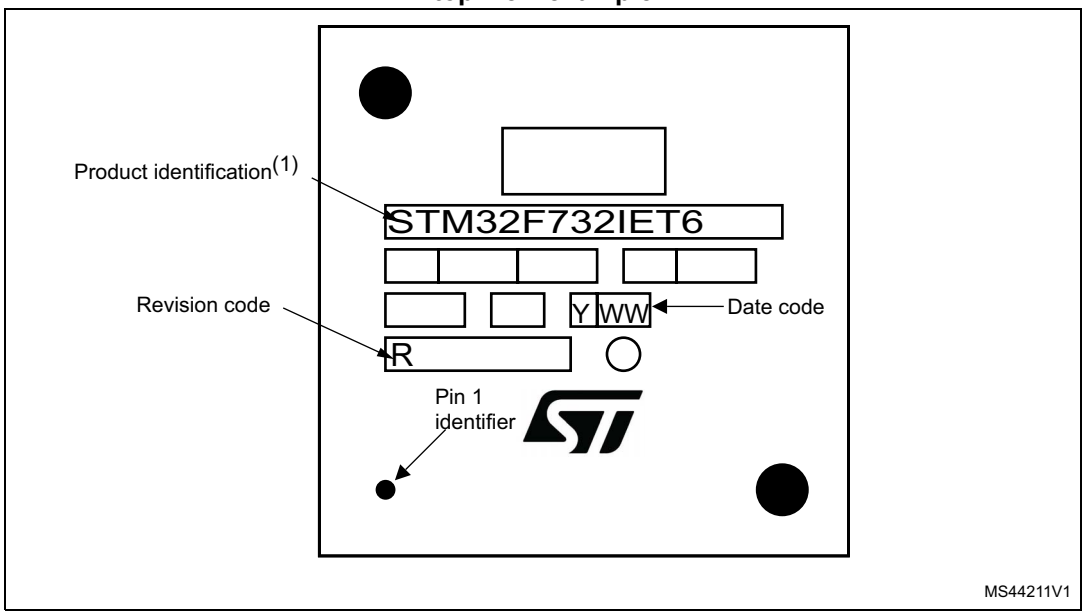
1. Values in inches are converted from mm and rounded to 4 decimal digits.

LQFP176 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 89. LQFP176, 24 x 24 mm, 176-pin low-profile quad flat package top view example



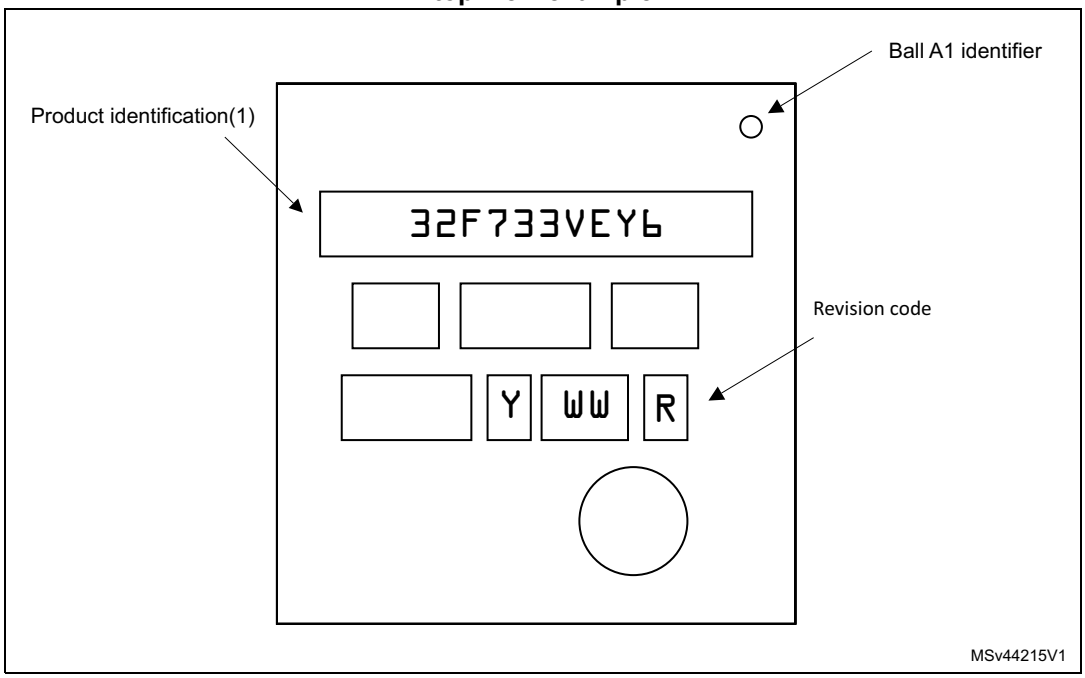
1. Parts marked as ES or E or accompanied by an engineering sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

WLCSP100 device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 98. WLCSP100 – 100L, 4.166 x 4.628 mm 0.4 mm pitch top view example



1. Parts marked as ES or E or accompanied by an engineering sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.