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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	216MHz
Connectivity	CANbus, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	50
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f732ret6

On the STM32F7x3xx devices, the USB OTG HS sub-system uses an additional power supply pin:

- The VDD12OTGHS pin is the output of PHY HS regulator (1.2V). An external capacitor of 2.2 µF must be connected on the VDD12OTGHS pin.

3.15 Power supply supervisor

3.15.1 Internal reset ON

On packages embedding the PDR_ON pin, the power supply supervisor is enabled by holding PDR_ON high. On the other packages, the power supply supervisor is always enabled.

The device has an integrated power-on reset (POR)/ power-down reset (PDR) circuitry coupled with a Brownout reset (BOR) circuitry. At power-on, POR/PDR is always active and ensures proper operation starting from 1.8 V. After the 1.8 V POR threshold level is reached, the option byte loading process starts, either to confirm or modify default BOR thresholds, or to disable BOR permanently. Three BOR thresholds are available through option bytes. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR}, without the need for an external reset circuit.

The device also features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.15.2 Internal reset OFF

This feature is available only on packages featuring the PDR_ON pin. The internal power-on reset (POR) / power-down reset (PDR) circuitry is disabled through the PDR_ON pin.

An external power supply supervisor should monitor V_{DD} and NRST and should maintain the device in reset mode as long as V_{DD} is below a specified threshold. PDR_ON should be connected to V_{SS}. Refer to *Figure 9: Power supply supervisor interconnection with internal reset OFF*.

3.16.3 Regulator ON/OFF and internal reset ON/OFF availability

Table 4. Regulator ON/OFF and internal reset ON/OFF availability

Package	Regulator ON	Regulator OFF	Internal reset ON	Internal reset OFF
LQFP64, LQFP100	Yes	No	Yes	No
LQFP144			Yes PDR_ON set to V_{DD}	Yes PDR_ON set to V_{SS}
LQFP176, UFBGA144, UFBGA176	Yes BYPASS_REG set to V_{SS}	Yes BYPASS_REG set to V_{DD}		

3.17 Real-time clock (RTC), backup SRAM and backup registers

The RTC is an independent BCD timer/counter. It supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.
- Two programmable alarms.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy.
- Three anti-tamper detection pins with programmable filter.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event, or by a switch to V_{BAT} mode.
- 17-bit auto-reload wakeup timer (WUT) for periodic events with programmable resolution and period.

The RTC and the 32 backup registers are supplied through a switch that takes power either from the V_{DD} supply when present or from the V_{BAT} pin.

The backup registers are 32-bit registers used to store 128 bytes of user application data when V_{DD} power is not present. They are not reset by a system or power reset, or when the device wakes up from Standby mode.

The RTC clock sources can be:

- A 32.768 kHz external crystal (LSE)
- An external resonator or oscillator(LSE)
- The internal low power RC oscillator (LSI, with typical frequency of 32 kHz)
- The high-speed external clock (HSE) divided by 32

The RTC is functional in V_{BAT} mode and in all low-power modes when it is clocked by the LSE. When clocked by the LSI, the RTC is not functional in V_{BAT} mode, but is functional in all low-power modes.

3.20.4 Low-power timer (LPTIM1)

The low-power timer has an independent clock and is running also in Stop mode if it is clocked by LSE, LSI or an external clock. It is able to wakeup the devices from Stop mode.

This low-power timer supports the following features:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous / one-shot mode
- Selectable software / hardware input trigger
- Selectable clock source:
- Internal clock source: LSE, LSI, HSI or APB clock
- External clock source over LPTIM input (working even with no internal clock source running, used by the Pulse Counter Application)
- Programmable digital glitch filter
- Encoder mode

3.20.5 Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes.

3.20.6 Window watchdog

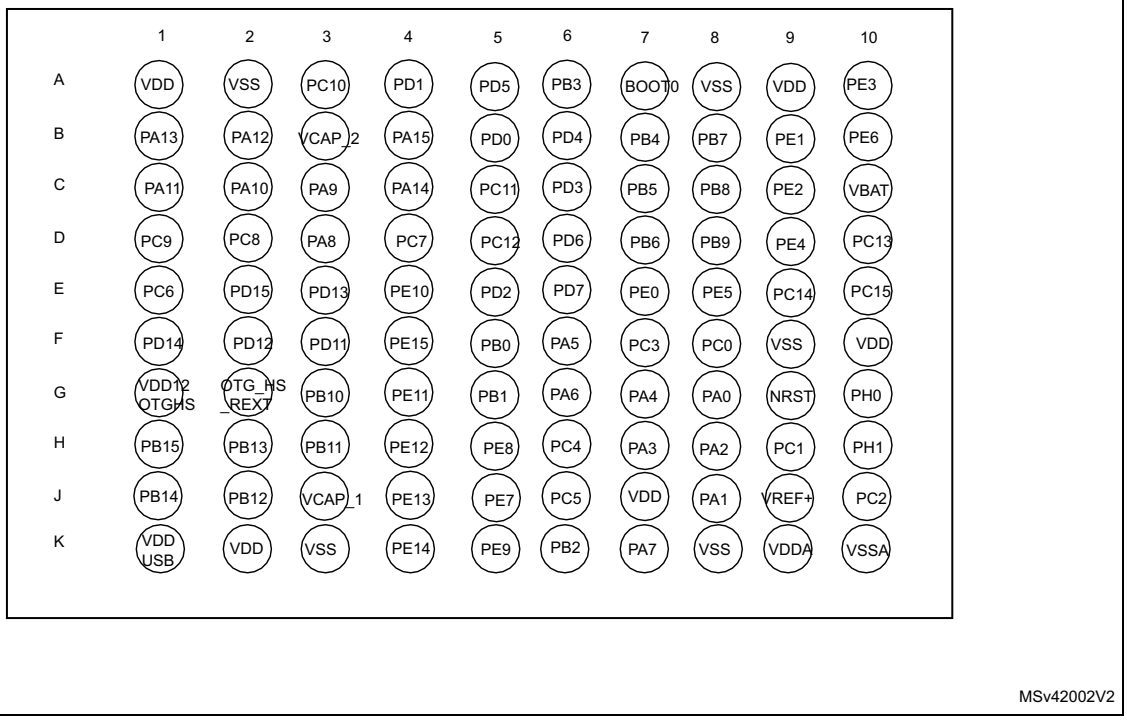
The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.20.7 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard downcounter. It features:

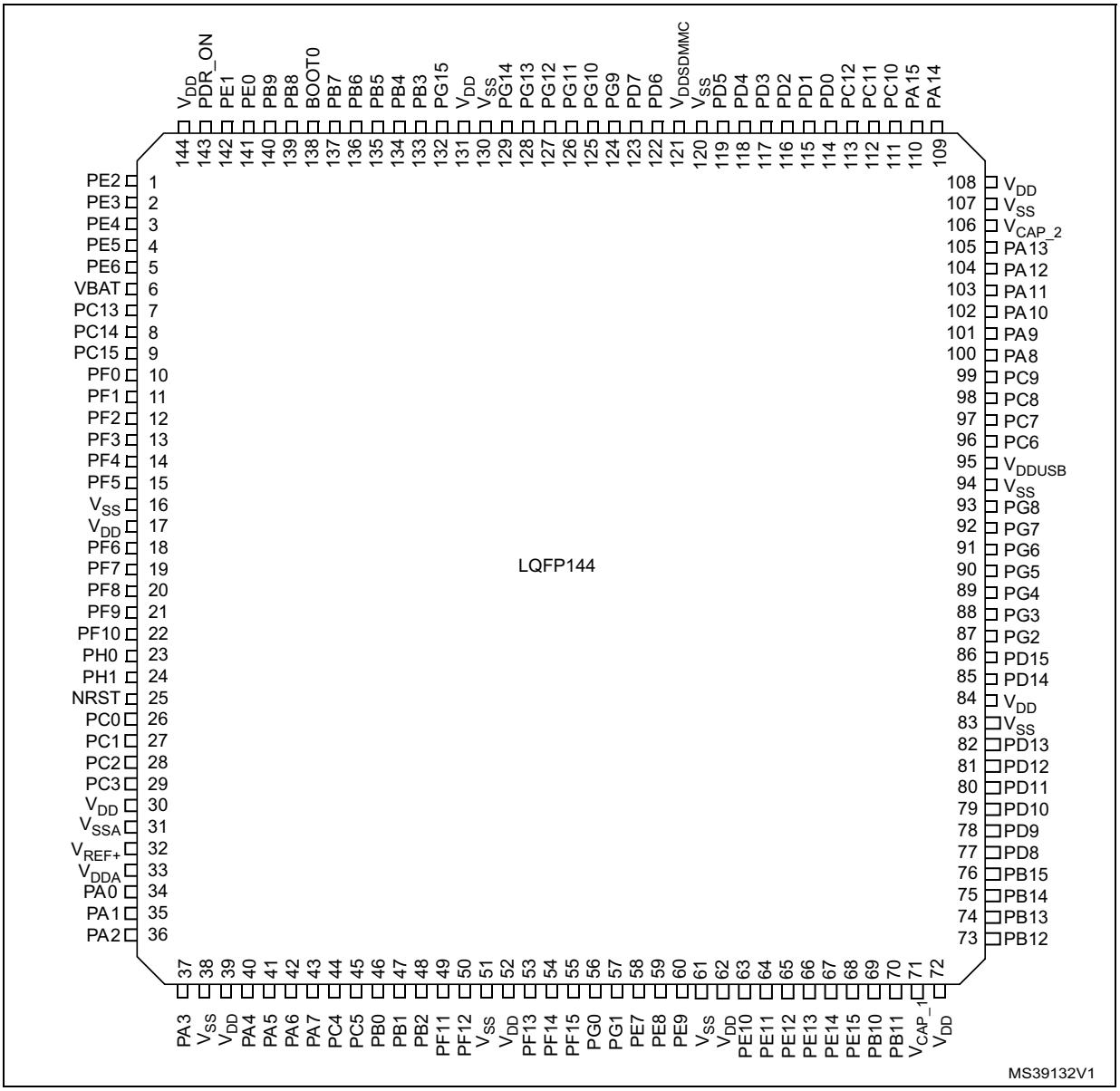
- A 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

Figure 16. STM32F733xx WLCSP100 ballout (with OTG PHY HS)



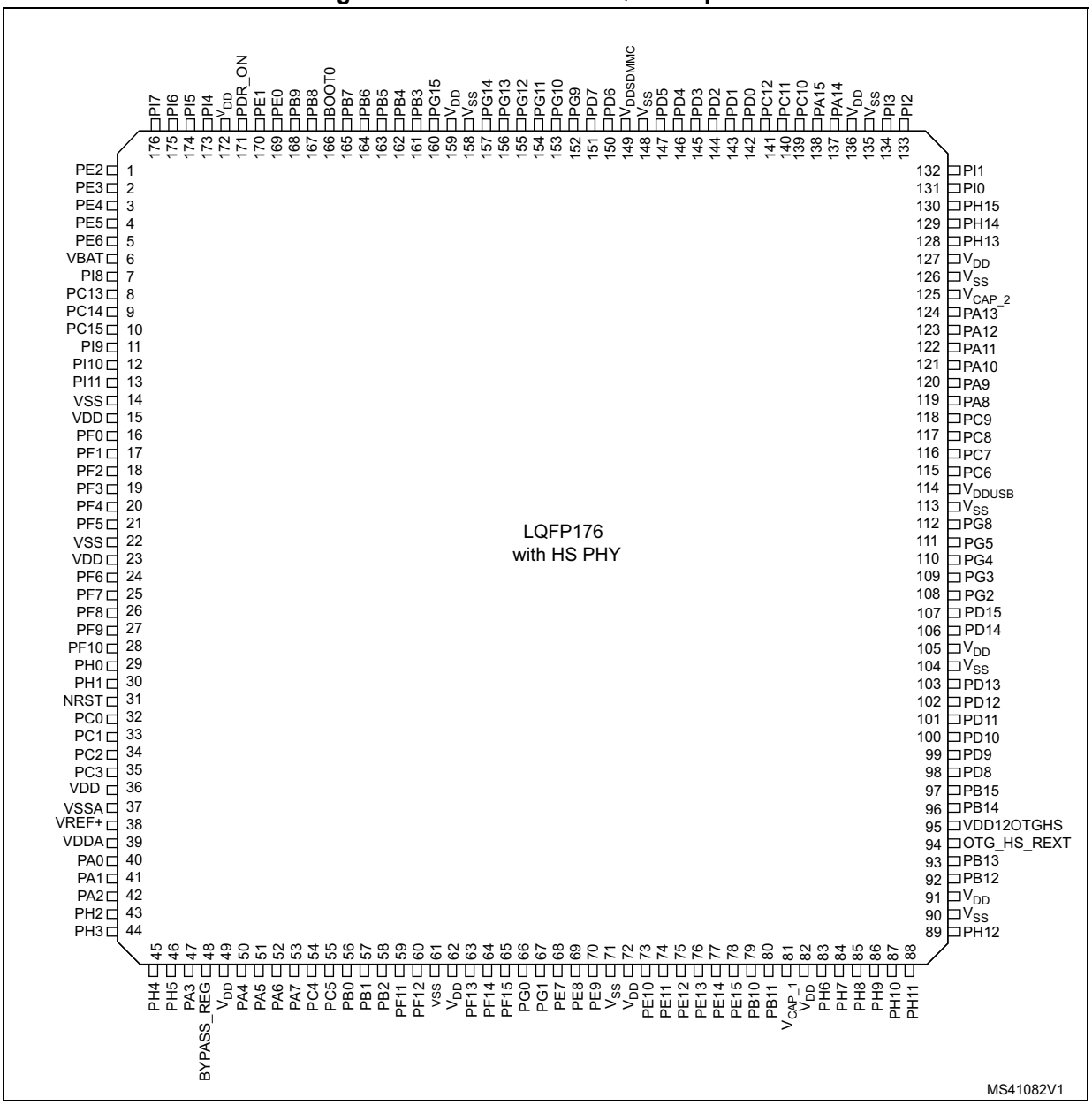
1. The above figure shows the package top view.

Figure 17. STM32F732xx LQFP144 pinout



1. The above figure shows the package top view.

Figure 21. STM32F733xx LQFP176 pinout



1. The above figure shows the package top view.

Table 10. STM32F732xx and STM32F733xx pin and ball definition (continued)

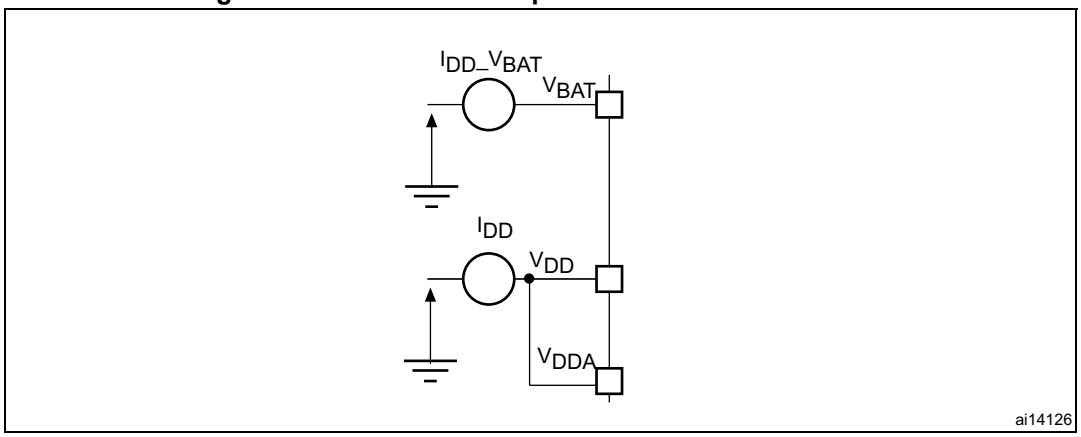
Pin Number										Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F732xx					STM32F733xx										
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
25	34	46	R5	56	F5	R5	L4	46	56	PB0	I/O	FT	(4)	TIM1_CH2N, TIM3_CH3, TIM8_CH2N, UART4_CTS, OTG_HS_ULPI_D1, EVENTOUT	ADC1_IN8, ADC2_IN8
26	35	47	R4	57	G5	R4	M4	47	57	PB1	I/O	FT	(4)	TIM1_CH3N, TIM3_CH4, TIM8_CH3N, OTG_HS_ULPI_D2, EVENTOUT	ADC1_IN9, ADC2_IN9
27	36	48	M6	58	K6	M6	J5	48	58	PB2	I/O	FT	-	SAI1_SD_A, SPI3_MOSI/I2S3_SD, QUADSPI_CLK, EVENTOUT	-
-	-	49	R6	59	-	R6	M5	49	59	PF11	I/O	FT	-	SPI5_MOSI, SAI2_SD_B, FMC_SDNRAS, EVENTOUT	-
-	-	50	P6	60	-	P6	L5	50	60	PF12	I/O	FT	-	FMC_A6, EVENTOUT	-
-	-	51	M8	61	-	M8	-	51	61	VSS	S	-	-	-	-
-	-	52	N8	62	-	N8	G5	52	62	VDD	S	-	-	-	-
-	-	53	N6	63	-	N6	K5	53	63	PF13	I/O	FT	-	FMC_A7, EVENTOUT	-
-	-	54	R7	64	-	R7	M6	54	64	PF14	I/O	FT	-	FMC_A8, EVENTOUT	-
-	-	55	P7	65	-	P7	L6	55	65	PF15	I/O	FT	-	FMC_A9, EVENTOUT	-
-	-	56	N7	66	-	N7	K6	56	66	PG0	I/O	FT	-	FMC_A10, EVENTOUT	-
-	-	57	M7	67	-	M7	J6	57	67	PG1	I/O	FT	-	FMC_A11, EVENTOUT	-

2. The two 2.2 µF ceramic capacitors should be replaced by two 100 nF decoupling capacitors when the voltage regulator is OFF.
3. The 4.7 µF ceramic capacitor must be connected to one of the V_{DD} pin.
4. V_{DDA}=V_{DD} and V_{SSA}=V_{SS}.

Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA} ...) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure good operation of the device. It is not recommended to remove filtering capacitors to reduce PCB size or cost. This might cause incorrect operation of the device.

6.1.7 Current consumption measurement

Figure 28. Current consumption measurement scheme



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 13: Voltage characteristics*, *Table 14: Current characteristics*, and *Table 15: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. The device mission profile (application conditions) is compliant with JEDEC JESD47 Qualification Standard. Extended mission profiles are available on demand.

Table 13. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD}–V_{SS}	External main supply voltage (including V_{DDA}, V_{DD}, V_{BAT}, V_{DDUSB} and $V_{DDSDMMC}$) (1)	− 0.3	4.0	V
V_{IN}	Input voltage on FT pins(2)	V_{SS} − 0.3	V_{DD}+4.0	
	Input voltage on TTa pins	V_{SS} − 0.3	4.0	
	Input voltage on any other pin	V_{SS} − 0.3	4.0	
	Input voltage on BOOT pin	V_{SS}	9.0	

Table 29. Typical and maximum current consumption in Sleep mode, regulator ON

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)			Unit
					TA= 25 °C	TA=85 °C	TA=105 °C	
I_{DD}	Supply current in SLEEP mode	All peripherals enabled(2)	216	82	96(3)	109.3(3)	128.3	mA
			200	77	84	103.4	122.6	
			180	67	72(3)	88.3(3)	120(3)	
			168	60	64	78.9	92.7	
			144	46	49	61.8	73.6	
			60	24	26	37.2	49	
			25	14	16	27	38.8	
		All peripherals disabled	216	24	28(3)	42.9(3)	62.2	
			200	22	26	41.9	61.2	
			180	19	21(3)	33.2(3)	48(3)	
			168	17	19	30.1	43.9	
			144	13	15	24.6	36.3	
			60	7	9	20.5	32.3	
			25	5	7	18.8	30.6	

1. Guaranteed by characterization results.
2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.
3. Guaranteed by test in production.

Table 30. Typical and maximum current consumption in Sleep mode, regulator OFF

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ		Max(1)						Unit
						TA= 25 °C		TA= 85 °C		TA= 105 °C		
				IDD12	IDD	IDD12	IDD	IDD12	IDD	IDD12	IDD	
IDD12/ IDD	Supply current in RUN mode from V12 and V_{DD} supply	All Peripherals Enabled(2)	180	62	1.3	67.5	2	84.4	2	95	2	mA
			168	55	1.3	59.8	2	75.4	2	86	2	
			144	43	1.3	46.3	2	59.6	2	70	2	
			60	22	1	24	2	35.8	2	46	2	
			25	13	1	15	2	25.8	2	36	2	
		All Peripherals Disabled	180	17	1.3	19	2	31.4	2	42	2	
			168	15	1.3	17	2	28.4	2	40	2	
			144	12	1.2	14	2	23.2	2	33	2	
			60	5	1	6	2	19.3	2	29	2	
			25	3	1	4	2	17.6	2	28	2	

Table 33. Typical and maximum current consumptions in V_{BAT} mode

Symbol	Parameter	Conditions[1]	Typ			Max[2]		Unit
			T_A =25 °C			T_A =85 °C	T_A =105 °C	
			V_{BAT} = 1.7 V	V_{BAT}= 2.4 V	V_{BAT}= 3.3 V	V_{BAT} = 3.6 V		
I_{DD_VBAT}	Supply current in V_{BAT} mode	Backup SRAM OFF, RTC and LSE OFF	0.035	0.037	0.043	4	10	µA
		Backup SRAM ON, RTC and LSE OFF	0.69	0.71	0.73	9	20	
		Backup SRAM OFF, RTC ON and LSE in low drive mode	0.57	0.74	1.05	98	244	
		Backup SRAM OFF, RTC ON and LSE in medium low drive mode	0.59	0.76	1.08	101	251	
		Backup SRAM OFF, RTC ON and LSE in medium high drive mode	0.69	0.86	1.19	111	277	
		Backup SRAM OFF, RTC ON and LSE in high drive mode	0.8	0.98	1.31	122	305	
		Backup SRAM ON, RTC ON and LSE in low drive mode	1.22	1.41	1.74	162	405	
		Backup SRAM ON, RTC ON and LSE in Medium low drive mode	1.25	1.43	1.78	166	414	
		Backup SRAM ON, RTC ON and LSE in Medium high drive mode	1.46	1.65	2.01	187	468	
		Backup SRAM ON, RTC ON and LSE in High drive mode	1.46	1.65	2.01	187	468	

1. Crystal used: Abracon ABS07-120-32.768 kHz-T with a C_L of 6 pF for typical values.
2. Guaranteed by characterization results.

Table 37. Low-power mode wakeup timings (continued)

Symbol	Parameter	Conditions	Typ(1)	Max(1)	Unit
t_{WUSTOP}(2)	Wakeup from Stop mode with MR/LP regulator in Under-drive mode	Main regulator in under-drive mode (Flash memory in Deep power-down mode)	107.4	113.2	µs
		Low power regulator in under-drive mode (Flash memory in Deep power-down mode)	112.7	120	
tWUSTDBY(2)	Wakeup from Standby mode	Exit Standby mode on rising edge	308	313	µs
		Exit Standby mode on falling edge	307	313	

1. Guaranteed by characterization results.
2. The wakeup times are measured from the wakeup event to the point in which the application code reads the first

6.3.9 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard I/O. The external clock signal has to respect the *Table 61: I/O static characteristics*. However, the recommended clock input waveform is shown in *Figure 35*.

The characteristics given in *Table 38* result from tests performed using an high-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 16*.

Table 38. High-speed external user clock characteristics

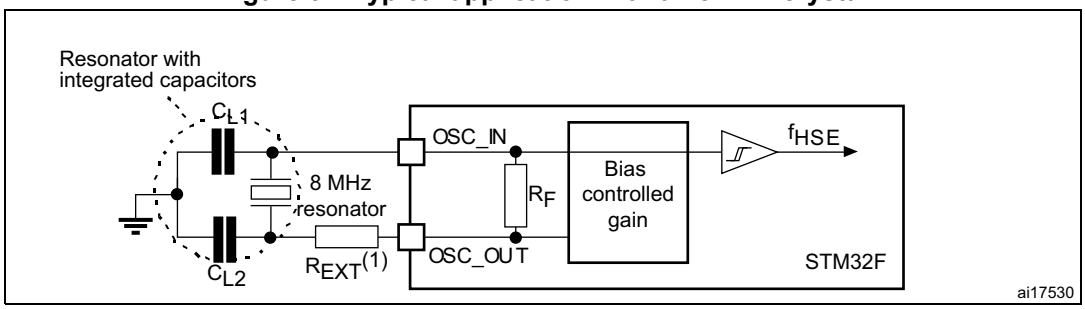
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	External user clock source frequency(1)	-	1	-	50	MHz
V_{HSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSE)}$ $t_{w(HSE)}$	OSC_IN high or low time(1)		5	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time(1)		-	-	10	
$C_{in(HSE)}$	OSC_IN input capacitance(1)	-	-	5	-	pF
$DuCy_{(HSE)}$	Duty cycle	-	45	-	55	%
I_L	OSC_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA

1. Guaranteed by design.

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 37*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 37. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 41*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 41. LSE oscillator characteristics (f_{LSE} = 32.768 kHz) (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	LSE current consumption	LSEDRV[1:0]=00 Low drive capability	-	250	-	nA
		LSEDRV[1:0]=10 Medium low drive capability	-	300	-	
		LSEDRV[1:0]=01 Medium high drive capability	-	370	-	
		LSEDRV[1:0]=11 High drive capability	-	480	-	

- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application, executing EEMBC code, is running. This emission test is compliant with SAE IEC61967-2 standard which specifies the test board and the pin loading.

Table 57. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{CPU}]	Unit
				25/200 MHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = 25 °C, LQFP176 package, conforming to IEC61967-2 ART/L1-cache OFF, over-drive ON, all peripheral clocks enabled, clock dithering disabled.	0.1 MHz to 30 MHz	23	dBµV
			30 MHz to 130 MHz	20	
			130 MHz to 1 GHz	34	
			1 GHz to 2 GHz	24	
			EMI Level	4	-

6.3.18 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/ESDA/JEDEC JS-001-2012 and ANSI/ESD S5.3.1-2009 standards.

Table 58. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C conforming to ANSI/ESDA/JEDEC JS-001-2012	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to ANSI/ESD STM5.3.1-2009, all the packages excepted WLCSP100	3	250	

1. Guaranteed by characterization results.

I²S interface characteristics

Unless otherwise specified, the parameters given in *Table 82* for the I²S interface are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 16*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.20: I/O port characteristics* for more details on the input/output alternate function characteristics (CK, SD, WS).

Table 82. I²S dynamic characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I2S Main clock output	-	256 x 8K	256xFs(2)	MHz
f_{CK}	I2S clock frequency	Master data: 32 bits	-	64xFs	MHz
		Slave data: 32 bits	-	64xFs	
D_{CK}	I2S clock frequency duty cycle	Slave receiver	30	70	%
$t_{v(WS)}$	WS valid time	Master mode	-	3	ns
$t_{h(WS)}$	WS hold time	Master mode	0	-	
$t_{su(WS)}$	WS setup time	Slave mode	5	-	
$t_{h(WS)}$	WS hold time	Slave mode	2	-	
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	2.5	-	
$t_{su(SD\_SR)}$		Slave receiver	2.5	-	
$t_{h(SD\_MR)}$	Data input hold time	Master receiver	3.5	-	
$t_{h(SD\_SR)}$		Slave receiver	2	-	
$t_{v(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	12	
$t_{v(SD\_MT)}$		Master transmitter (after enable edge)	-	3	
$t_{h(SD\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	5	-	
$t_{h(SD\_MT)}$		Master transmitter (after enable edge)	0	-	

1. Guaranteed by characterization results.
2. 256xFs maximum is 49.152 MHz (APB1 Maximum frequency).

Note: Refer to RM0385 reference manual I2S section for more details on the sampling frequency (F_S).

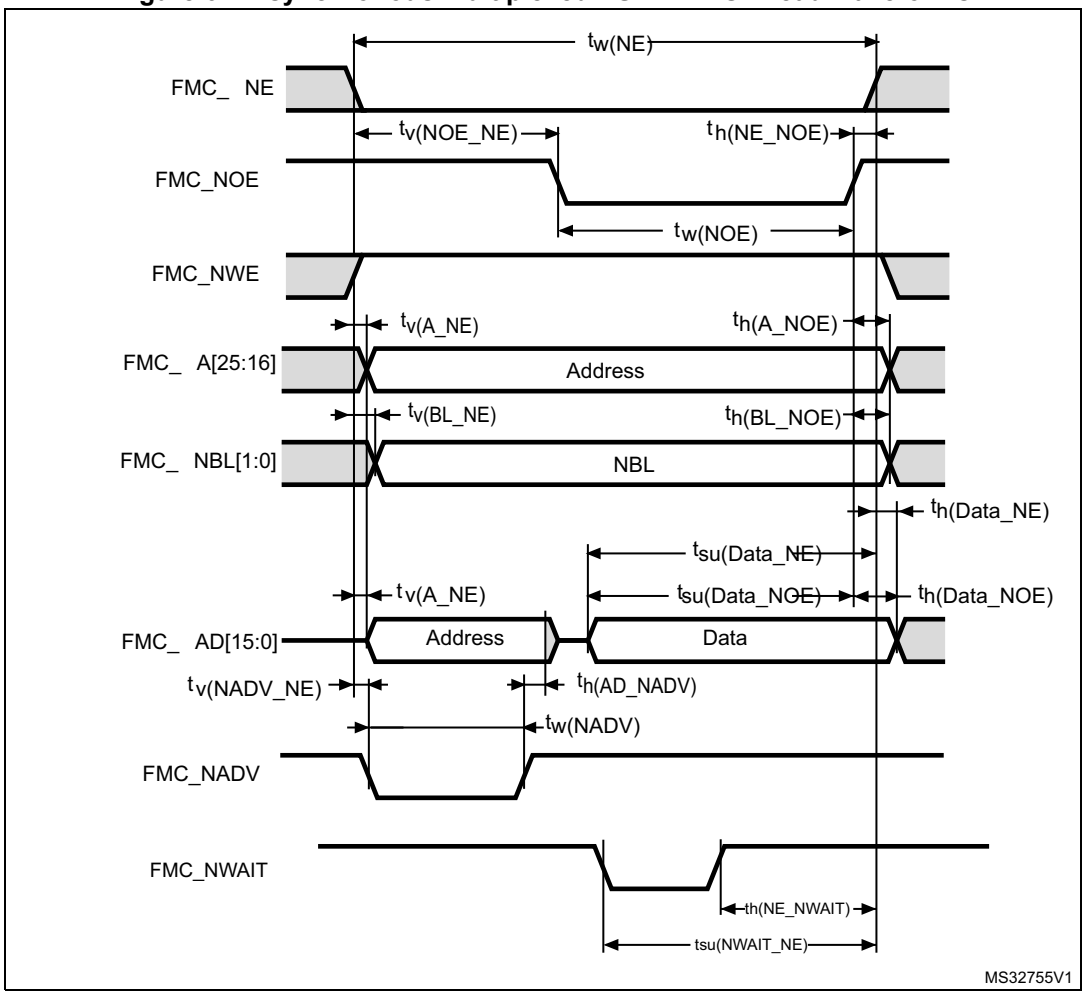
*f_{MCK}, f_{CK}, and D_{CK} values reflect only the digital peripheral behavior. The values of these parameters might be slightly impacted by the source clock precision. D_{CK} depends mainly on the value of ODD bit. The digital contribution leads to a minimum value of (I2SDIV/(2*I2SDIV+ODD) and a maximum value of (I2SDIV+ODD)/(2*I2SDIV+ODD). F_S maximum value is supported for each mode/condition.*

Table 96. Asynchronous non-multiplexed SRAM/PSRAM/NOR write - NWAIT timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	8Thclk -1	8Thclk +1	ns
$t_{w(NWE)}$	FMC_NWE low time	6Thclk -1.5	6Thclk +0.5	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	6Thclk -1	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	4Thclk + 2	-	

1. Guaranteed by characterization results.

Figure 62. Asynchronous multiplexed PSRAM/NOR read waveforms



SDRAM waveforms and timings

- CL = 30 pF on data and address lines. CL = 10 pF on FMC_SDCLK unless otherwise specified.

In all timing tables, the T_{HCLK} is the HCLK clock period.

- For 3.0 V≤V_{DD}≤3.6 V, maximum FMC_SDCLK= 100 MHz at CL=20 pF (on FMC_SDCLK).
- For 2.7 V≤V_{DD}≤3.6 V, maximum FMC_SDCLK = 90 MHz at CL=30 pF (on FMC_SDCLK).
- For 1.71 V≤V_{DD}<1.9 V, maximum FMC_SDCLK = 70 MHz at CL=10 pF (on FMC_SDCLK).

Figure 72. SDRAM read access waveforms (CL = 1)

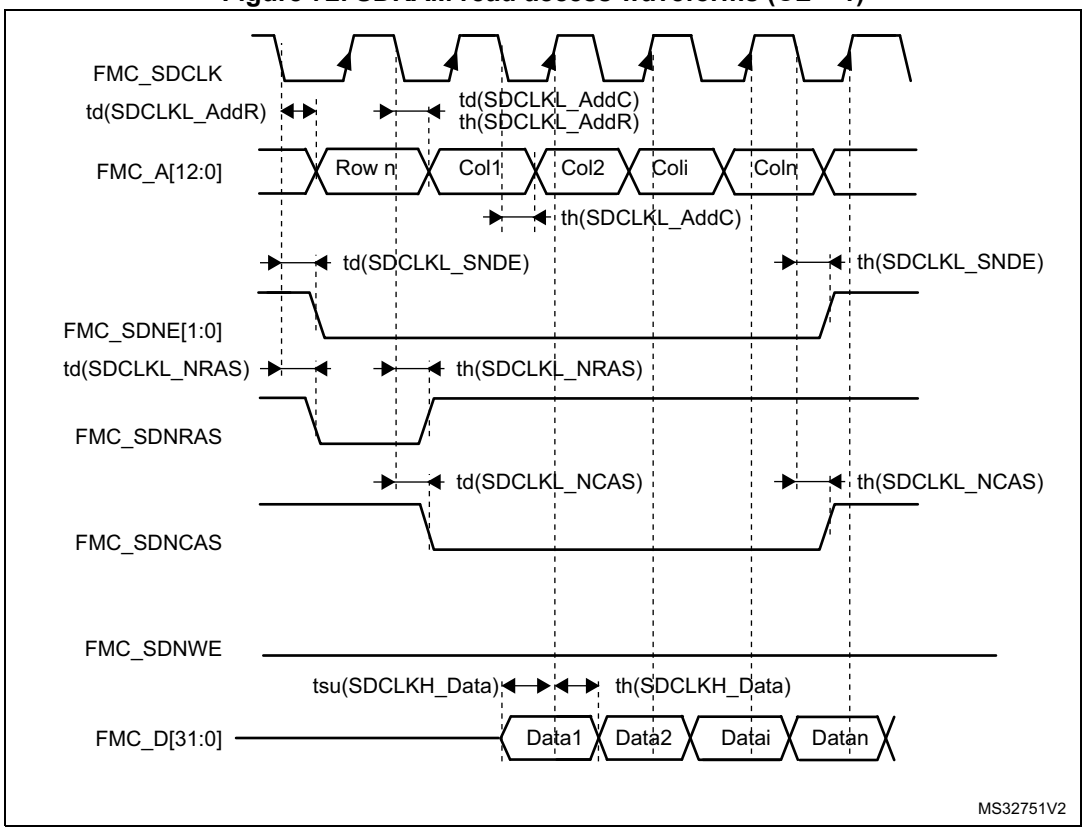
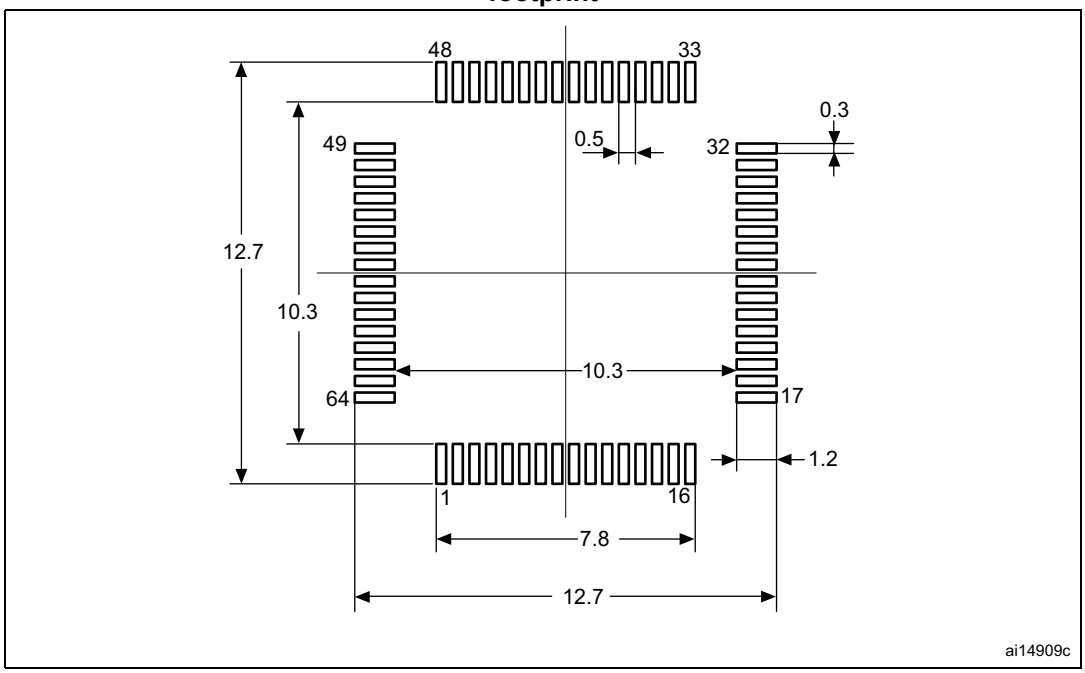


Table 115. LQFP64 – 10 x 10 mm, low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
c	0.09	-	0.20	0.0035	-	0.0079
D	-	12.00	-	-	0.4724	-
D1	-	10.00	-	-	0.3937	-
D3	-	7.50	-	-	0.2953	-
E	-	12.00	-	-	0.4724	-
E1	-	10.00	-	-	0.3937	-
E3	-	7.50	-	-	0.2953	-
e	-	0.50	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	-	1.00	-	-	0.0394	-
ccc	-	-	0.08	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

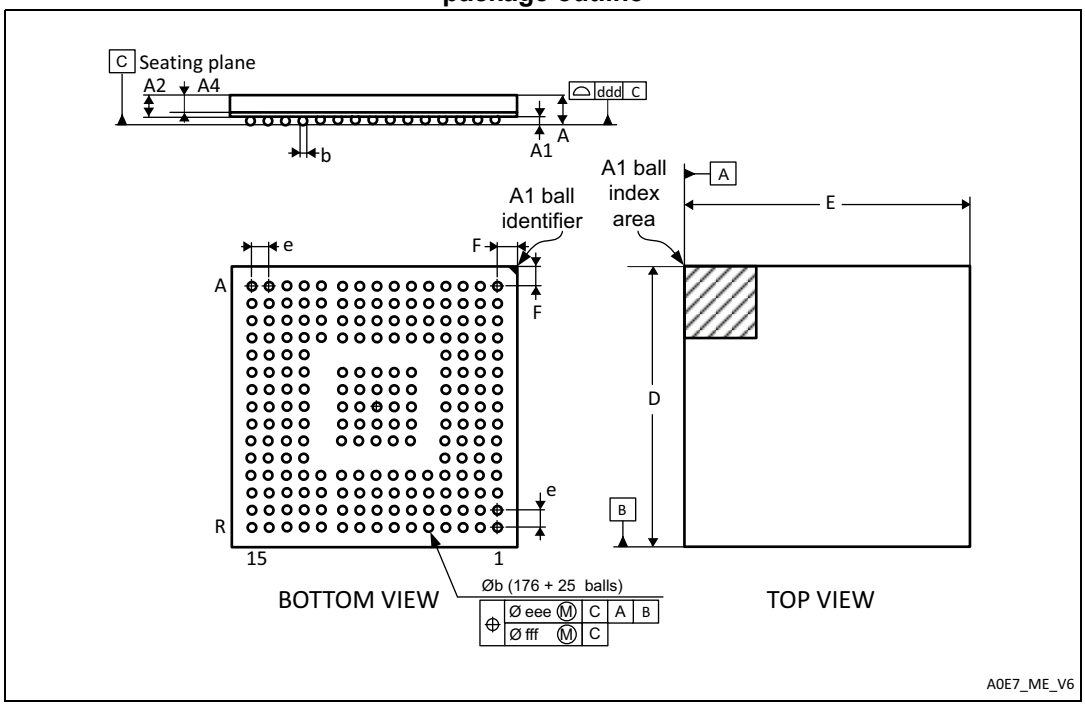
Figure 79. LQFP64 – 10 x 10 mm, low-profile quad flat package recommended footprint



1. Dimensions are in millimeters.

7.6 UFBGA176+25, 10 x 10, 0.65 mm ultra thin-pitch ball grid array package information

Figure 93. UFBGA176+25, 10 × 10 × 0.65 mm ultra thin fine-pitch ball grid array package outline



1. Drawing is not to scale.

Table 121. UFBGA176+25, 10 × 10 × 0.65 mm ultra thin fine-pitch ball grid array package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.002	0.0031	0.0043
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
b	0.230	0.280	0.330	0.0091	0.0110	0.0130
D	9.950	10.000	10.050	0.3917	0.3937	0.3957
E	9.950	10.000	10.050	0.3917	0.3937	0.3957
e	-	0.650	-	-	0.0256	-
F	0.400	0.450	0.500	0.0157	0.0177	0.0197
ddd	-	-	0.080	-	-	0.0031
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

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