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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	216MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	138
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f733iet6

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Table 2. STM32F732xx and STM32F733xx features and peripheral counts (continued)

Peripherals	STM32F73xRx	STM32F73xVx	STM32F73xZx	STM32F73xIx
Maximum CPU frequency	216 MHz(7)			
Operating voltage	1.7 to 3.6 V(8)			
Operating temperatures	Ambient temperatures: –40 to +85 °C /–40 to +105 °C			
	Junction temperature: –40 to + 125 °C			
Package	LQFP64(9)	LQFP100(9) WLCSP100(10)	LQFP144 UFBGA144(10)	UFBGA176 LQFP176

1. For the LQFP100 package, only FMC Bank1 is available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select.
2. On the STM32F733xx device packages, except the 176-pin ones, the TIM12 is not available, so there are 9 general-purpose timers.
3. The SPI1, SPI2 and SPI3 interfaces give the flexibility to work in an exclusive way in either the SPI mode or the I2S audio mode.
4. USB OTG HS with the ULPI in the STM32F732xx devices and with integrated HS PHY in the STM32F733xx devices.
5. The SDMMC2 supports a dedicated power rail for clock, command and data 0..4 lines, feature available starting from 144 pin package.
6. The SDMMC2 is not available on the STM32F733Vx devices.
7. 216 MHz maximum frequency for - 40°C to + 85°C ambient temperature range (200 MHz maximum frequency for - 40°C to + 105°C ambient temperature range).
8. V_{DD}/V_{DDA} minimum value of 1.7 V is obtained when the internal reset is OFF (refer to *Section 3.15.2: Internal reset OFF*).
9. Available only on the STM32F732xx devices.
10. Available only on the STM32F733xx devices.

2.2 STM32F733xx versus STM32F732xx LQFP144/LQFP176 packages:

Figure 3. Compatible board design for LQFP144 package

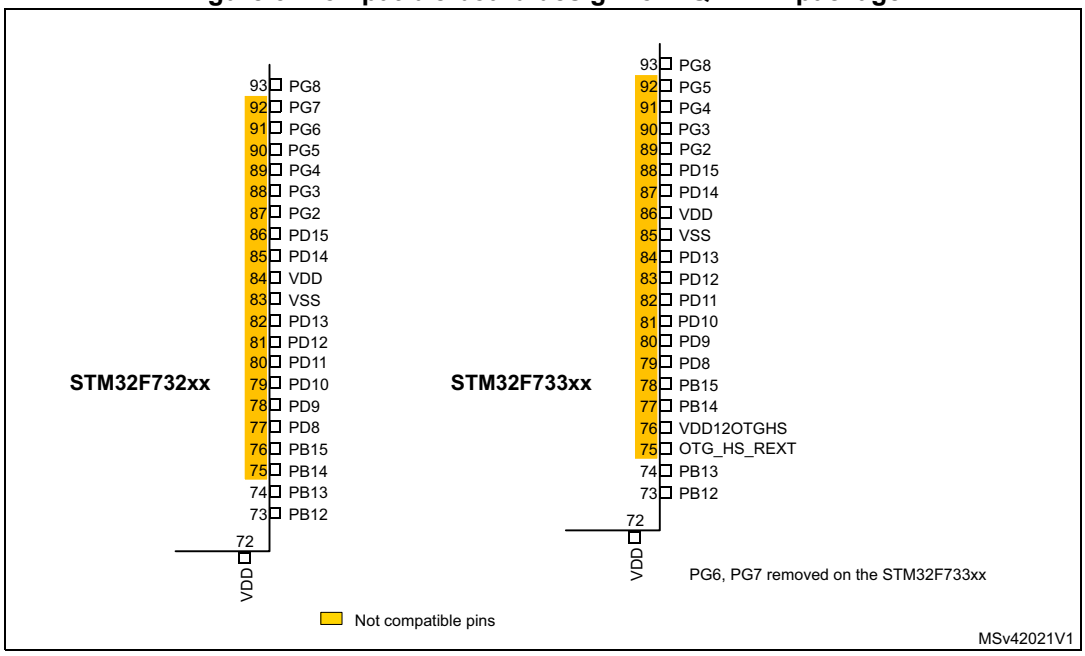


Figure 4. Compatible board design for LQFP176 package

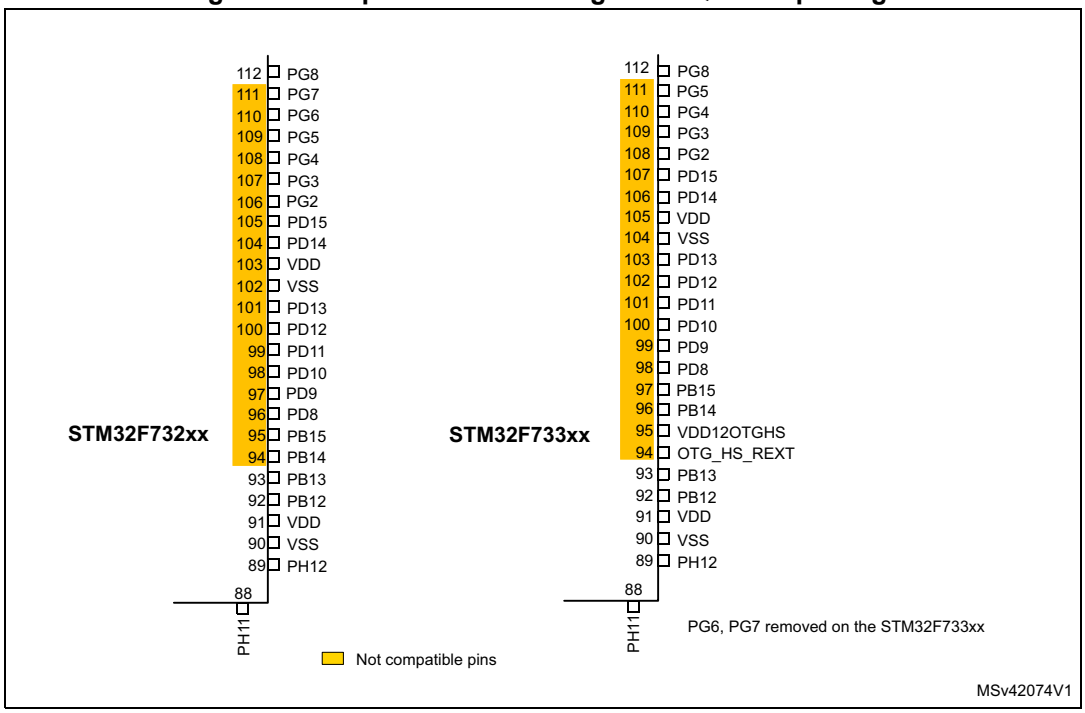


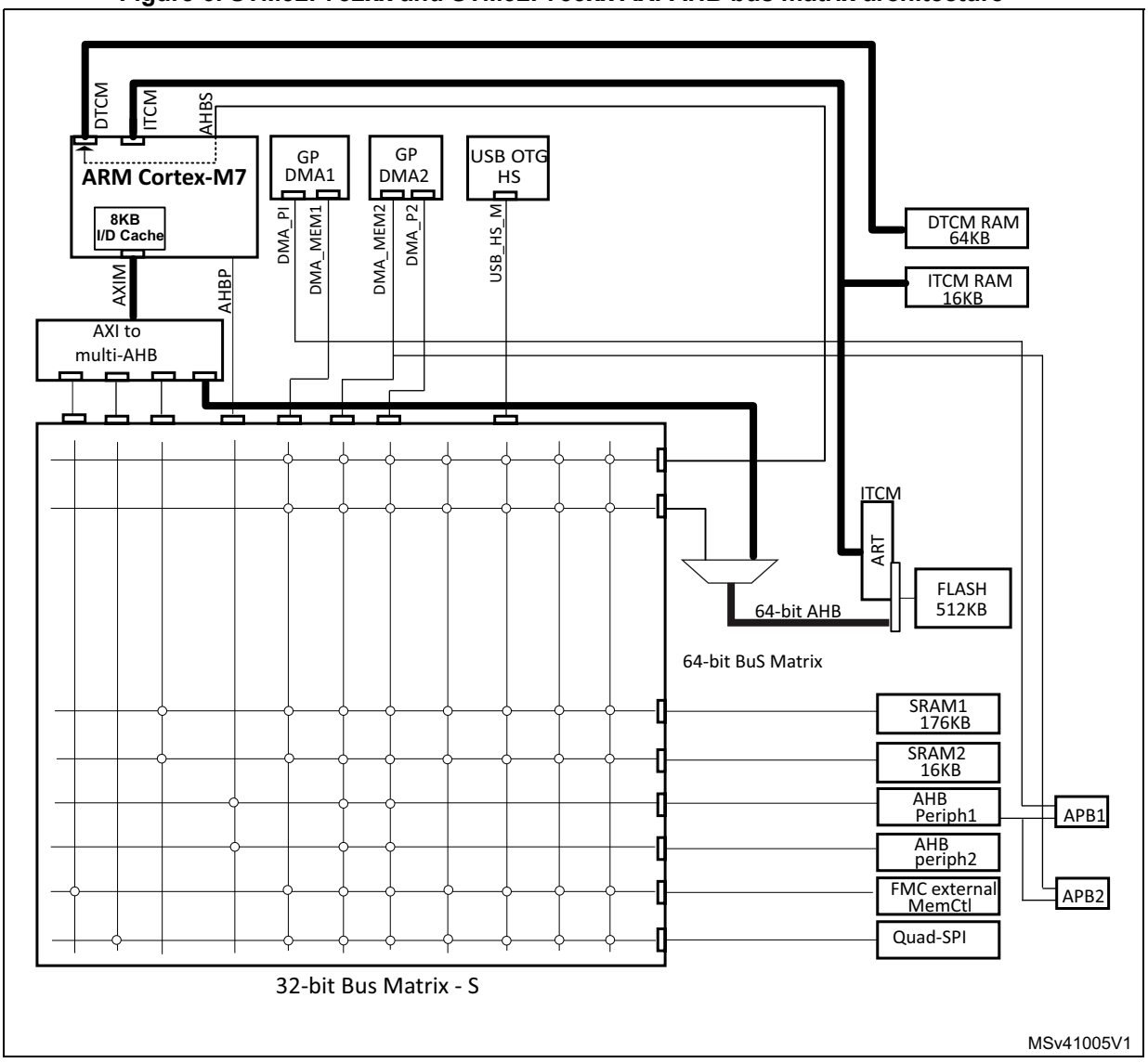
Figure 5 shows the general block diagram of the device family.

3.6 AXI-AHB bus matrix

The STM32F732xx and STM32F733xx system architecture is based on 2 sub-systems:

- An AXI to multi AHB bridge converting AXI4 protocol to AHB-Lite protocol:
  - 3x AXI to 32-bit AHB bridges connected to AHB bus matrix
  - 1x AXI to 64-bit AHB bridge connected to the embedded Flash memory
- A multi-AHB Bus-Matrix
  - The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs, USB HS) and the slaves (Flash memory, RAM, FMC, Quad-SPI, AHB and APB peripherals) and ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

Figure 6. STM32F732xx and STM32F733xx AXI-AHB bus matrix architecture(1)



1. The above figure has large wires for 64-bits bus and thin wires for 32-bits bus.

3.20.4 Low-power timer (LPTIM1)

The low-power timer has an independent clock and is running also in Stop mode if it is clocked by LSE, LSI or an external clock. It is able to wakeup the devices from Stop mode.

This low-power timer supports the following features:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous / one-shot mode
- Selectable software / hardware input trigger
- Selectable clock source:
- Internal clock source: LSE, LSI, HSI or APB clock
- External clock source over LPTIM input (working even with no internal clock source running, used by the Pulse Counter Application)
- Programmable digital glitch filter
- Encoder mode

3.20.5 Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes.

3.20.6 Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.20.7 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard downcounter. It features:

- A 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

Table 10. STM32F732xx and STM32F733xx pin and ball definition (continued)

Pin Number										Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F732xx					STM32F733xx										
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
-	-	20	L3	26	-	L3	G3	20	26	PF8	I/O	FT	-	SPI5_MISO, SAI1_SCK_B, UART7_RTS, TIM13_CH1, QUADSPI_BK1_IO0, EVENTOUT	ADC3_IN6
-	-	21	L2	27	-	L2	G2	21	27	PF9	I/O	FT	-	SPI5_MOSI, SAI1_FS_B, UART7_CTS, TIM14_CH1, QUADSPI_BK1_IO1, EVENTOUT	ADC3_IN7
-	-	22	L1	28	-	L1	G1	22	28	PF10	I/O	FT	-	EVENTOUT	ADC3_IN8
5	12	23	G1	29	G10	G1	D1	23	29	PH0-OSC_IN	I/O	FT	(5)	EVENTOUT	OSC_IN
6	13	24	H1	30	H10	H1	E1	24	30	PH1-OSC_OUT	I/O	FT	(5)	EVENTOUT	OSC_OUT
7	14	25	J1	31	G9	J1	F1	25	31	NRST	I/O	RST	-	-	-
8	15	26	M2	32	F8	M2	H1	26	32	PC0	I/O	FT	(4)	SAI2_FS_B, OTG_HS_ULPI_STP, FMC_SDNWE, EVENTOUT	ADC1_IN10, ADC2_IN10, ADC3_IN10
9	16	27	M3	33	H9	M3	H2	27	33	PC1	I/O	FT	-	TRACED0, SPI2_MOSI/I2S2_SD, SAI1_SD_A, EVENTOUT	ADC1_IN11, ADC2_IN11, ADC3_IN11, RTC_TAMP3, WKUP3

Table 12. STM32F732xx and STM32F733xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11/LPTIM1	I2C1/2/3/USART1	SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5	SPI2/I2S2/SPI3/I2S3/SPI3/I2S3/SAI1/UART4	SPI2/I2S2/SPI3/I2S3/USART1/2/3/UART5	SAI2/USART6/UART4/5/7/8/OTG1_FS	CAN1/TIM12/13/14/QUADSPI/FMC/OTG2_HS	SAI2/QUADSPI/SDMMC2/OTG2_HS/OTG1_FS	SDMMC2	UART7/FMC/SDMMC1/OTG2_FS	SYS
Port I	PI7	-	-	-	TIM8_CH3	-	-	-	-	-	-	SAI2_FS_A	-	FMC_D29	EVENTOUT
	PI8	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PI9	-	-	-	-	-	-	-	-	UART4_RX	CAN1_RX	-	-	FMC_D30	EVENTOUT
	PI10	-	-	-	-	-	-	-	-	-	-	-	-	FMC_D31	EVENTOUT
	PI11	-	-	-	-	-	-	-	-	-	-	OTG_HS_ULPI_DIR	-	-	EVENTOUT
	PI12	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PI13	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PI14	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PI15	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT

Table 15. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	− 65 to +150	°C
T_J	Maximum junction temperature	125	

6.3 Operating conditions

6.3.1 General operating conditions

Table 16. General operating conditions

Symbol	Parameter	Conditions[1]		Min	Typ	Max	Unit
f_{HCLK}	Internal AHB clock frequency	Power Scale 3 (VOS[1:0] bits in PWR_CR register = 0x01), Regulator ON, over-drive OFF		0	-	144	MHz
		Power Scale 2 (VOS[1:0] bits in PWR_CR register = 0x10), Regulator ON	Over-drive OFF	0	-	168	
			Over-drive ON		-	180	
		Power Scale 1 (VOS[1:0] bits in PWR_CR register= 0x11), Regulator ON	Over-drive OFF	0	-	180	
			Over-drive ON		-	216[2]	
f_{PCLK1}	Internal APB1 clock frequency	Over-drive OFF		0	-	45	
		Over-drive ON		0	-	54	
f_{PCLK2}	Internal APB2 clock frequency	Over-drive OFF		0	-	90	
		Over-drive ON		0	-	108	
V_{DD}	Standard operating voltage	-		1.7[3]	-	3.6	V
V_{DDA}[4][5]	Analog operating voltage (ADC limited to 1.2 M samples)	Must be the same potential as V_{DD}[6]		1.7[3]	-	2.4	
	Analog operating voltage (ADC limited to 2.4 M samples)			2.4	-	3.6	
V_{DDUSB}	USB supply voltage (supply voltage for PA11,PA12, PB14 and PB15 pins)	USB not used		1.7	3.3	3.6	
		USB used		3.0	-	3.6	
V_{BAT}	Backup operating voltage	-		1.65	-	3.6	
$V_{DDSDMMC}$	SDMMC2 supply voltage (supply voltage for PG[12:9] and PD6 pins)	It can be different from V_{DD}		1.7	-	3.6	

Table 27. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory on ITCM interface (ART disabled), regulator ON

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)			Unit
					TA= 25 °C	TA=85 °C	TA=105 °C	
I_{DD}	Supply current in RUN mode	All peripherals enabled(2)(3)	216	138	151	174.7	184	mA
			200	133	141	164.3	174	
			180	110	131	149.2	159	
			168	99	117	134	144	
			144	79	98	111.7	121	
			60	49	53	64	75	
			25	27	30	38.3	48	
		All peripherals disabled(3)	216	82	96	119.5	131	
			200	81	89	113.1	124	
			180	65	85	103.1	114	
			168	58	76	93.2	104	
			144	48	67	80.4	91	
			60	33	36	49.7	60	
			25	18	21	31.1	41	

1. Guaranteed by characterization results.
2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.
3. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.73 mA per ADC for the analog part.

Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard I/O. The external clock signal has to respect the *Table 61: I/O static characteristics*. However, the recommended clock input waveform is shown in *Figure 36*.

The characteristics given in *Table 39* result from tests performed using an low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 16*.

Table 39. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User External clock source frequency(1)	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	-	$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{f(LSE)}$	OSC32_IN high or low time(1)		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time(1)		-	-	50	
$C_{in(LSE)}$	OSC32_IN input capacitance(1)	-	-	5	-	pF
$DuCy_{(LSE)}$	Duty cycle	-	30	-	70	%
I_L	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA

1. Guaranteed by design.

Figure 35. High-speed external clock source AC timing diagram

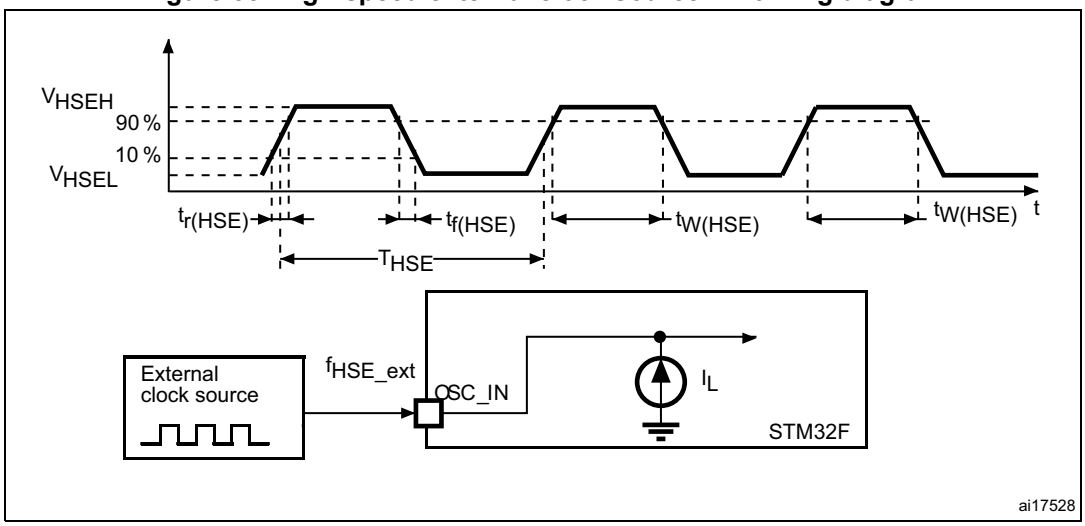
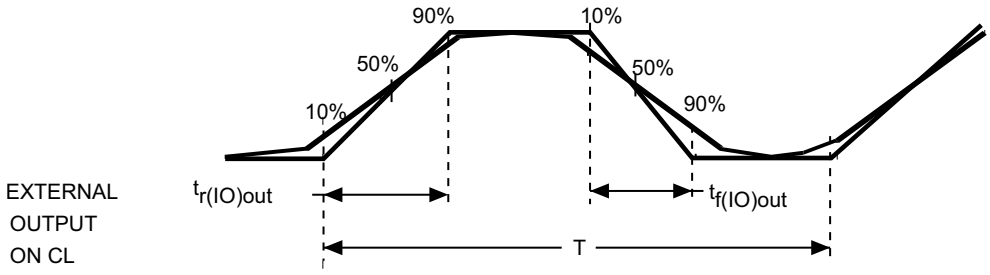


Table 63. I/O AC characteristics(1)(2) (continued)

OSPEEDRy [1:0] bit value(1)	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
11	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 30 pF, V_{DD} ≥ 2.7 V	-	-	100(4)	MHz
			C_L = 30 pF, V_{DD} ≥ 1.8 V	-	-	50	
			C_L = 30 pF, V_{DD} ≥ 1.7 V	-	-	42.5	
			C_L = 10 pF, V_{DD}≥ 2.7 V	-	-	180(4)	
			C_L = 10 pF, V_{DD} ≥ 1.8 V	-	-	100	
			C_L = 10 pF, V_{DD} ≥ 1.7 V	-	-	72.5	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 30 pF, V_{DD} ≥ 2.7 V	-	-	4	ns
			C_L = 30 pF, V_{DD} ≥1.8 V	-	-	6	
			C_L = 30 pF, V_{DD} ≥1.7 V	-	-	7	
			C_L = 10 pF, V_{DD} ≥ 2.7 V	-	-	2.5	
			C_L = 10 pF, V_{DD} ≥1.8 V	-	-	3.5	
			C_L = 10 pF, V_{DD} ≥1.7 V	-	-	4	
-	tEXTIpw	Pulse width of external signals detected by the EXTI controller	-	10	-	-	ns

1. Guaranteed by design.
2. The I/O speed is configured using the OSPEEDRy[1:0] bits. Refer to the STM32F72xxx and STM32F73xxx reference manual for a description of the GPIOx_SPEEDR GPIO port output speed register.
3. The maximum frequency is defined in *Figure 44*.
4. For maximum frequencies above 50 MHz and V_{DD} > 2.4 V, the compensation cell should be used.

Figure 44. I/O AC characteristics definition



Maximum frequency is achieved if (t_r + t_f) ≤ (2/3)T and if the duty cycle is (45-55%) when loaded by CL specified in the table " *I/O AC characteristics*".

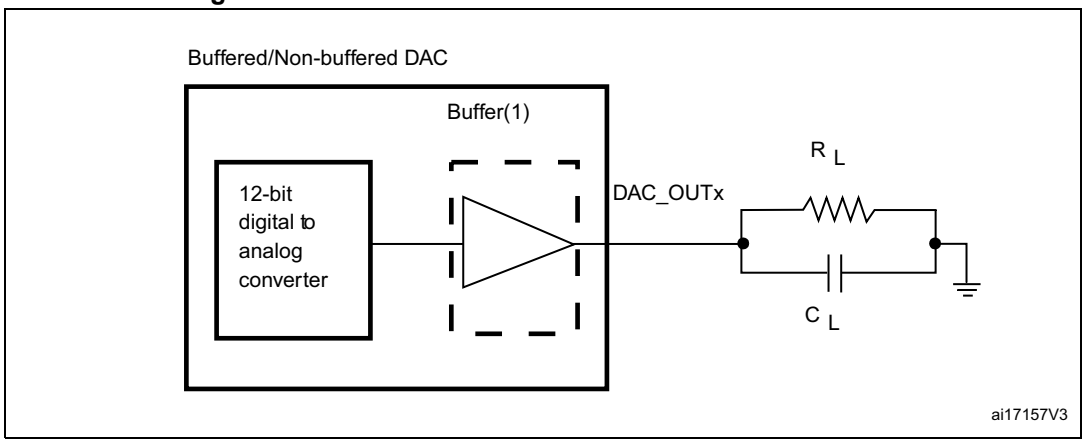
ai14131d

Table 78. DAC characteristics (continued)

Symbol	Parameter	Min	Typ	Max	Unit	Comments
t_{WAKEUP} (4)	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	-	6.5	10	µs	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ input code between lowest and highest possible ones.
PSRR+ (2)	Power supply rejection ratio (to V_{DDA}) (static DC measurement)	-	–67	–40	dB	No R_{LOAD}, C_{LOAD} = 50 pF

1. V_{DDA} minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to *Section 3.15.2: Internal reset OFF*).
2. Guaranteed by design.
3. The quiescent mode corresponds to a state where the DAC maintains a stable output level to ensure that no dynamic consumption occurs.
4. Guaranteed by characterization results.

Figure 50. 12-bit buffered /non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

6.3.29 Communications interfaces

I²C interface characteristics

The I²C interface meets the timings requirements of the I²C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s.
- Fast-mode Plus (Fm+): with a bit rate up to 1Mbit/s.

The I²C timings requirements are guaranteed by design when the I2C peripheral is properly configured (refer to RM0385 reference manual) and when the I2CCLK frequency is greater than the minimum shown in the table below:

USB OTG full speed (FS) characteristics

This interface is present in both the USB OTG HS and USB OTG FS controllers.

Table 84. USB OTG full speed startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB OTG full speed transceiver startup time	1	µs

1. Guaranteed by design.

Table 85. USB OTG full speed DC electrical characteristics

Symbol		Parameter	Conditions	Min.(1)	Typ.	Max.(1)	Unit
Input levels	V_{DDUSB}	USB OTG full speed transceiver operating voltage	-	3.0(2)	-	3.6	V
	V_{DI}(3)	Differential input sensitivity	I(USB_FS_DP/DM, USB_HS_DP/DM)	0.2	-	-	V
	V_{CM}(3)	Differential common mode range	Includes V_{DI} range	0.8	-	2.5	
	V_{SE}(3)	Single ended receiver threshold	-	1.3	-	2.0	
Output levels	V_{OL}	Static output level low	R_L of 1.5 kΩ to 3.6 V(4)	-	-	0.3	V
	V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}(4)	2.8	-	3.6	
R_{PD}		PA11, PA12 (USB_FS_DP/DM)	V_{IN} = V_{DD}	14.25	-	24.8	kΩ
		PA9, PB13 (OTG_FS_VBUS, OTG_HS_VBUS)	V_{IN} = V_{DD}	2.4	5.2	8	
R_{PU}		PA12 (USB_FS_DP)	V_{IN} = V_{SS}, during idle	0.9	1.25	1.575	
		PA9, PB13 (OTG_FS_VBUS, OTG_HS_VBUS)	V_{IN} = V_{SS}, during reception	0.55	0.95	1.35	

1. All the voltages are measured from the local ground potential.
2. The USB OTG full speed transceiver functionality is ensured down to 2.7 V but not the full USB full speed electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DDUSB} voltage range.
3. Guaranteed by design.
4. R_L is the load connected on the USB OTG full speed drivers.

Note: When VBUS sensing feature is enabled, PA9 and PB13 should be left at their default state (floating input), not as alternate function. A typical 200 µA current consumption of the sensing block (current to voltage conversion to determine the different sessions) can be observed on PA9 and PB13 when the feature is enabled.

Table 89. Dynamic characteristics: USB ULPI(1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{SC}	Control in (ULPI_DIR, ULPI_NXT) setup time	-	1.5	-	-	ns
t_{HC}	Control in (ULPI_DIR, ULPI_NXT) hold time	-	1	-	-	
t_{SD}	Data in setup time	-	1.5	-	-	
t_{HD}	Data in hold time	-	1	-	-	
t_{DC}/t_{DD}	Data/control output delay	2.7 V < V_{DD} < 3.6 V, C_L = 20 pF and OSPEEDRy[1:0] = 11	-	6	7.5	
		-	-	9.5	11	
		1.7 V < V_{DD} < 3.6 V, C_L = 15 pF and OSPEEDRy[1:0] = 11	-			

1. Guaranteed by characterization results.

USB high speed (HS) characteristics (Embedded PHY High speed in STM32F733xx devices)

Table 90. USB OTG high speed DC electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{hssq}	High speed squelch detection threshold	-	100	-	150	mV
V_{hsdsc}	High speed disconnect detection threshold	-	525	-	625	mV
V_{hsdif}	High speed differential detection threshold	-	100	-	-	mV
V_{hscm}	High speed data signalling common mode voltage range	-	-50	-	500	mV
V_{hsoi}	High speed idle level	-	-10	-	10	mV
V_{hsoh}	High speed data signaling high	-	360	-	440	mV
V_{hsol}	High speed data signaling low	-	-10	-	10	mV
V_{chirpj}	Chirp J level	-	700	-	1100	mV
V_{chirpk}	Chirp K level	-	-900	-	-500	mV

Table 91. USB OTG high speed electrical characteristics

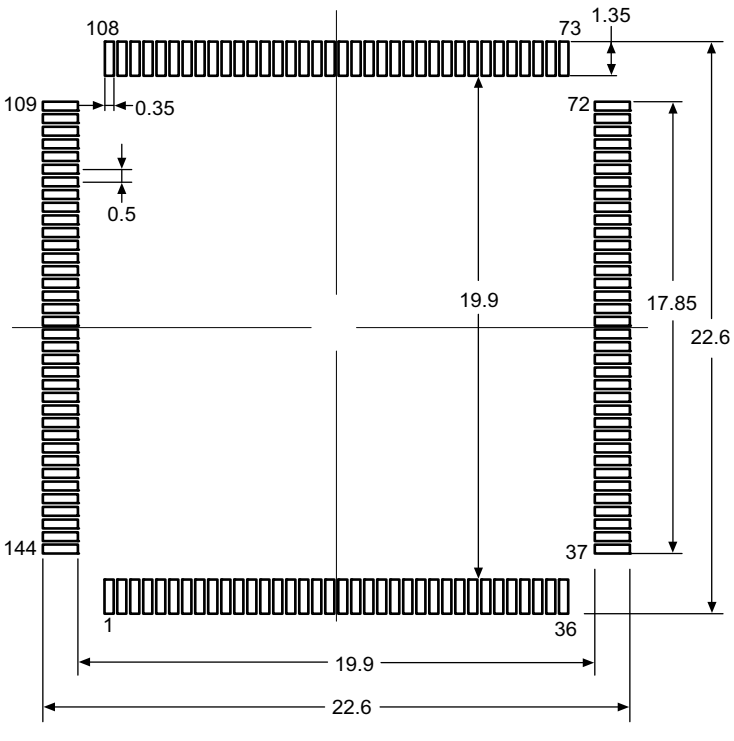
Parameter	Comments	Conditions	Min	Typ	Max	Unit
t_{lr}	Rise time	-	0.5	-	-	ns
t_{lf}	Fall time	-	0.5	-	-	ns
t_{lrfm}	Setup time from INHSDRIVERENABLE=1 to the transition on INHSDATAP/INHSDATAN	-	10	-	-	ns
Z_{drv}	Driver output impedance	-	40.5	-	49.5	Ω

Table 117. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3	-	17.500	-	-	0.689	-
E	21.800	22.000	22.200	0.8583	0.8661	0.8740
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3	-	17.500	-	-	0.6890	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

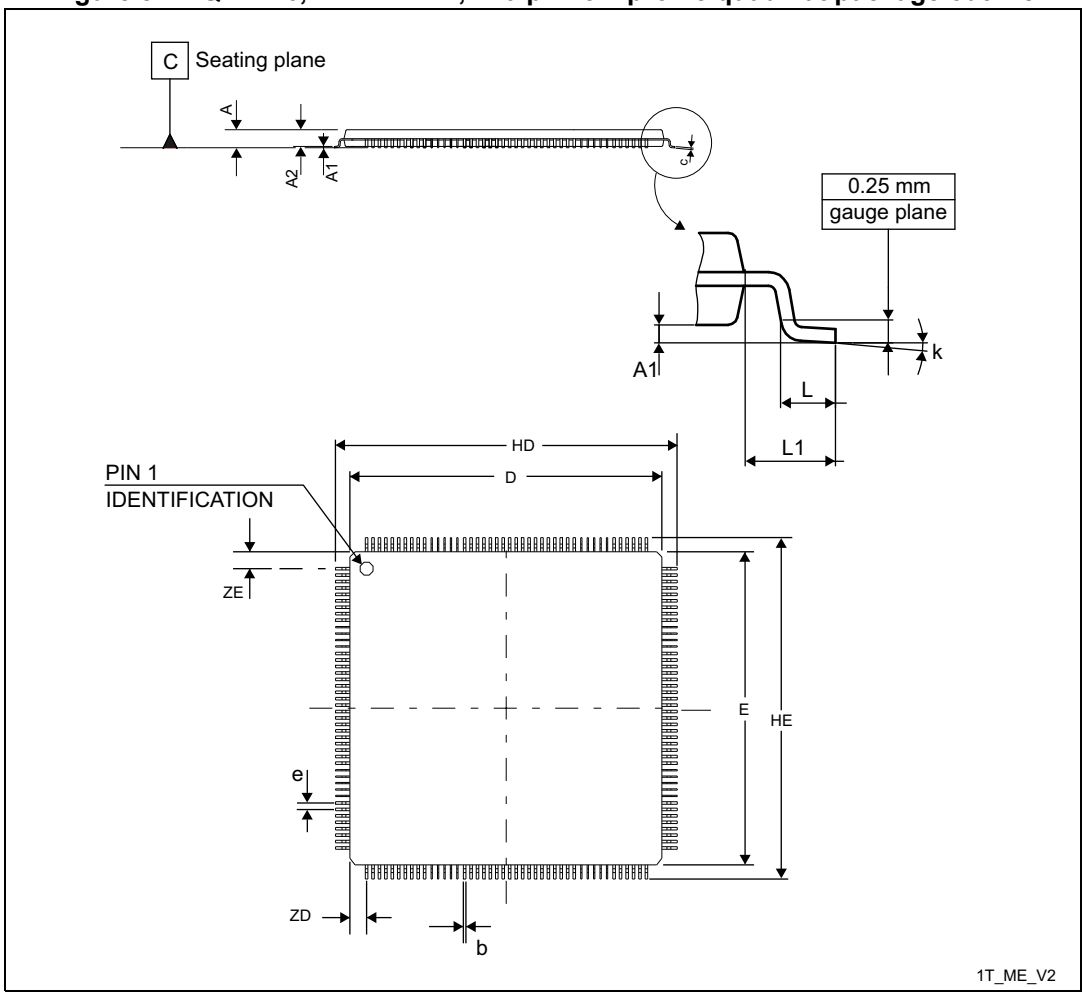
Figure 85. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

7.4 LQFP176 24 x 24 mm low-profile quad flat package information

Figure 87. LQFP176, 24 x 24 mm, 176-pin low-profile quad flat package outline



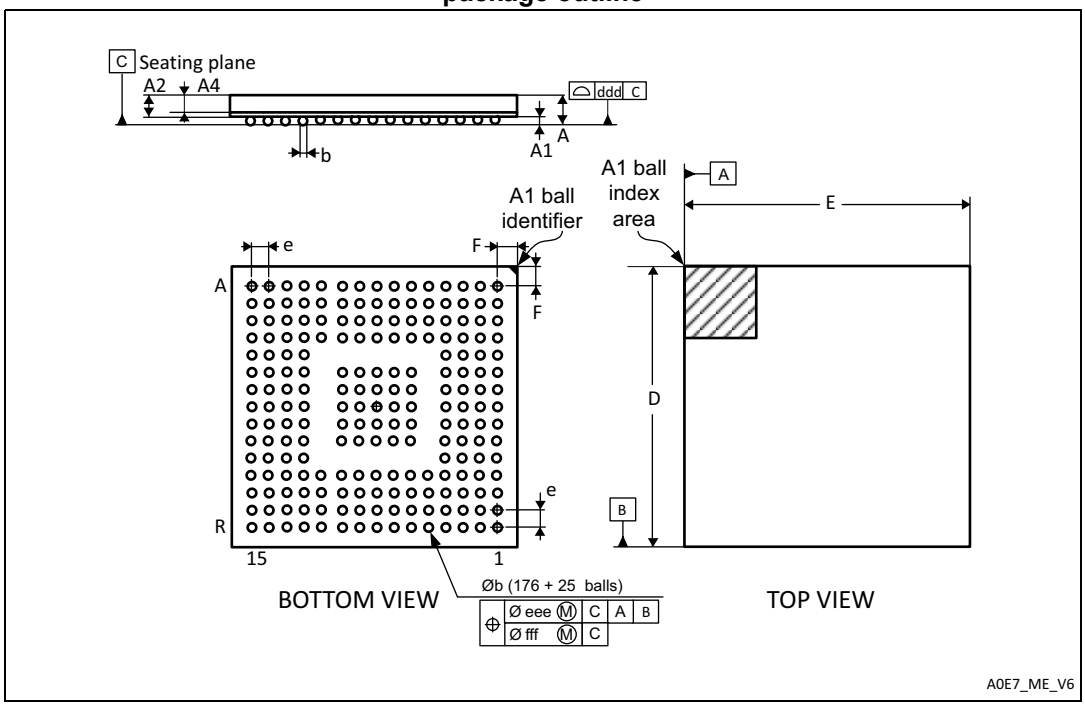
1. Drawing is not to scale.

Table 118. LQFP176, 24 x 24 mm, 176-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	-	1.450	0.0531	-	0.0060
b	0.170	-	0.270	0.0067	-	0.0106
C	0.090	-	0.200	0.0035	-	0.0079
D	23.900	-	24.100	0.9409	-	0.9488

7.6 UFBGA176+25, 10 x 10, 0.65 mm ultra thin-pitch ball grid array package information

Figure 93. UFBGA176+25, 10 × 10 × 0.65 mm ultra thin fine-pitch ball grid array package outline



1. Drawing is not to scale.

Table 121. UFBGA176+25, 10 × 10 × 0.65 mm ultra thin fine-pitch ball grid array package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.002	0.0031	0.0043
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
b	0.230	0.280	0.330	0.0091	0.0110	0.0130
D	9.950	10.000	10.050	0.3917	0.3937	0.3957
E	9.950	10.000	10.050	0.3917	0.3937	0.3957
e	-	0.650	-	-	0.0256	-
F	0.400	0.450	0.500	0.0157	0.0177	0.0197
ddd	-	-	0.080	-	-	0.0031
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.080	-	-	0.0031

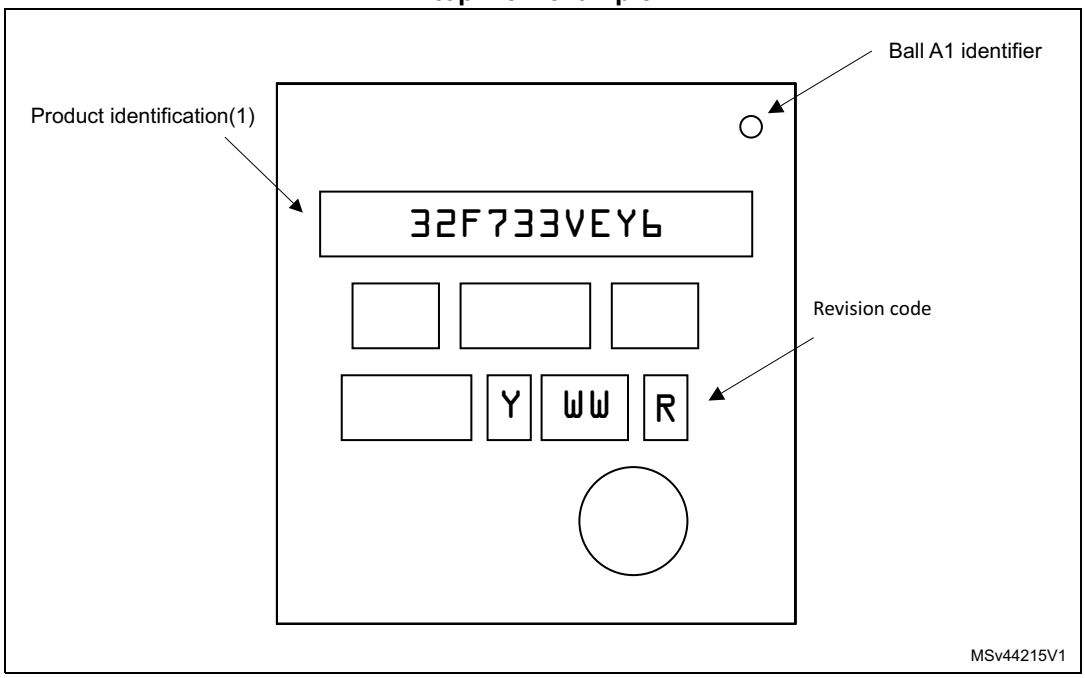
1. Values in inches are converted from mm and rounded to 4 decimal digits.

WLCSP100 device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 98. WLCSP100 – 100L, 4.166 x 4.628 mm 0.4 mm pitch top view example



1. Parts marked as ES or E or accompanied by an engineering sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.8 Thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

T_J max = T_A max + (P_D max x Θ_{JA})

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$P_{I/O}$ max = Σ (V_{OL} × I_{OL}) + Σ((V_{DD} – V_{OH}) × I_{OH}),

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 125. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP64 - 10 × 10 mm / 0.5 mm pitch	48.5	°C/W
	Thermal resistance junction-ambient LQFP100 - 14× 14 mm / 0.5 mm pitch	47.1	
	Thermal resistance junction-ambient WLCSP100 - 0.4 mm pitch	35.85	
	Thermal resistance junction-ambient LQFP144 - 20 × 20 mm / 0.5 mm pitch	45.6	
	Thermal resistance junction-ambient LQFP176 - 24 × 24 mm / 0.5 mm pitch	43.9	
	Thermal resistance junction-ambient UFBGA144 - 7 × 7 mm / 0.5 mm pitch	42	
	Thermal resistance junction-ambient UFBGA176 - 10× 10 mm / 0.5 mm pitch	41.2	

Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

Revision history

Table 128. Document revision history

Date	Revision	Changes
03-Feb-2017	1	Initial release.
30-Mar-2017	2	Updated cover with the maximum SPI speed at 54 Mbit/s. Updated *Figure 14: STM32F732xx LQFP64 pinout*.
01-Jun-2017	3	Updated *Figure 16: STM32F733xx WLCSP100 ballout (with OTG PHY HS)*. Updated note 1 below all the package device marking figures. Updated *Section 1: Introduction*. Updated *Table 60: I/O current injection susceptibility* note by 'injection is not possible'. Updated *Table 67: ADC characteristics* R_{ADC} min at 1.5 Kohm. Updated *Figure 45: Recommended NRST pin protection* note about the 0.1uF capacitor. Updated *Table 78: DAC characteristics* R_{LOAD} feature. Updated *Figure 39: ACCHSI versus temperature*.
10-Apr-2018	4	Added *Section 1: Introduction*. Removed memory mapping, transferred in the reference manual (RM0431). Updated *Table 10: STM32F732xx and STM32F733xx pin and ball definition* footnote 5 only for PC14, PC15, PH0, PH1. Updated *Table 125: Package thermal characteristics* thermal values for LQFP packages.