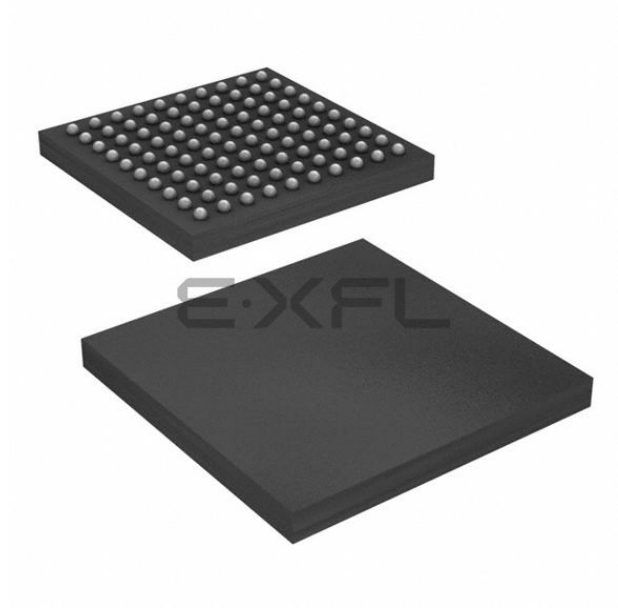

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	216MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	79
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-UFBGA, WLCSP
Supplier Device Package	100-WLCSP (4.2x4.7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f733vey6tr

2.2 STM32F733xx versus STM32F732xx LQFP144/LQFP176 packages:

Figure 3. Compatible board design for LQFP144 package

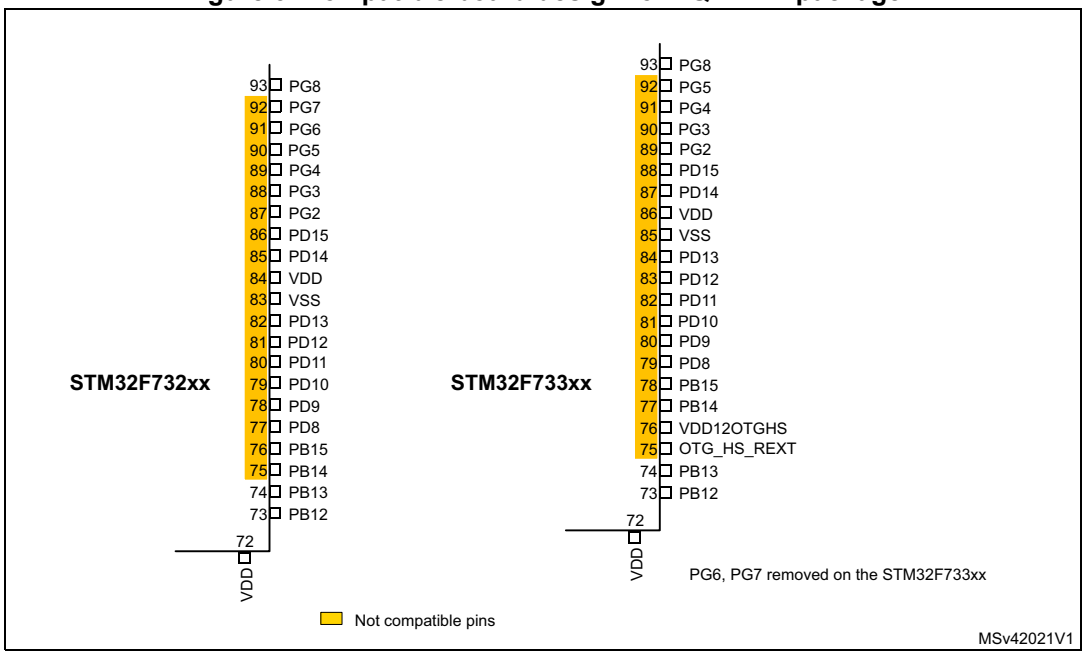


Figure 4. Compatible board design for LQFP176 package

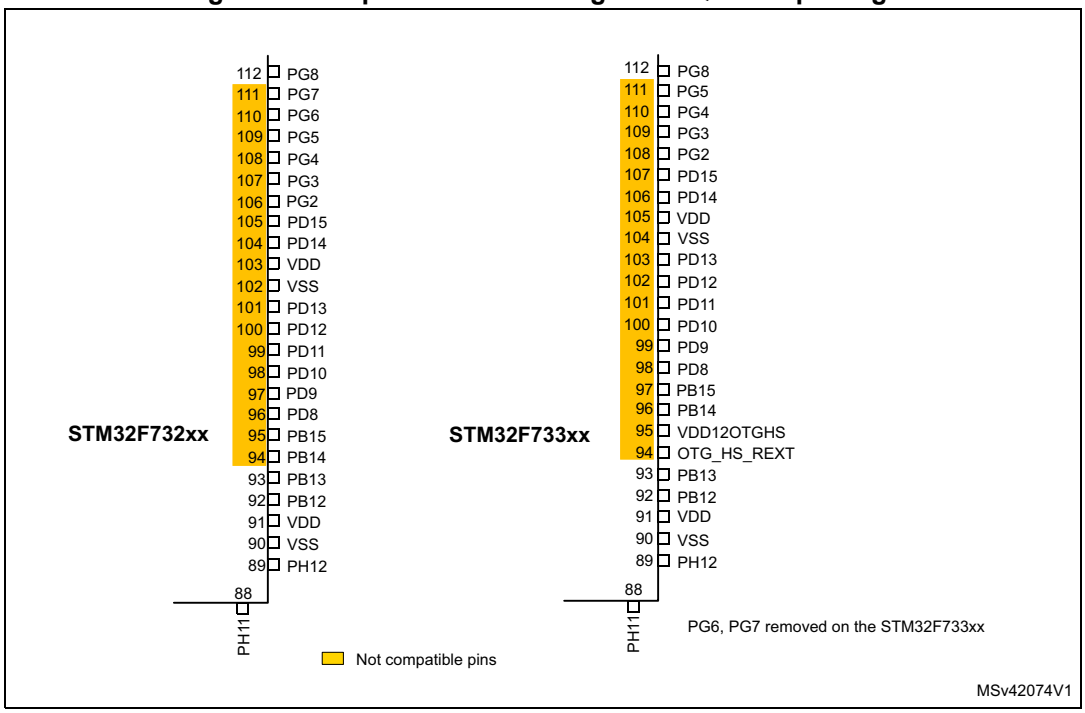
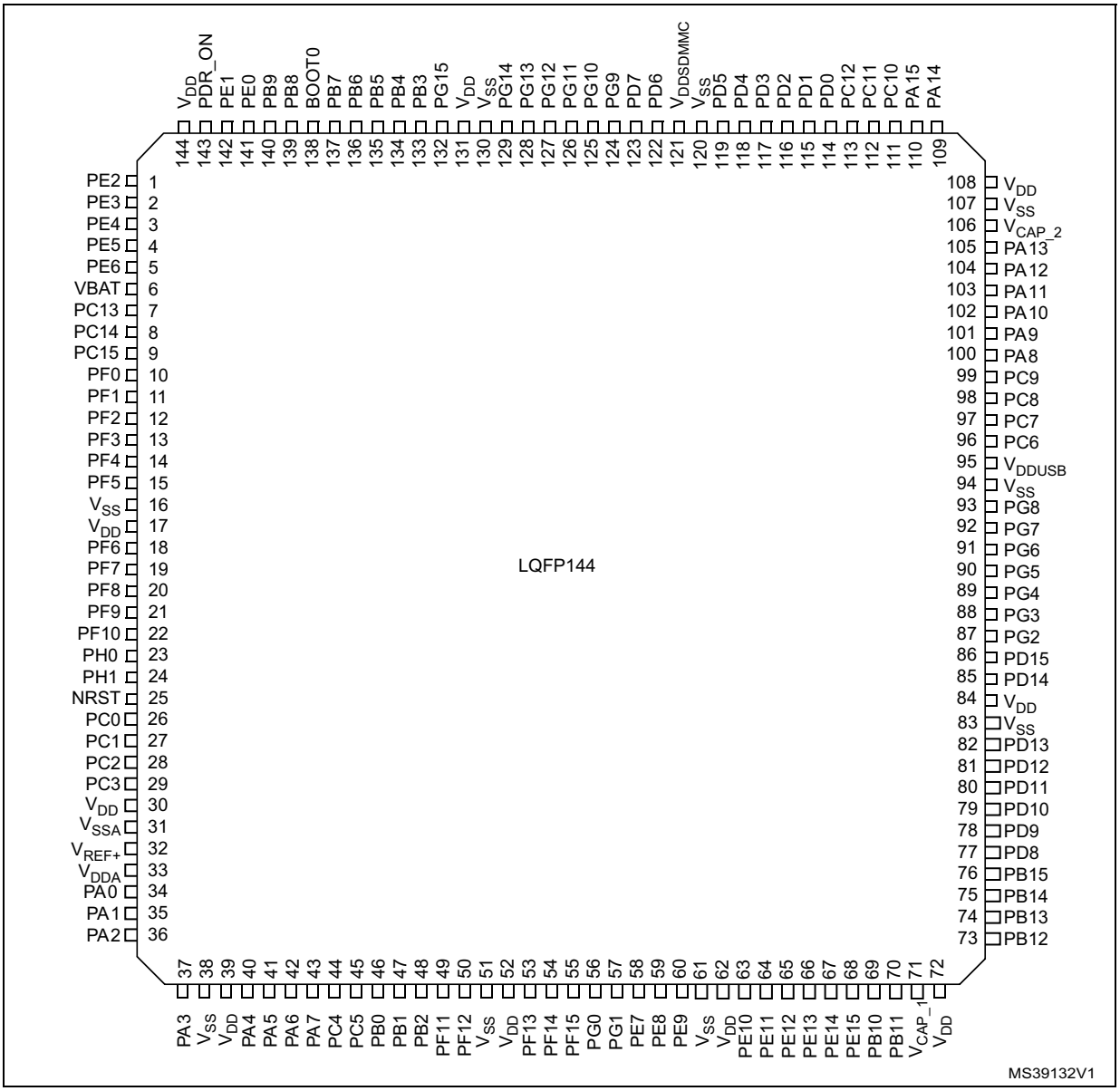


Figure 5 shows the general block diagram of the device family.

Figure 17. STM32F732xx LQFP144 pinout



1. The above figure shows the package top view.

Table 10. STM32F732xx and STM32F733xx pin and ball definition (continued)

Pin Number										Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F732xx					STM32F733xx										
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
-	73	106	F13	125	B3	F13	G9	106	125	VCAP_2	S	-	-	-	-
47	74	107	F12	126	A2	F12	G10	107	126	VSS	S	-	-	-	-
48	75	108	G13	127	A1	G13	F9	108	127	VDD	S	-	-	-	-
-	-	-	E12	128	-	E12	-	-	128	PH13	I/O	FT	-	TIM8_CH1N, UART4_TX, CAN1_TX, FMC_D21, EVENTOUT	-
-	-	-	E13	129	-	E13	-	-	129	PH14	I/O	FT	-	TIM8_CH2N, UART4_RX, CAN1_RX, FMC_D22, EVENTOUT	-
-	-	-	D13	130	-	D13	-	-	130	PH15	I/O	FT	-	TIM8_CH3N, FMC_D23, EVENTOUT	-
-	-	-	E14	131	-	E14	-	-	131	PI0	I/O	FT	-	TIM5_CH4, SPI2_NSS/I2S2_WS, FMC_D24, EVENTOUT	-
-	-	-	D14	132	-	D14	-	-	132	PI1	I/O	FT	-	TIM8_BKIN2, SPI2_SCK/I2S2_CK, FMC_D25, EVENTOUT	-
-	-	-	C14	133	-	C14	-	-	133	PI2	I/O	FT	-	TIM8_CH4, SPI2_MISO, FMC_D26, EVENTOUT	-
-	-	-	C13	134	-	C13	-	-	134	PI3	I/O	FT	-	TIM8_ETR, SPI2_MOSI/I2S2_SD, FMC_D27, EVENTOUT	-
-	-	-	D9	135	-	D9	-	-	135	VSS	S	-	-	-	-

Table 12. STM32F732xx and STM32F733xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11/LPTIM1	I2C1/2/3/USART1	SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5	SPI2/I2S2/SPI3/I2S3/SPI3/I2S3/SAI1/UART4	SPI2/I2S2/SPI3/I2S3/USART1/2/3/UART5	SAI2/USART6/UART4/5/7/8/OTG1_FS	CAN1/TIM12/13/14/QUADSPI/FMC/OTG2_HS	SAI2/QUADSPI/SDMMC2/OTG2_HS/OTG1_FS	SDMMC2	UART7/FMC/SDMMC1/OTG2_FS	SYS
Port A	PA12	-	TIM1_ETR	-	-	-	-	-	USART1_RTS	SAI2_FS_B	CAN1_TX	OTG_FS_DP	-	-	EVENTOUT
	PA13	JTMS-SWDIO	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PA14	JTCK-SWCLK	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PA15	JTDI	TIM2_CH1/TIM2_ETR	-	-	-	SPI1_NSS/I2S1_WS	SPI3_NSS/I2S3_WS	-	UART4_RTS	-	-	-	-	EVENTOUT
Port B	PB0	-	TIM1_CH2N	TIM3_CH3	TIM8_CH2N	-	-	-	-	UART4_CTS	-	OTG_HS_ULPI_D1	-	-	EVENTOUT
	PB1	-	TIM1_CH3N	TIM3_CH4	TIM8_CH3N	-	-	-	-	-	-	OTG_HS_ULPI_D2	-	-	EVENTOUT
	PB2	-	-	-	-	-	-	SAI1_SD_A	SPI3_MOSI/I2S3_SD	-	QUADSPI_CLK	-	-	-	EVENTOUT
	PB3	JTDO/TRACESWO	TIM2_CH2	-	-	-	SPI1_SCK/I2S1_CK	SPI3_SCK/I2S3_CK	-	-	-	SDMMC2_D2	-	-	EVENTOUT
	PB4	NJTRST	-	TIM3_CH1	-	-	SPI1_MISO	SPI3_MISO	SPI2_NSS/I2S2_WS	-	-	SDMMC2_D3	-	-	EVENTOUT
	PB5	-	-	TIM3_CH2	-	I2C1_SMBA	SPI1_MOSI/I2S1_SD	SPI3_MOSI/I2S3_SD	-	-	-	OTG_HS_ULPI_D7	-	FMC_SDCKE1	EVENTOUT
	PB6	-	-	TIM4_CH1	-	I2C1_SCL	-	-	USART1_TX	-	-	QUADSPI_BK1_NCS	-	FMC_SDNE1	EVENTOUT
	PB7	-	-	TIM4_CH2	-	I2C1_SDA	-	-	USART1_RX	-	-	-	-	FMC_NL	EVENTOUT
	PB8	-	-	TIM4_CH3	TIM10_CH1	I2C1_SCL	-	-	-	-	CAN1_RX	SDMMC2_D4	-	SDMMC1_D4	EVENTOUT

Table 12. STM32F732xx and STM32F733xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11/LPTIM1	I2C1/2/3/USART1	SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5	SPI2/I2S2/SPI3/I2S3/SPI3/I2S3/SAI1/UART4	SPI2/I2S2/SPI3/I2S3/USART1/2/3/UART5	SAI2/USART6/UART4/5/7/8/OTG1_FS	CAN1/TIM12/13/14/QUADSPI/FMC/OTG2_HS	SAI2/QUADSPI/SDMMC2/OTG2_HS/OTG1_FS	SDMMC2	UART7/FMC/SDMMC1/OTG2_FS	SYS
Port G	PG0	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A10	EVENTOUT
	PG1	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A11	EVENTOUT
	PG2	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A12	EVENTOUT
	PG3	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A13	EVENTOUT
	PG4	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A14/FMC_BA0	EVENTOUT
	PG5	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A15/FMC_BA1	EVENTOUT
	PG6	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PG7	-	-	-	-	-	-	-	-	USART6_CK	-	-	-	FMC_INT	EVENTOUT
	PG8	-	-	-	-	-	-	-	-	USART6_RTS	-	-	-	FMC_SDCLK	EVENTOUT
	PG9	-	-	-	-	-	-	-	-	USART6_RX	QUADSPI_BK2_IO2	SAI2_FS_B	SDMMC2_D0	FMC_NE2/FMC_NCE	EVENTOUT
	PG10	-	-	-	-	-	-	-	-	-	-	SAI2_SD_B	SDMMC2_D1	FMC_NE3	EVENTOUT

Table 12. STM32F732xx and STM32F733xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11/LPTIM1	I2C1/2/3/USART1	SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5	SPI2/I2S2/SPI3/I2S3/SPI3/I2S3/SAI1/UART4	SPI2/I2S2/SPI3/I2S3/USART1/2/3/UART5	SAI2/USART6/UART4/5/7/8/OTG1_FS	CAN1/TIM12/13/14/QUADSPI/FMC/OTG2_HS	SAI2/QUADSPI/SDMMC2/OTG2_HS/OTG1_FS	SDMMC2	UART7/FMC/SDMMC1/OTG2_FS	SYS
Port G	PG11	-	-	-	-	-	-	-	-	-	-	SDMMC2_D2	-	-	EVENTOUT
	PG12	-	-	-	LPTIM1_IN1	-	-	-	-	USART6_RTS	-	-	SDMMC2_D3	FMC_NE4	EVENTOUT
	PG13	TRACED0	-	-	LPTIM1_OUT	-	-	-	-	USART6_CTS	-	-	-	FMC_A24	EVENTOUT
	PG14	TRACED1	-	-	LPTIM1_ETR	-	-	-	-	USART6_TX	QUADSPI_BK2_IO3	-	-	FMC_A25	EVENTOUT
	PG15	-	-	-	-	-	-	-	-	USART6_CTS	-	-	-	FMC_SDNCAS	EVENTOUT
Port H	PH0	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PH1	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PH2	-	-	-	LPTIM1_IN2	-	-	-	-	-	QUADSPI_BK2_IO0	SAI2_SCK_B	-	FMC_SDCKE0	EVENTOUT
	PH3	-	-	-	-	-	-	-	-	-	QUADSPI_BK2_IO1	SAI2_MCK_B	-	FMC_SDNE0	EVENTOUT
	PH4	-	-	-	-	I2C2_SCL	-	-	-	-	-	OTG_HS_ULPI_NXT	-	-	EVENTOUT
	PH5	-	-	-	-	I2C2_SDA	SPI5_NSS	-	-	-	-	-	-	FMC_SDNWE	EVENTOUT
	PH6	-	-	-	-	I2C2_SMBA	SPI5_SCK	-	-	-	TIM12_CH1	-	-	FMC_SDNE1	EVENTOUT
	PH7	-	-	-	-	I2C3_SCL	SPI5_MISO	-	-	-	-	-	-	FMC_SDCKE1	EVENTOUT

5 Memory mapping

Refer to the product line reference manual for details on the memory mapping as well as the boundary addresses for all peripherals.

Table 26. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory or SRAM on AXI (L1-cache disabled), regulator ON

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)			Unit
					TA= 25 °C	TA=85 °C	TA=105 °C	
I_{DD}	Supply current in RUN mode	All peripherals enabled(2)(3)	216	129.3	137.6	162.8	173	mA
			200	122	128	153.2	163.3	
			180	108	117	136.4	146	
			168	99	104.5	122.3	132	
			144	80	84.7	99.3	109.2	
			60	42	45	59.5	70	
			25	23	23.4	37.8	48	
		All peripherals disabled(3)	216	73.3	82.3	107.4	119	
			200	70	77	101.8	113.5	
			180	62	71	90.2	101	
			168	59	63.6	81.4	92.1	
			144	49	53.3	67.9	79	
			60	26	31	45.1	56	
			25	14	16	30.6	41.2	

1. Guaranteed by characterization results.
2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.
3. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.73 mA per ADC for the analog part.

Table 35. Peripheral current consumption (continued)

Peripheral		I_{DD}(Typ)(1)			Unit
		Scale 1	Scale 2	Scale 3	
APB2 (up to 108 MHz)	TIM1	24.9	23.8	20	µA/MHz
	TIM8	24.5	23.7	20	
	USART1	12.4	11.6	10	
	USART6	12.3	11.7	10	
	ADC1(5)	6.3	5.8	4.9	
	ADC2(5)	6.3	5.6	4.9	
	ADC3(5)	6.4	5.8	5	
	SDMMC1	9.1	8.3	7.1	
	SDMMC2	7	7.2	6	
	SPI1/I2S1(3)	3.2	3.2	2.6	
	SPI4	2.9	2.9	2.2	
	SYSCFG	1	1	0.7	
	TIM9	9.9	9.1	7.8	
	TIM10	7	6.4	5.6	
	TIM11	7.2	6.8	5.7	
	SPI5	4.8	4.1	3.6	
	SAI1	5.6	4.9	4.2	
	SAI2	5.4	4.7	4	
	USB PHY HS Controller	8.3	7.9	6.7	

1. When the I/O compensation cell is ON, I_{DD} typical value increases by 0.22 mA.
2. The BusMatrix is automatically active when at least one master is ON.
3. To enable an I2S peripheral, first set the I2SMOD bit and then the I2SE bit in the SPI_I2SCFGR register.
4. When the DAC is ON and EN1/2 bits are set in DAC_CR register, add an additional power consumption of 0.75 mA per DAC channel for the analog part.
5. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.73 mA per ADC for the analog part.

Table 45. PLLI2S characteristics (continued)

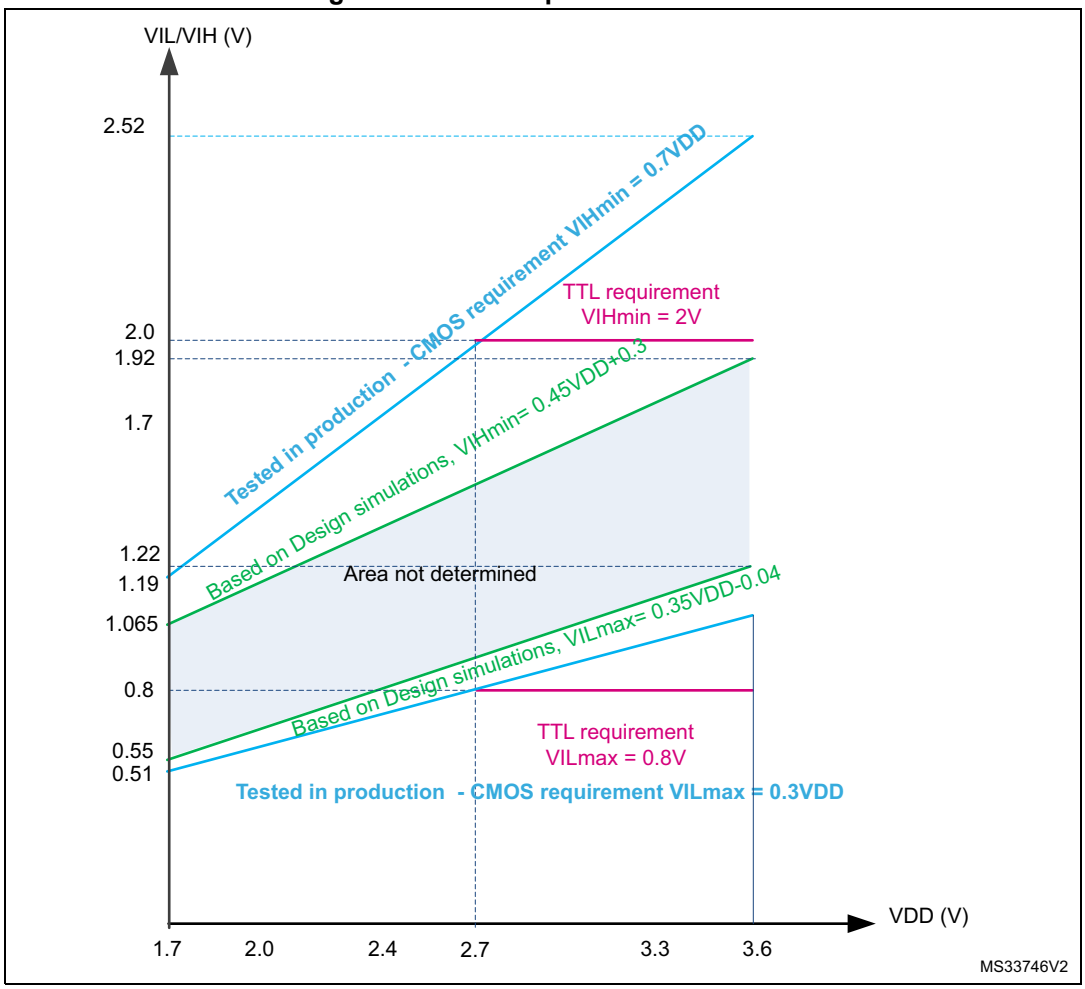
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Jitter(3)	Master I2S clock jitter	Cycle to cycle at 12.288 MHz on 48KHz period, N=432, R=5	RMS	-	90	-	ps
			peak to peak	-	±280	-	ps
		Average frequency of 12.288 MHz N = 432, R = 5 on 1000 samples		-	90	-	ps
	WS I2S clock jitter	Cycle to cycle at 48 KHz on 1000 samples		-	400	-	ps
$I_{DD(PLLI2S)}$(4)	PLLI2S power consumption on V_{DD}	VCO freq = 100 MHz VCO freq = 432 MHz		0.15 0.45	-	0.40 0.75	mA
$I_{DDA(PLLI2S)}$(4)	PLLI2S power consumption on V_{DDA}	VCO freq = 100 MHz VCO freq = 432 MHz		0.30 0.55	-	0.40 0.85	mA

1. Take care of using the appropriate division factor M to have the specified PLL input clock values.
2. Guaranteed by design.
3. Value given with main PLL running.
4. Guaranteed by characterization results.

Table 46. PLLISAI characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{PLLSAI_IN}	PLLSAI input clock(1)	-		0.95(2)	1	2.10	MHz
$f_{PLLSAIP\_OUT}$	PLLSAI multiplier output clock for 48 MHz	-		-	48	75	
$f_{PLLSAIQ\_OUT}$	PLLSAI multiplier output clock for SAI	-		-	-	216	
f_{VCO_OUT}	PLLSAI VCO output	-		100	-	432	
t_{LOCK}	PLLSAI lock time	VCO freq = 100 MHz		75	-	200	µs
		VCO freq = 432 MHz		100	-	300	
Jitter(3)	Master SAI clock jitter	Cycle to cycle at 12.288 MHz on 48KHz period, N=432, R=5	RMS	-	90	-	ps
			peak to peak	-	±280	-	ps
		Average frequency of 12.288 MHz N = 432, R = 5 on 1000 samples		-	90	-	ps
	FS clock jitter	Cycle to cycle at 48 KHz on 1000 samples		-	400	-	ps

Figure 43. FT I/O input characteristics



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA (with a relaxed V_{OL}/V_{OH}) except PC13, PC14, PC15 and PI8 which can sink or source up to ±3mA. When using the PC13 to PC15 and PI8 GPIOs in output mode, the speed should not exceed 2 MHz with a maximum load of 30 pF.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*. In particular:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 14*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 14*).

Output voltage levels

Unless otherwise specified, the parameters given in *Table 62* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 16*. All I/Os are CMOS and TTL compliant.

SAI characteristics

Unless otherwise specified, the parameters given in *Table 83* for SAI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and VDD supply voltage conditions summarized in *Table 16*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C=30 pF
- Measurement points are performed at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.20: I/O port characteristics* for more details on the input/output alternate function characteristics (SCK,SD,WS).

Table 83. SAI characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCKL}	SAI Main clock output	-	256x8K	256xFs	MHz
F_{CK}	SAI clock frequency(2)	Master data: 32 bits	-	128xFs(3)	
		Slave data: 32 bits	-	128xFs(3)	
$t_{v(FS)}$	FS valid time	Master mode 2.7≤VDD≤3.6V	-	18	ns
		Master mode 1.71≤VDD≤3.6V	-	20	
$t_{su(FS)}$	FS setup time	Slave mode	1	-	
$t_{h(FS)}$	FS hold time	Master mode	7	-	
		Slave mode	0.5	-	
$t_{su(SD\_A\_MR)}$	Data input setup time	Master receiver	1	-	
$t_{su(SD\_B\_SR)}$		Slave receiver	2.5	-	
$t_{h(SD\_A\_MR)}$	Data input hold time	Master receiver	3.5	-	
$t_{h(SD\_B\_SR)}$		Slave receiver	0.5	-	
$t_{v(SD\_B\_MT)}$	Data output valid time	Slave transmitter (after enable edge) 2.7≤VDD≤3.6V	-	11	
		Slave transmitter (after enable edge) 1.71≤VDD≤3.6V	-	18	
$t_{h(SD\_B\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	5	-	
$t_{v(SD\_A\_MT)}$	Data output valid time	Master transmitter (after enable edge) 2.7≤VDD≤3.6V	-	16	
		Master transmitter (after enable edge) 1.71≤VDD≤3.6V	-	18.5	
$t_{h(SD\_A\_MT)}$	Data output hold time	Master transmitter (after enable edge)	7.5	-	

1. Guaranteed by characterization results.
2. APB clock frequency must be at least twice SAI clock frequency.
3. With Fs = 192 KHz.

Table 104. Synchronous non-multiplexed PSRAM write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{(CLK)}$	FMC_CLK period	2Thclk - 0.5	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2	
$t_{(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	Thclk +0.5	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	0.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	3	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	Thclk	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	1.5	
$t_{d(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	Thclk +1	-	
$t_{d(CLKL-Data)}$	FMC_D[15:0] valid data after FMC_CLK low	-	3	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	-	2	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	Thclk +1	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	3.5	-	

1. Guaranteed by characterization results.

NAND controller waveforms and timings

Figure 68 through *Figure 71* represent synchronous waveforms, and *Table 105* and *Table 106* provide the corresponding timings. The results shown in this table are obtained with the following FMC configuration:

- COM.FMC_SetupTime = 0x01;
- COM.FMC_WaitSetupTime = 0x03;
- COM.FMC_HoldSetupTime = 0x02;
- COM.FMC_HiZSetupTime = 0x01;
- ATT.FMC_SetupTime = 0x01;
- ATT.FMC_WaitSetupTime = 0x03;
- ATT.FMC_HoldSetupTime = 0x02;
- ATT.FMC_HiZSetupTime = 0x01;
- Bank = FMC_Bank_NAND;
- MemoryDataWidth = FMC_MemoryDataWidth_16b;
- ECC = FMC_ECC_Enable;
- ECCPageSize = FMC_ECCPageSize_512Bytes;
- TCLRSetupTime = 0;
- TARSetupTime = 0.

In all timing tables, the T_{HCLK} is the HCLK clock period.

Figure 68. NAND controller waveforms for read access

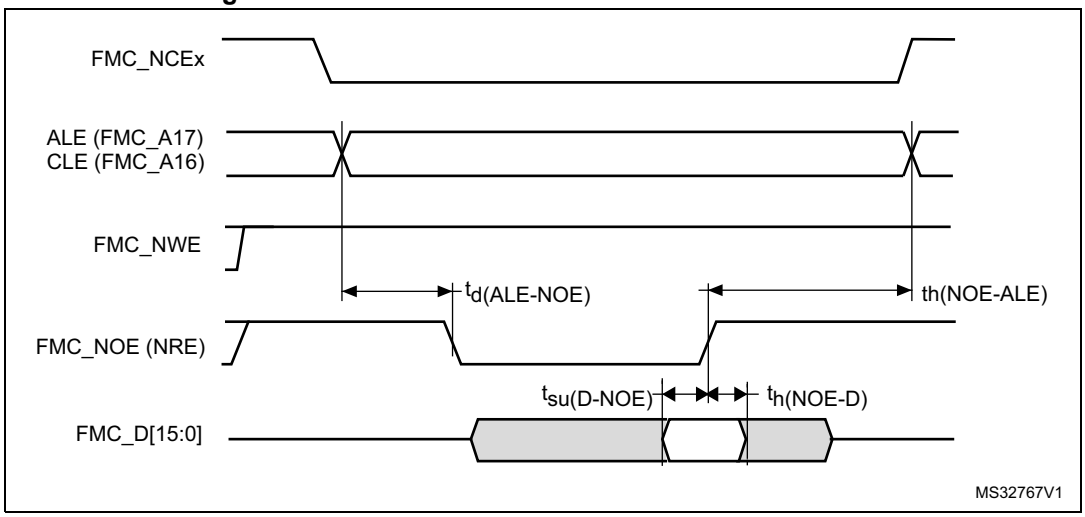


Figure 69. NAND controller waveforms for write access

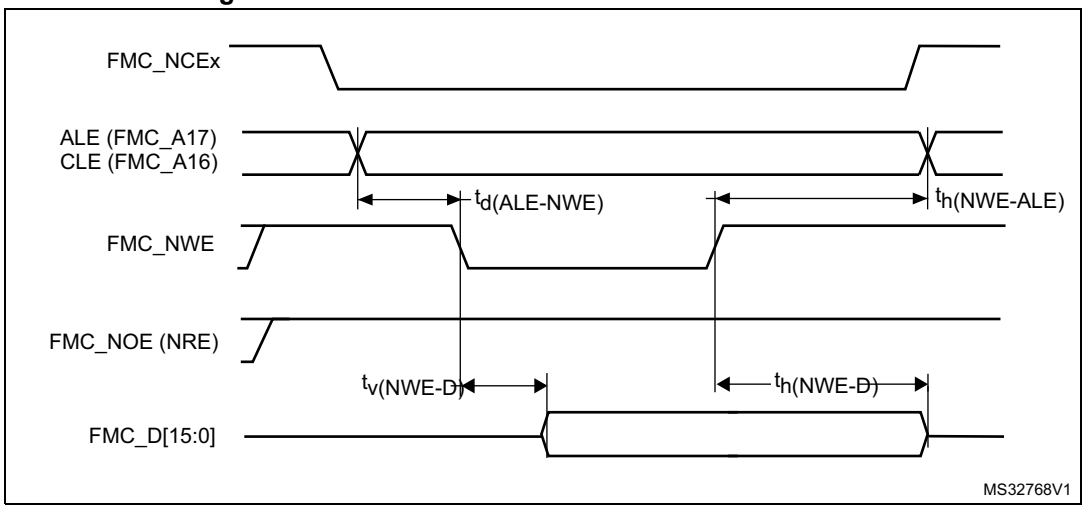
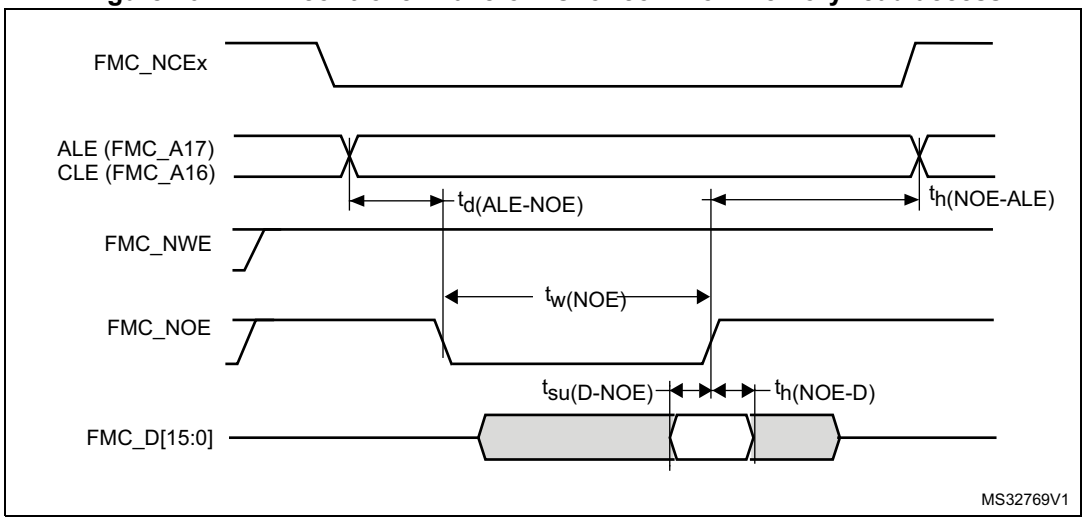


Figure 70. NAND controller waveforms for common memory read access



SDRAM waveforms and timings

- CL = 30 pF on data and address lines. CL = 10 pF on FMC_SDCLK unless otherwise specified.

In all timing tables, the T_{HCLK} is the HCLK clock period.

- For 3.0 V≤V_{DD}≤3.6 V, maximum FMC_SDCLK= 100 MHz at CL=20 pF (on FMC_SDCLK).
- For 2.7 V≤V_{DD}≤3.6 V, maximum FMC_SDCLK = 90 MHz at CL=30 pF (on FMC_SDCLK).
- For 1.71 V≤V_{DD}<1.9 V, maximum FMC_SDCLK = 70 MHz at CL=10 pF (on FMC_SDCLK).

Figure 72. SDRAM read access waveforms (CL = 1)

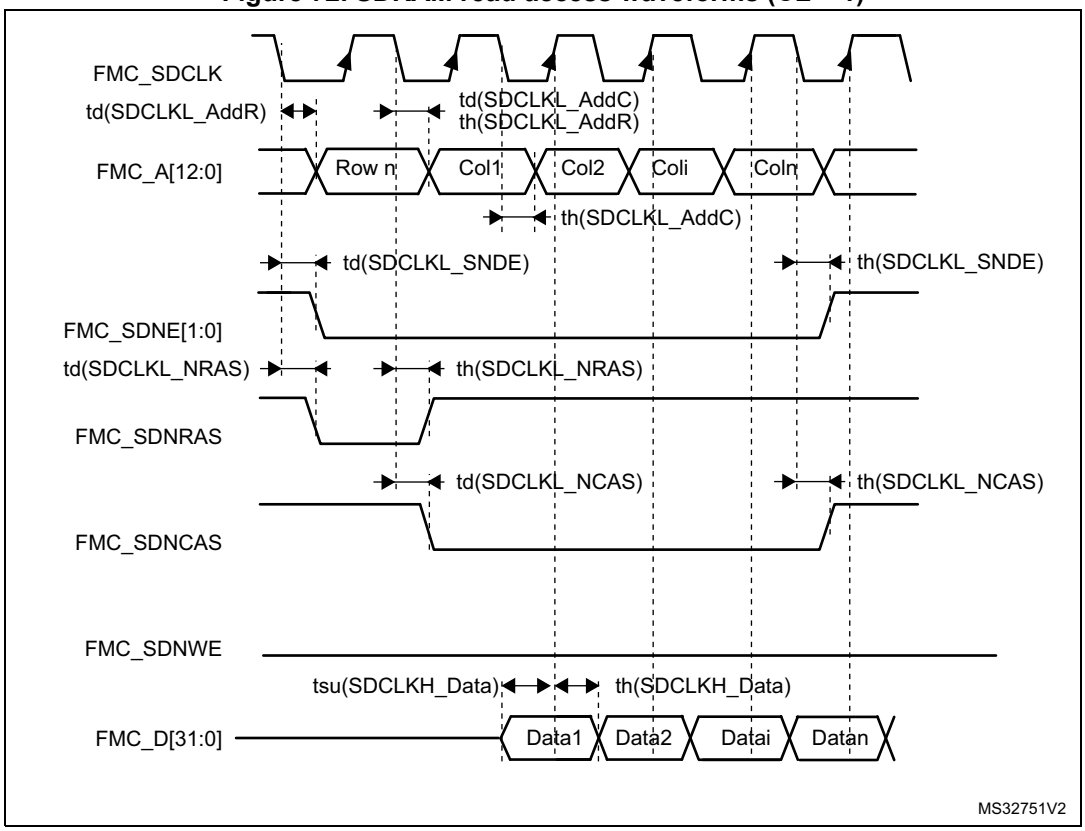
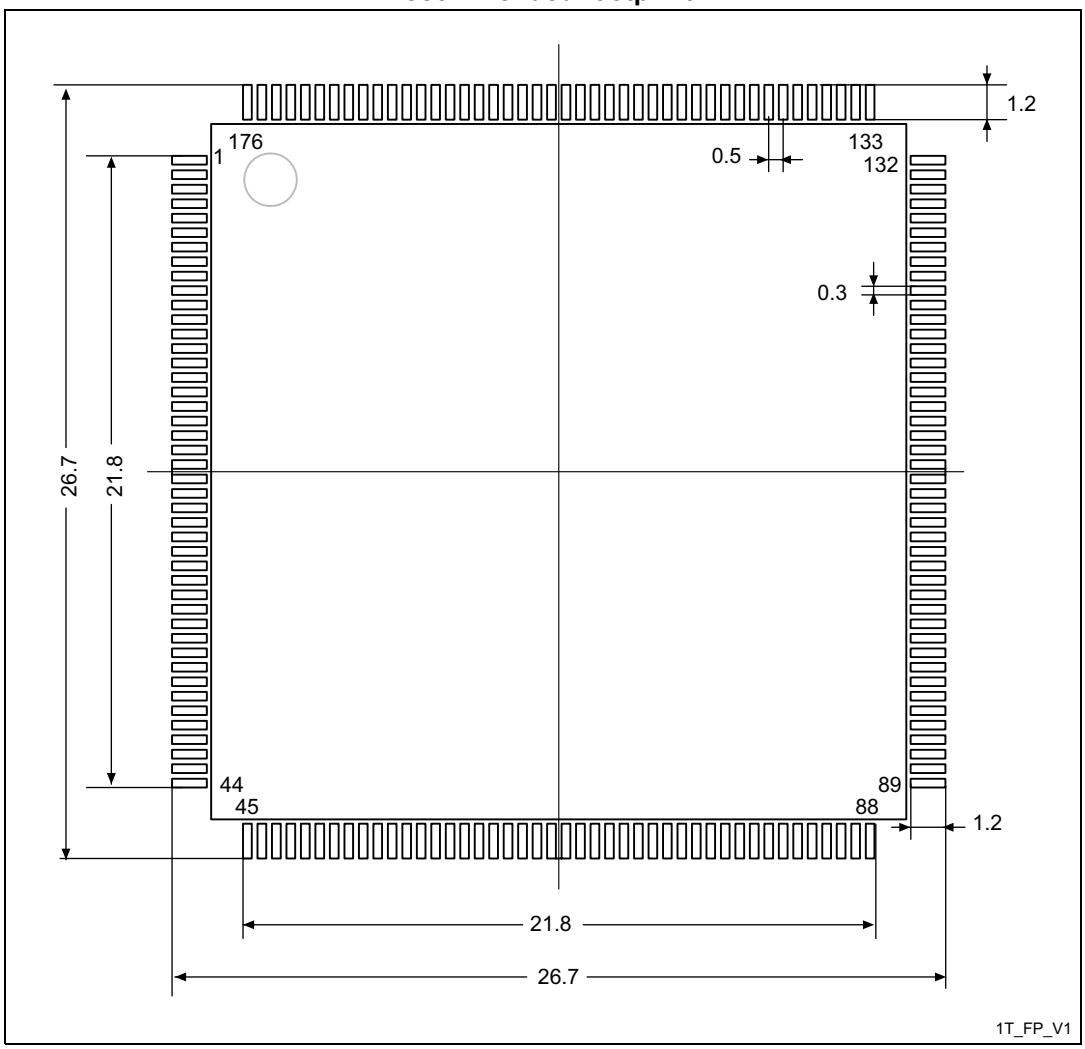


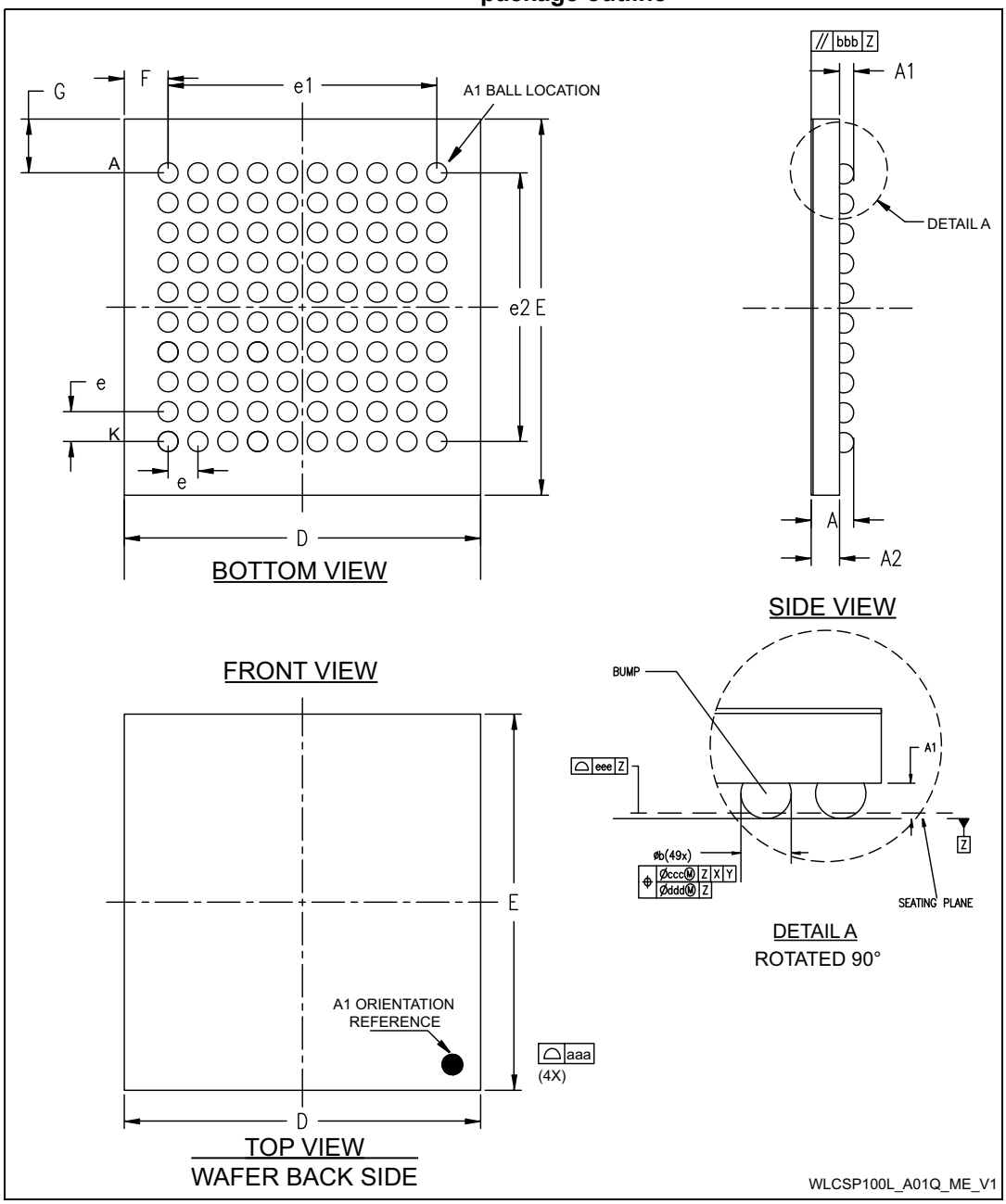
Figure 88. LQFP176, 24 x 24 mm, 176-pin low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

7.7 WLCSP100 - 0.4 mm pitch wafer level chip scale package information

Figure 96. WLCSP100 – 100L, 4.166 x 4.628 mm 0.4 mm pitch wafer level chip scale package outline



1. Drawing is not to scale.

Table 123. WLCSP100 – 100L, 4.166 x 4.628 mm 0.4 mm pitch wafer level chip scale package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Typ	Min	Max
A	0.525	0.555	0.585	0.0207	0.0219	0.0230
A1	-	0.17	-	-	0.0067	-
A2	-	0.38	-	-	0.0150	-
A3[2]	-	0.025	-	-	0.0010	-
Ø b[3]	0.22	0.25	0.28	-	0.0098	0.0110
D	4.166	4.201	4.236	-	0.1654	0.1668
E	4.628	4.663	4.698	-	0.1836	0.1850
e	-	0.4	-	-	0.0157	-
e1	-	3.6	-	-	0.1417	-
e2	-	3.6	-	-	0.1417	-
F	-	0.3005	-	-	0.0118	-
G	-	0.5315	-	-	0.0209	-
N	-	100	-	-	3.9370	-
aaa	-	0.1	-	-	0.0039	-
bbb	-	0.1	-	-	0.0039	-
ccc	-	0.1	-	-	0.0039	-
ddd	-	0.05	-	-	0.0020	-
eee	-	0.05	-	-	0.0020	-

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Back side coating.
3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.