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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	216MHz
Connectivity	CANbus, EBI/EMI, I ² C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	112
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-UFBGA
Supplier Device Package	144-UFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f733zei6

2 Description

The STM32F732xx and STM32F733xx devices are based on the high-performance Arm® Cortex®-M7 32-bit RISC core operating at up to 216 MHz frequency. The Cortex®-M7 core features a single floating point unit (SFPU) precision which supports Arm® single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances the application security.

The STM32F732xx and STM32F733xx devices incorporate high-speed embedded memories with a Flash memory up to 512 Kbytes, 256 Kbytes of SRAM (including 64 Kbytes of data TCM RAM for critical real-time data), 16 Kbytes of instruction TCM RAM (for critical real-time routines), 4 Kbytes of backup SRAM available in the lowest power modes, and an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses, a 32-bit multi-AHB bus matrix and a multi layer AXI interconnect supporting internal and external memories access.

All the devices offer three 12-bit ADCs, two DACs, a low-power RTC, thirteen general-purpose 16-bit timers including two PWM timers for motor control, two general-purpose 32-bit timers, a true random number generator (RNG). They also feature standard and advanced communication interfaces.

- Up to three I²Cs
- Five SPIs, three I²Ss in half duplex mode. To achieve the audio class accuracy, the I²S peripherals can be clocked via a dedicated internal audio PLL or via an external clock to allow synchronization.
- Four USARTs plus four UARTs
- An USB OTG full-speed and a USB OTG high-speed with full-speed capability (with the ULPI in the STM32F732xx devices and with the integrated HS PHY in the STM32F733xx devices)
- One CAN
- Two SAI serial audio interfaces
- Two SDMMC host interfaces

Advanced peripherals include two SDMMC interfaces, a flexible memory control (FMC) interface, a Quad-SPI Flash memory interface.

The STM32F732xx and STM32F733xx devices operate in the –40 to +105 °C temperature range from a 1.7 to 3.6 V power supply. Dedicated supply inputs for the USB (OTG_FS and OTG_HS) and the SDMMC2 (clock, command and 4-bit data) are available on all the packages except LQFP100 and LQFP64 for a greater power supply choice.

The supply voltage can drop to 1.7 V with the use of an external power supply supervisor. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F732xx and STM32F733xx devices offer devices in 7 packages ranging from 64 pins to 176 pins. The set of included peripherals changes with the device chosen.

3.16.3 Regulator ON/OFF and internal reset ON/OFF availability

Table 4. Regulator ON/OFF and internal reset ON/OFF availability

Package	Regulator ON	Regulator OFF	Internal reset ON	Internal reset OFF
LQFP64, LQFP100	Yes	No	Yes	No
LQFP144			Yes PDR_ON set to V_{DD}	Yes PDR_ON set to V_{SS}
LQFP176, UFBGA144, UFBGA176	Yes BYPASS_REG set to V_{SS}	Yes BYPASS_REG set to V_{DD}		

3.17 Real-time clock (RTC), backup SRAM and backup registers

The RTC is an independent BCD timer/counter. It supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.
- Two programmable alarms.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy.
- Three anti-tamper detection pins with programmable filter.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event, or by a switch to V_{BAT} mode.
- 17-bit auto-reload wakeup timer (WUT) for periodic events with programmable resolution and period.

The RTC and the 32 backup registers are supplied through a switch that takes power either from the V_{DD} supply when present or from the V_{BAT} pin.

The backup registers are 32-bit registers used to store 128 bytes of user application data when V_{DD} power is not present. They are not reset by a system or power reset, or when the device wakes up from Standby mode.

The RTC clock sources can be:

- A 32.768 kHz external crystal (LSE)
- An external resonator or oscillator (LSE)
- The internal low power RC oscillator (LSI, with typical frequency of 32 kHz)
- The high-speed external clock (HSE) divided by 32

The RTC is functional in V_{BAT} mode and in all low-power modes when it is clocked by the LSE. When clocked by the LSI, the RTC is not functional in V_{BAT} mode, but is functional in all low-power modes.

3.29 Universal serial bus on-the-go full-speed (OTG_FS)

The device embeds an USB OTG full-speed device/host/OTG peripheral with integrated transceivers. The USB OTG FS peripheral is compliant with the USB 2.0 specification and with the OTG 2.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator.

The major features are:

- Combined Rx and Tx FIFO size of 1.28 Kbytes with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 1 bidirectional control endpoint + 5 IN endpoints + 5 OUT endpoints
- 12 host channels with periodic OUT support
- Software configurable to OTG1.3 and OTG2.0 modes of operation
- USB 2.0 LPM (Link Power Management) support
- Internal FS OTG PHY support
- HNP/SNP/IP inside (no need for any external resistor)
- BCD support

For the OTG/Host modes, a power switch is needed in case bus-powered devices are connected

3.30 Universal serial bus on-the-go high-speed (OTG_HS)

The device embeds an USB OTG high-speed (up to 480 Mbit/s) device/host/OTG peripheral. The USB OTG HS supports both full-speed and high-speed operations. It integrates the transceivers for full-speed operation (12 Mbit/s).

The STM32F732xx devices feature a UTMI low-pin interface (ULPI) for high-speed operation (480 Mbit/s). When using the USB OTG HS in HS mode, an external PHY device connected to the ULPI is required.

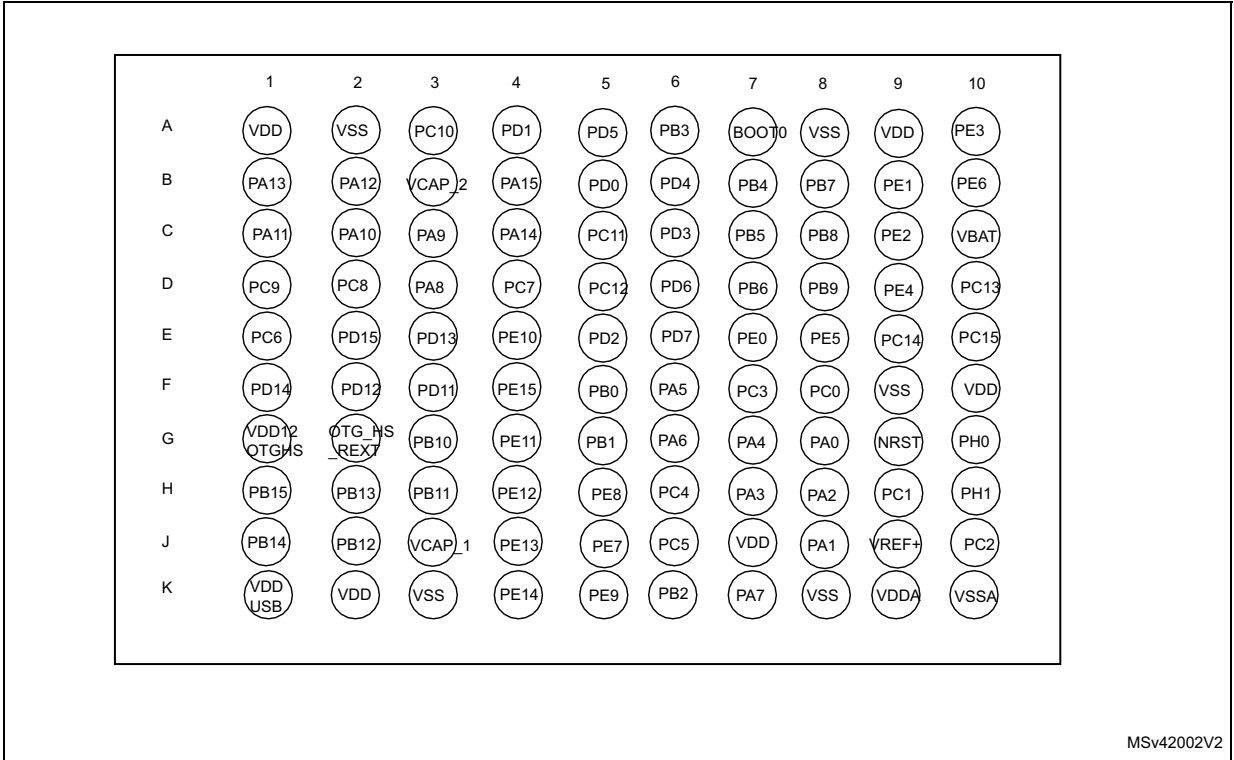
The STM32F733xx devices feature an integrated PHY HS.

The USB OTG HS peripheral is compliant with the USB 2.0 specification and with the OTG 2.0 specification. It has a software-configurable endpoint setting and supports suspend/resume. The USB OTG controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator.

The major features are:

- Combined Rx and Tx FIFO size of 4 Kbytes with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 8 bidirectional endpoints
- 16 host channels with periodic OUT support
- Software configurable to OTG1.3 and OTG2.0 modes of operation
- USB 2.0 LPM (Link Power Management) support

Figure 16. STM32F733xx WLCSP100 ballout (with OTG PHY HS)



1. The above figure shows the package top view.

Figure 19. STM32F733xx UFBGA144 ballout (with OTG PHY HS)

	1	2	3	4	5	6	7	8	9	10	11	12
A	PC13	PE3	PE2	PE1	PE0	PB4	PB3	PD6	PD7	PA15	PA14	PA13
B	PC14- OSC32_IN	PE4	PE5	PE6	PB9	PB5	PG15	PG12	PD5	PC11	PC10	PA12
C	PC15- OSC32_OUT	VBAT	PF0	PF1	PB8	PB6	PG14	PG11	PD4	PC12	VDDUSB	PA11
D	PH0 - OSC_IN	VSS	VDD	PF2	BOOT0	PB7	PG13	PG10	PD3	PD1	PA10	PA9
E	PH1 - OSC_OUT	PF3	PF4	PF5	PDR_ON	VSS	VSS	PG9	PD2	PD0	PC9	PA8
F	NRST	PF7	PF6	VDD	VDD	VDD	VDD	VDD	VDD	VDD	PC8	PC7
G	PF10	PF9	PF8	VSS	VDD	VDD	VDD	VSS	VCAP_2	VSS	PG8	PC6
H	PC0	PC1	PC2	PC3	BYPASS_ REG	VSS	VCAP_1	PE11	PD11	VDD12OTG HS	OTG_HS _REXT	PG5
J	VSSA	PA0	PA4	PC4	PB2	PG1	PE10	PE12	PD10	PG4	PG3	PG2
K	VREF-	PA1	PA5	PC5	PF13	PG0	PE9	PE13	PD9	PD13	PD14	PD15
L	VREF+	PA2	PA6	PB0	PF12	PF15	PE8	PE14	PD8	PD12	PB14	PB15
M	VDDA	PA3	PA7	PB1	PF11	PF14	PE7	PE15	PB10	PB11	PB12	PB13

MSv42000V1

1. The above figure shows the package top view.

Table 10. STM32F732xx and STM32F733xx pin and ball definition (continued)

Pin Number										Pin name (function after reset) ⁽¹⁾	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F732xx					STM32F733xx										
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
39	65	98	G14	117	D2	G14	F11	98	117	PC8	I/O	FT	-	TRACED1, TIM3_CH3, TIM8_CH3, UART5_RTS, USART6_CK, SDMMC1_D0, EVENTOUT	-
40	66	99	F14	118	D1	F14	E11	99	118	PC9	I/O	FTf	-	MCO2, TIM3_CH4, TIM8_CH4, I2C3_SDA, I2S_CKIN, UART5_CTS, QUADSPI_BK1_IO0, SDMMC1_D1, EVENTOUT	-
41	67	100	F15	119	D3	F15	E12	100	119	PA8	I/O	FTf	-	MCO1, TIM1_CH1, TIM8_BKIN2, I2C3_SCL, USART1_CK, OTG_FS_SOF, EVENTOUT	-
42	68	101	E15	120	C3	E15	D12	101	120	PA9	I/O	FT	-	TIM1_CH2, I2C3_SMBA, SPI2_SCK/I2S2_CK, USART1_TX, EVENTOUT	OTG_FS_VBUS
43	69	102	D15	121	C2	D15	D11	102	121	PA10	I/O	FT	-	TIM1_CH3, USART1_RX, OTG_FS_ID, EVENTOUT	-
44	70	103	C15	122	C1	C15	C12	103	122	PA11	I/O	FT	-	TIM1_CH4, USART1_CTS, CAN1_RX, OTG_FS_DM, EVENTOUT	-
45	71	104	B15	123	B2	B15	B12	104	123	PA12	I/O	FT	-	TIM1_ETR, USART1_RTS, SAI2_FS_B, CAN1_TX, OTG_FS_DP, EVENTOUT	-
46	72	105	A15	124	B1	A15	A12	105	124	PA13(JTMS-SWDIO)	I/O	FT	-	JTMS-SWDIO, EVENTOUT	-

5 Memory mapping

Refer to the product line reference manual for details on the memory mapping as well as the boundary addresses for all peripherals.

pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

Where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DD} is the MCU supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT}$

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

Table 34. Switching output I/O current consumption⁽¹⁾

Symbol	Parameter	Conditions	I/O toggling frequency (fsw) MHz	Typ $V_{DD} = 3.3\text{ V}$	Typ $V_{DD} = 1.8\text{ V}$	Unit
I_{DDIO}	I/O switching Current	$C_{EXT} = 0\text{ pF}$ $C = C_{INT} + C_S + C_{EXT}$	2	0.1	0.1	mA
			8	0.4	0.2	
			25	1.1	0.7	
			50	2.4	1.3	
			60	3.1	1.6	
			84	4.3	2.4	
			90	4.9	2.6	
			100	5.4	2.8	
			108	5.6	-	
		$C_{EXT} = 10\text{ pF}$ $C = C_{INT} + C_S + C_{EXT}$	2	0.2	0.1	
			8	0.6	0.3	
			25	1.8	1.1	
			50	3.1	2.3	
			60	4.6	3.4	
			84	9.7	3.6	
			90	10.12	5.2	
			100	14.92	5.4	
			108	18.11	-	

USB OTG HS and USB OTG HS PHY current consumption (on STM32F733xx devices)

The MCU is placed under the following conditions:

- STM32 MCU is enumerated as a HID device.
- $f_{HCLK} = 216 \text{ MHz}$ (Scale 1 + over-drive ON), $f_{HCLK} = 168 \text{ MHz}$ (Scale 2), $f_{HCLK} = 144 \text{ MHz}$ (Scale 3)

The given value is calculated by measuring the difference of current consumption in case:

- USB is configured but no transfer is done.
- USB is configured and there is a transmission on going.
- Ambient operating temperature is 25°C , $V_{DD} = V_{DDUSB} = 3.3 \text{ V}$.

Table 36. USB OTG HS and USB OTG PHY HS current consumption

	I_{DD} (Typ)			Unit
	Scale 1	Scale 2	Scale 3	
USB OTG HS and USB OTG HS PHY current consumption	50.16	44.92	38.98	mA

6.3.8 Wakeup time from low-power modes

The wakeup times given in [Table 37](#) are measured starting from the wakeup event trigger up to the first instruction executed by the CPU:

- For Stop or Sleep modes: the wakeup event is WFE.
- WKUP (PA0) pin is used to wakeup from Standby, Stop and Sleep modes.

All timings are derived from tests performed under ambient temperature and $V_{DD}=3.3 \text{ V}$.

Table 37. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ ⁽¹⁾	Max ⁽¹⁾	Unit
$t_{WUSLEEP}^{(2)}$	Wakeup from Sleep	-	13	13	CPU clock cycles
$t_{WUSTOP}^{(2)}$	Wakeup from Stop mode with MR/LP regulator in normal mode	Main regulator is ON	14	14.9	μs
		Main regulator is ON and Flash memory in Deep power down mode	104.1	107.6	
		Low power regulator is ON	21.4	24.2	
		Low power regulator is ON and Flash memory in Deep power down mode	111.5	116.5	

Table 62. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin	CMOS port ⁽²⁾ $I_{IO} = +8 \text{ mA}$ $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	0.4	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin except PC14	CMOS port ⁽²⁾ $I_{IO} = -8 \text{ mA}$ $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	$V_{DD} - 0.4$	-	
$V_{OH}^{(3)}$	Output high level voltage for PC14	CMOS port ⁽²⁾ $I_{IO} = -2 \text{ mA}$ $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	$V_{DD} - 0.4$	-	
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin	TTL port ⁽²⁾ $I_{IO} = +8 \text{ mA}$ $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	0.4	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin except PC14	TTL port ⁽²⁾ $I_{IO} = -8 \text{ mA}$ $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	2.4	-	
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin	$I_{IO} = +20 \text{ mA}$ $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	1.3 ⁽⁴⁾	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin except PC14	$I_{IO} = -20 \text{ mA}$ $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	$V_{DD} - 1.3^{(4)}$	-	
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin	$I_{IO} = +6 \text{ mA}$ $1.8 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	0.4 ⁽⁴⁾	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin except PC14	$I_{IO} = -6 \text{ mA}$ $1.8 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	$V_{DD} - 0.4^{(4)}$	-	
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin	$I_{IO} = +4 \text{ mA}$ $1.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	0.4 ⁽⁵⁾	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin except PC14	$I_{IO} = -4 \text{ mA}$ $1.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	$V_{DD} - 0.4^{(5)}$	-	
$V_{OH}^{(3)}$	Output high level voltage for PC14	$I_{IO} = -1 \text{ mA}$ $1.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	$V_{DD} - 0.4^{(5)}$	-	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in [Table 14](#). and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS} .
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in [Table 14](#) and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD} .
4. Based on characterization data.
5. Guaranteed by design.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in [Figure 44](#) and [Table 63](#), respectively.

Table 79. Minimum I2CCLK frequency in all I2C modes

Symbol	Parameter	Condition		Min	Unit
f(I2CCLK)	I2CCLK frequency	Standard-mode	-	2	MHz
		Fast-mode	Analog Filter ON DNF=0	10	
			Analog Filter OFF DNF=1	9	
		Fast-mode Plus	Analog Filter ON DNF=0	22.5	
			Analog Filter OFF DNF=1	16	

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

The 20mA output drive requirement in Fast-mode Plus is not supported. This limits the maximum load C_{load} supported in Fm+, which is given by these formulas:

- $Tr(SDA/SCL) = 0.8473 \times R_p \times C_{load}$
- $R_p(min) = (V_{DD} - V_{OL(max)}) / I_{OL(max)}$

Where R_p is the I2C lines pull-up. Refer to [Section 6.3.20: I/O port characteristics](#) for the I2C I/Os characteristics.

All I²C SDA and SCL I/Os embed an analog filter. Refer to the table below for the analog filter characteristics:

Table 80. I2C analog filter characteristics⁽¹⁾

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	50 ⁽²⁾	260 ⁽³⁾	ns

1. Guaranteed by characterization results.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered

Table 93. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings⁽¹⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	2Thclk -1	2Thclk +1	ns
$t_{v(NOE_NE)}$	FMC_NEx low to FMC_NOE low	0	0.5	
$t_{w(NOE)}$	FMC_NOE low time	2Thclk -1	2Thclk +1	
$t_{h(NE_NOE)}$	FMC_NOE high to FMC_NE high hold time	0	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	0.5	
$t_{h(A_NOE)}$	Address hold time after FMC_NOE high	0	-	
$t_{v(BL_NE)}$	FMC_NEx low to FMC_BL valid	-	0.5	
$t_{h(BL_NOE)}$	FMC_BL hold time after FMC_NOE high	0	-	
$t_{su(Data_NE)}$	Data to FMC_NEx high setup time	Thclk -1.5	-	
$t_{su(Data_NOE)}$	Data to FMC_NOEx high setup time	Thclk -1.5	-	
$t_{h(Data_NOE)}$	Data hold time after FMC_NOE high	0	-	
$t_{h(Data_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	-	0	
$t_{w(NADV)}$	FMC_NADV low time	-	Thclk -0.5	

1. $C_L = 30$ pF.

Table 94. Asynchronous non-multiplexed SRAM/PSRAM/NOR read - NWAIT timings⁽¹⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	7Thclk +1	7Thclk +1	ns
$t_{w(NOE)}$	FMC_NWE low time	5Thclk -1	5Thclk +1	
$t_{w(NWAIT)}$	FMC_NWAIT low time	Thclk -0.5	-	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	5Thclk +1.5	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	4Thclk +1	-	

1. Guaranteed by characterization results.

1. Guaranteed by characterization results.

Table 100. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings⁽¹⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	9Thclk - 1	9Thclk + 1	ns
$t_{w(NWE)}$	FMC_NWE low time	7Thclk - 0.5	7Thclk + 0.5	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	6Thclk + 2	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	4Thclk - 1	-	

1. Guaranteed by characterization results.

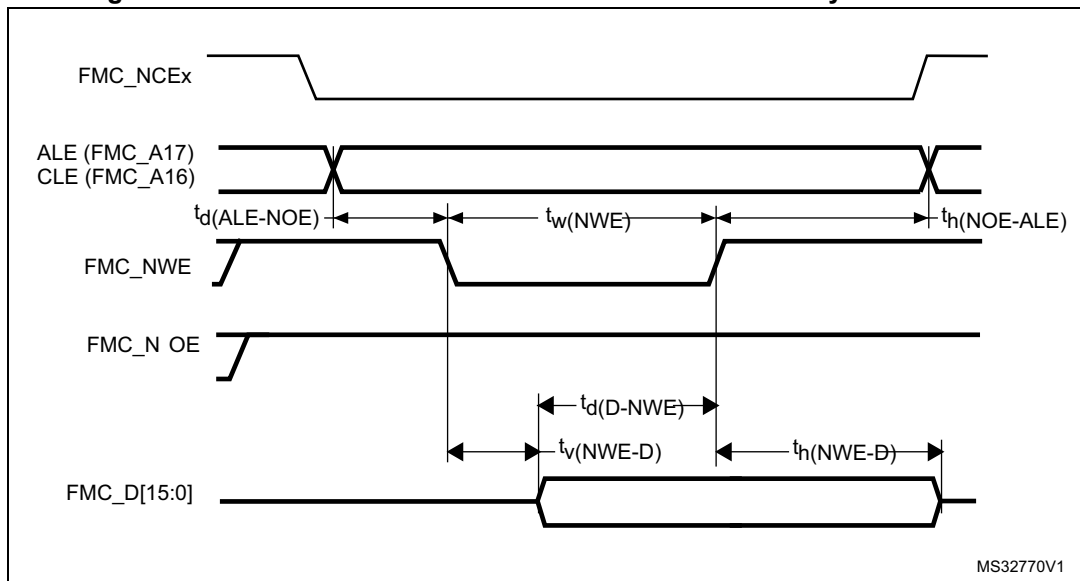
Synchronous waveforms and timings

[Figure 64](#) through [Figure 67](#) represent synchronous waveforms and [Table 101](#) through [Table 104](#) provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- BurstAccessMode = FMC_BurstAccessMode_Enable;
- MemoryType = FMC_MemoryType_CRAM;
- WriteBurst = FMC_WriteBurst_Enable;
- CLKDivision = 1;
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM
- CL = 30 pF on data and address lines. CL = 10 pF on FMC_CLK unless otherwise specified.

In all timing tables, the T_{HCLK} is the HCLK clock period.

- For $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, maximum FMC_CLK = 108 MHz at CL=20 pF or 90 MHz at CL=30 pF (on FMC_CLK).
- For $1.71\text{ V} \leq V_{DD} < 2.7\text{ V}$, maximum FMC_CLK = 70 MHz at CL=10 pF (on FMC_CLK).

Figure 71. NAND controller waveforms for common memory write access**Table 105. Switching characteristics for NAND Flash read cycles⁽¹⁾**

Symbol	Parameter	Min	Max	Unit
$t_{w(NOE)}$	FMC_NOE low width	4Thclk - 0.5	4Thclk + 0.5	ns
$t_{su(D-NOE)}$	FMC_D[15-0] valid data before FMC_NOE high	11	-	
$t_{h(NOE-D)}$	FMC_D[15-0] valid data after FMC_NOE high	0	-	
$t_d(ALE-NOE)$	FMC_ALE valid before FMC_NOE low	-	3Thclk + 1.5	
$t_{h(NOE-ALE)}$	FMC_NWE high to FMC_ALE invalid	4Thclk - 2	-	

1. Guaranteed by characterization results.

Table 106. Switching characteristics for NAND Flash write cycles⁽¹⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(NWE)}$	FMC_NWE low width	4Thclk - 0.5	4Thclk + 0.5	ns
$t_{v(NWE-D)}$	FMC_NWE low to FMC_D[15-0] valid	0	-	
$t_{h(NWE-D)}$	FMC_NWE high to FMC_D[15-0] invalid	2Thclk - 1	-	
$t_d(D-NWE)$	FMC_D[15-0] valid before FMC_NWE high	5Thclk - 1	-	
$t_d(ALE-NWE)$	FMC_ALE valid before FMC_NWE low	-	3Thclk + 1.5	
$t_{h(NWE-ALE)}$	FMC_NWE high to FMC_ALE invalid	2Thclk - 2	-	

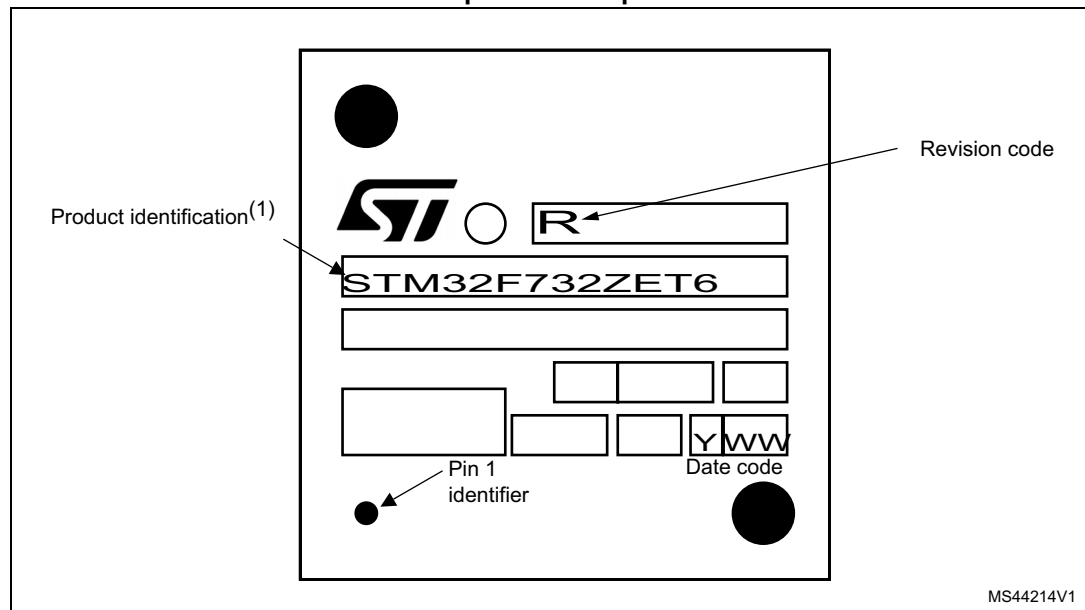
1. Guaranteed by characterization results.

LQP144 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 86. LQFP144, 20 x 20mm, 144-pin low-profile quad flat package top view example



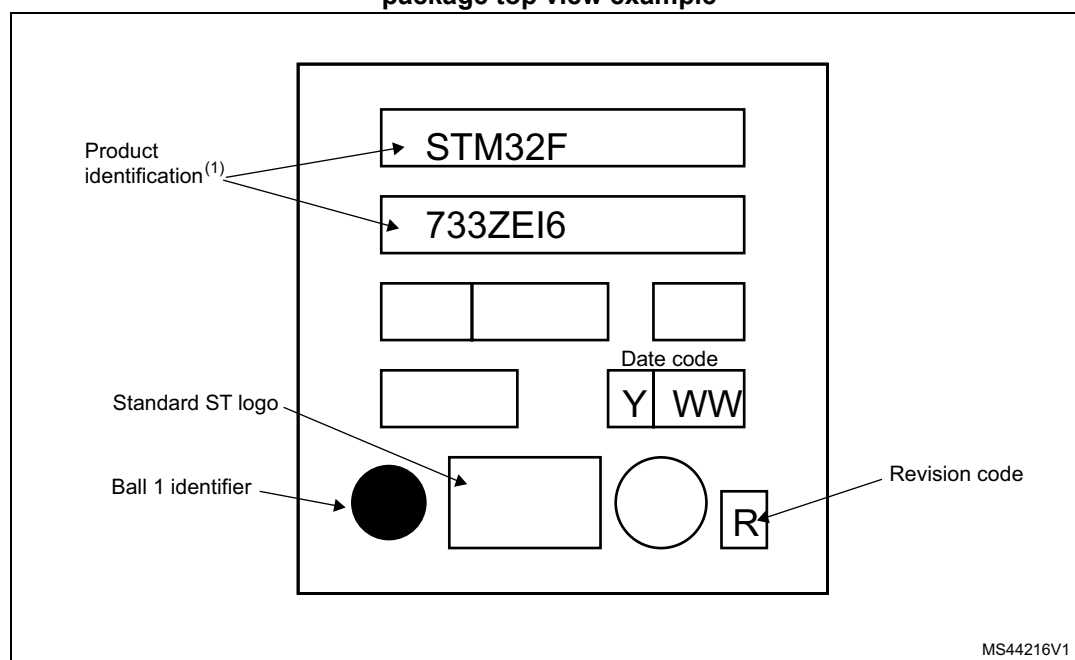
1. Parts marked as ES or E or accompanied by an engineering sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

UFBGA144 device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

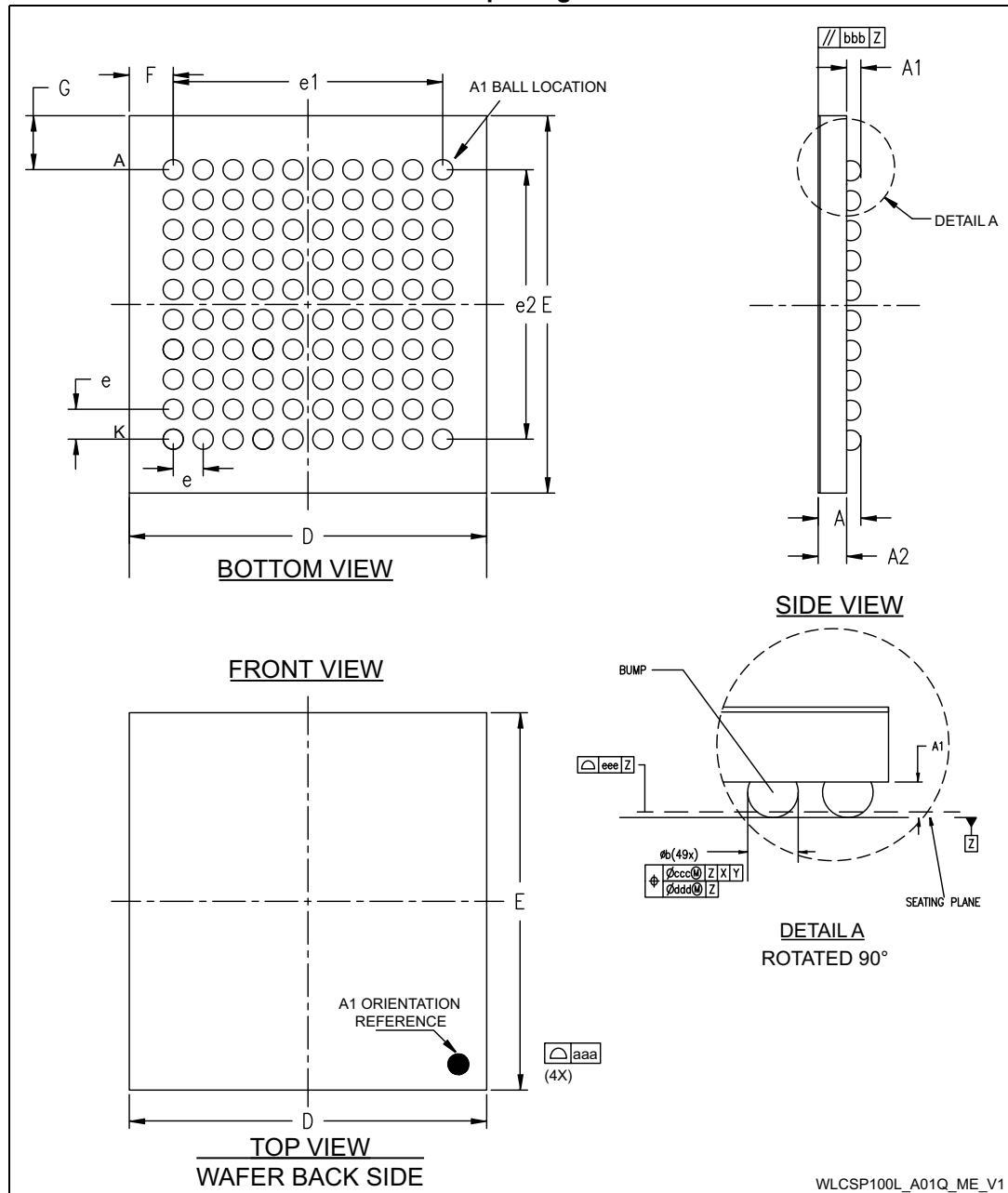
**Figure 92. UFBGA144- 144-ball, 7 x 7 mm, 0.50 mm pitch
package top view example**



1. Parts marked as ES or E or accompanied by an engineering sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.7 WLCSP100 - 0.4 mm pitch wafer level chip scale package information

Figure 96. WLCSP100 – 100L, 4.166 x 4.628 mm 0.4 mm pitch wafer level chip scale package outline



1. Drawing is not to scale.

Figure 97. WLCSP100 – 100L, 4.166 x 4.628 mm 0.4 mm pitch wafer level chip scale package recommended footprint

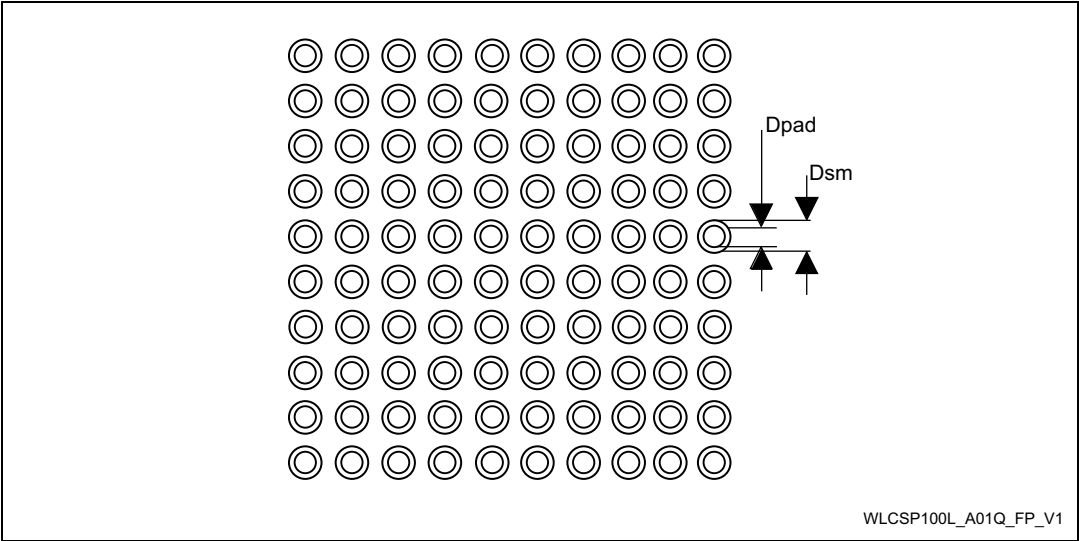


Table 124. WLCSP100 recommended PCB design rules (0.4 mm pitch)

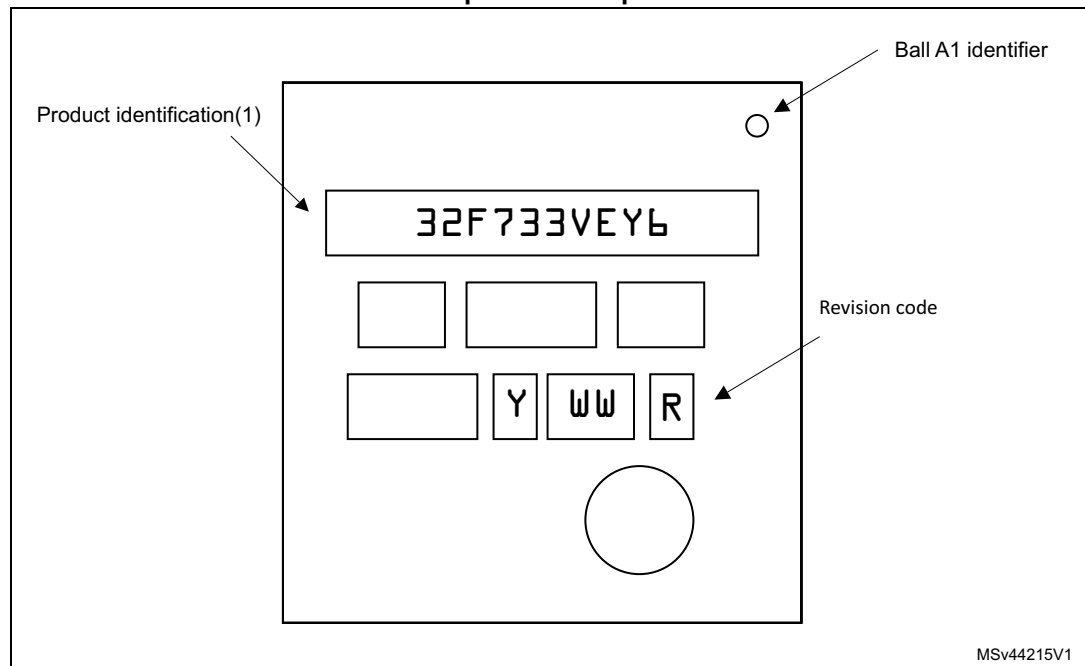
Dimension	Recommended values
Pitch	0.4 mm
Dpad	0.225 mm
Dsm	0.290 mm
Stencil thickness	0.1 mm

WLCSP100 device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

**Figure 98. WLCSP100 – 100L, 4.166 x 4.628 mm 0.4 mm pitch
top view example**



1. Parts marked as ES or E or accompanied by an engineering sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.